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Rev. 7, Mar-2000

High-Speed CMOS Data

ON Semiconductor

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Function Selector Guide

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ALPHANUMERIC INDEX

BUFFERS/INVERTERS

Device Number MC74	Function	Functional Equivalent LSTTL Device 74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC04A	Hex Inverter	LS04	*4069	LS/CMOS	14
HCT04A	Hex Inverter with LSTTL–Compatible Inputs	LS04	*4069	LS/CMOS	14
HCU04A	Hex Unbuffered Inverter	LS04	4069	LS/CMOS	14
HC14A	Hex Schmitt–Trigger Inverter	LS14	4584	LS/CMOS	14
HCT14A	Hex Schmitt–Trigger Inverter with LSTTL–Compatible Inputs	LS14	4584	LS/CMOS	14
HC125A	Quad 3–State Noninverting Buffer	LS125,LS125A		LS	14
HC126A	Quad 3–State Noninverting Buffer	LS126,LS126A		LS	14
HC240A	Octal 3–State Inverting Buffer/Line Driver/Line Receiver	LS240		LS	20
HC244A	Octal 3–State Noninverting Buffer/Line Driver/Line Receiver	LS244		LS	20
HCT244A	Octal 3–State Noninverting Buffer/Line Driver/Line Receiver with LSTTL–Compatible Inputs	LS244		LS	20
HC245A	Octal 3–State Noninverting Bus Transceiver	LS245		LS	20
HCT245A	Octal 3–State Noninverting Bus Transceiver with LSTTL–Compatible Inputs	LS245		LS	20
HC540A	Octal 3–State Inverting Buffer/Line Driver/Line Receiver				20
HC541A	Octal 3–State Noninverting Buffer/Line Driver/Line Receiver	LS541		LS	20
HCT541A	Octal 3–State Noninverting Buffer/Line Driver/Line Receiver with LSTTL–Compatible Inputs	LS541		LS	20

HC Devices Have CMOS–Compatible Inputs. HCT Devices Have LSTTL–Compatible Inputs.

Device	HC HCT 04A	HCU 04A	HC 14A	HC 125A	HC 126A	HC 240A	HC HCT 244A	HC HCT 245A
# Pins	14	14	14	14	14	20	20	20
Quad Device				•	•			
Hex Device	•	•	•					
Octal Device						•	•	•
Nine–Wide Device								
Noninverting Outputs				•	•		•	•
Inverting Outputs	•	•	•			•		
Single Stage (unbuffered)		•						
Schmitt Trigger			•					
3–State Outputs				•	•	•	•	•
Open–Drain Outputs								
Common Output Enables						•	•	•
Active–Low Output Enables				•		•	•	•
Active–High Output Enables					•			
Separate 4–Bit Sections						•	•	
Separate 2–Bit and 4–Bit Sections								
Transceiver								•
Direction Control								•
Logic–Level Down Converter								

BUFFERS/INVERTERS (Continued)

HC Devices Have CMOS–Compatible Inputs. HCT Devices Have LSTTL–Compatible Inputs.

Device	HC 540A	HC HCT 541A
# Pins	20	20
Quad Device Hex Device Octal Device Nine–Wide Device	●	●
Noninverting Outputs Inverting Outputs	●	●
Single Stage (unbuffered)		
Schmitt Trigger		
3–State Outputs Open–Drain Outputs Common Output Enables Active–Low Output Enables	● ● ●	● ● ●

GATES

Device Number MC74	Function	Functional Equivalent LSTTL Device 74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC00A	Quad 2–Input NAND Gate	LS00	4011	LS	14
HC02A	Quad 2–Input NOR Gate		4001		14
HC03A	Quad 2–Input NAND Gate with Open–Drain Outputs		*4011		14
HC08A	Quad 2–Input AND Gate	LS08	4081	LS	14
HC32A	Quad 2–Input OR Gate	LS32	4071	LS	14
HC86A	Quad 2–Input Exclusive OR Gate	LS86	4070	LS	14
HC132A	Quad 2–Input NAND Gate with Schmitt–Trigger Inputs	LS132	4093	LS	14

HC Devices Have CMOS–Compatible Inputs.

Device	HC 00A	HC 02A	HC 03A	HC 08A	HC 32A
# Pins	14	14	14	14	14
Single Device					
Dual Device					
Triple Device					
Quad Device	●	●	●	●	●
NAND	●		●		
NOR		●			
AND				●	
OR					●
Exclusive OR					
Exclusive NOR					
AND–NOR					
AND–OR					
2–Input	●	●	●	●	●
3–Input					
4–Input					
8–Input					
13–Input					
Schmitt–Trigger Inputs					
Open–Drain Outputs			●		

GATES (Continued)

HC Devices Have CMOS–Compatible Inputs.

Device	HC 86A	HC 132A
# Pins	14	14
Single Device Dual Device Triple Device Quad Device	●	●
NAND NOR AND OR		●
Exclusive OR Exclusive NOR AND–NOR AND–OR	●	
2–Input 3–Input 4–Input 8–Input 13–Input	●	●
Schmitt–Trigger Inputs		●
Open–Drain Outputs		

SCHMITT TRIGGERS

Device Number MC74	Function	Functional Equivalent LSTTL Device 74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC14A	Hex Schmitt–Trigger Inverter	LS14	4584	LS/CMOS	14
HCT14A	Hex Schmitt–Trigger Inverter with LSTTL–Compatible Inputs	LS14	4584	LS	14
HC132A	Quad 2–Input NAND Gate with Schmitt–Trigger Inputs	LS132	4093	LS	14

BUS TRANSCEIVERS

Device Number MC74	Function	Functional Equivalent LSTTL Device 74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC245A	Octal 3–State Noninverting Bus Transceiver	LS245		LS	20
HCT245A	Octal 3–State Noninverting Bus Transceiver with LSTTL–Compatible Inputs	LS245		LS	20

HC Devices Have CMOS–Compatible Inputs. HCT Devices Have LSTTL–Compatible Inputs.

Device	HC HCT 245A
# Pins	20
Quad Device	
Octal Device	●
Buffer	●
Storage Capability	
Inverting Outputs	
Noninverting Outputs	●
Common Output Enable	●
Active–Low Output Enable	●
Active–High Output Enable	
Direction Control	●

LATCHES

Device Number MC74	Function	Functional Equivalent LSTTL Device 74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC373A HCT373A	Octal 3–State Noninverting Transparent Latch Octal 3–State Noninverting Transparent Latch with LSTTL–Compatible Inputs	LS373 LS373		LS373 LS373	20 20
HC573A HCT573A	Octal 3–State Noninverting Transparent Latch Octal 3–State Noninverting Transparent Latch with LSTTL–Compatible Inputs	LS373 LS373		LS573 LS573	20 20

HC Devices Have CMOS–Compatible Inputs. HCT Devices Have LSTTL–Compatible Inputs.

Device	HC HCT 373A	HC HCT 573A
# Pins	20	20
Single Device Dual Device Octal Device	 ●	 ●
Number of Bits Controlled by Latch Enable: 2 8	 ●	 ●
Transparent Addressable Readback Capability	●	●
Noninverting Outputs Inverting Outputs	●	●
Common Latch Enable, Active–Low	●	●
3–State Outputs Common Output Enable, Active–Low	● ●	● ●

These devices are identical in function and are different in pinout only: HC/HCT373A and HC/HCT573A

FLIP–FLOPS

Device Number MC74	Function	Functional Equivalent LSTTL Device 74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC74A	Dual D Flip–Flop with Set and Reset	LS74,LS74A	*4013	LS	14
HCT74A	Dual D Flip–Flop with Set and Reset with LSTTL–Compatible Inputs	LS74,LS74A	4013	LS	14
HC174A	Hex D Flip–Flop with Common Clock and Reset	LS174	4174	LS/CMOS	16
HC175A	Quad D Flip–Flop with Common Clock and Reset	LS175	4175	LS/CMOS	16
HC273A	Octal D Flip–Flop with Common Clock and Reset	LS273		LS	20
HCT273A	Octal D Flip–Flop with Common Clock and Reset with LSTTL–Compatible Inputs	LS273		LS	20
HC374A	Octal 3–State Noninverting D Flip–Flop	LS374		LS374	20
HCT374A	Octal 3–State Noninverting D Flip–Flop with LSTTL–Compatible Inputs	LS374		LS374	20
HC574A	Octal 3–State Noninverting D Flip–Flop	LS374			20
HCT574A	Octal 3–State Noninverting D Flip–Flop with LSTTL–Compatible Inputs	LS374			20

*Suggested alternative

HC Devices Have CMOS–Compatible Inputs. HCT Devices Have LSTTL–Compatible Inputs.

Device	HC HCT 74A	HC 174A	HC 175/A
# Pins	14	16	16
Type	D	D	D
Dual Device	●		
Quad Device			●
Hex Device		●	
Octal Device			
Common Clock		●	●
Negative–Transition Clocking			
Positive–Transition Clocking	●	●	●
Common, Active–Low Data Enables			
Noninverting Outputs	●	●	●
Inverting Outputs	●		●
3–State Outputs			
Common, Active–Low Output Enables			
Common Reset		●	●
Active–Low Reset	●	●	●
Active–High Reset			
Active–Low Set	●		
Transceiver			
Direction Control			

FLIP–FLOPS (Continued)

HC Devices Have CMOS–Compatible Inputs. HCT Devices Have LSTTL–Compatible Inputs.

Device	HC HCT 273A	HC HCT 374A	HC HCT 574A
# Pins	20	20	20
Type	D	D	D
Dual Device Quad Device Hex Device Octal Device	 ●	 ●	 ●
Common Clock Negative–Transition Clocking Positive–Transition Clocking	● ●	● ●	● ●
Common, Active–Low Data Enables			
Noninverting Outputs Inverting Outputs	●	●	●
3–State Outputs Common, Active–Low Output Enables		● ●	● ●
Common Reset Active–Low Reset Active–High Reset	● ●		
Active–Low Set			
Transceiver Direction Control			

These devices are identical in function and are different in pinout only: HC374A and HC574A

DIGITAL DATA SELECTORS/MULTIPLEXERS

Device Number MC74	Function	Functional Equivalent LSTTL Device 74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC157A	Quad 2–Input Noninverting Data Selector/Multiplexer	LS157		LS	16
HC251	8–Input Data Selector/Multiplexer with 3–State Outputs	LS251	*4512	LS	16
HC253	Dual 4–Input Data Selector/Multiplexer with 3–State Outputs	LS253		LS	16
HC257	Quad 2–Input Data Selector/Multiplexer with 3–State Outputs	LS257B		LS	16

*Suggested alternative

HC Devices Have CMOS–Compatible Inputs.

Device	HC 157A
# Pins	16
Description	One of two 4–bit words is selected
Single Device Dual Device Quad Device	 ●
Data Latch with Active–Low Latch Enable	
Common Address 1–Bit Binary Address 2–Bit Binary Address 3–Bit Binary Address	● ●
Address Latch (Transparent) Address Latch (Non–transparent) Active–Low Address Latch Enable	
Noninverting Output Inverting Output	●
3–State Outputs	
Common Output Enable Active–High Output Enable Active–Low Output Enable	● ●

DECODERS/DEMULTIPLEXERS/DISPLAY DRIVERS

Device Number MC74	Function	Functional Equivalent LSTTL Device 74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC138A	1–of–8 Decoder/Demultiplexer	LS138	*4028	LS	16
HCT138A	1–of–8 Decoder/Demultiplexer with LSTTL–Compatible Inputs	LS138	*4028	LS	16
HC139A	Dual 1–of–4 Decoder/Demultiplexer	LS139	4556	LS/CMOS	16

*Suggested alternative

HC Devices Have CMOS–Compatible Inputs.

Device	HC HCT 138A	HC 139A
# Pins	16	16
Input Description	3–Bit Binary Address	2–Bit Binary Address
Output Description	One of 8	One of 4
Single Device Dual Device	●	●
Address Input Latch Active–High Latch Enable Active–Low Latch Enable		
Active–Low Inputs		
Active–Low Outputs Active–High Outputs	●	●
Active–Low Output Enable Active–High Output Enable	●● ●	●
Active–Low Reset		
Active–Low Blanking Input Active–High Blanking Input		
Active–Low Lamp–Test Input		
Phase Input (for LCD's)		

●● Implies the device has two such enables

ANALOG SWITCHES/MULTIPLEXERS/DEMULTIPLEXERS

Device Number MC74	Function	Functional Equivalent LSTTL Device 74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC4051A	8–Channel Analog Multiplexer/Demultiplexer		4051	CMOS	16
HC4052A	Dual 4–Channel Analog Multiplexer/Demultiplexer		4052	CMOS	16
HC4053A	Triple 2–Channel Analog Multiplexer/Demultiplexer		4053	CMOS	16
HC4066A	Quad Analog Switch/Multiplexer/Demultiplexer		4066,4016	CMOS	14
⋆HC4316/A	Quad Analog Switch/Multiplexer/Demultiplexer with Separate Analog and Digital Power Supplies		*4016		16
⋆HC4851A	Analog Multiplexer/Demultiplexer with Injection Current Effect Control		*4051		20
⋆HC4852A	Analog Multiplexer/Demultiplexer with Injection Current Effect Control		*4052		20

*Suggested alternative
⋆ High–Speed CMOS design only

HC Devices Have CMOS–Compatible Inputs.

Device	HC 4051A	HC 4052A	HC 4053A	HC 4066A
# Pins	16	16	16	14
Description	A 3–Bit Address Selects One of 8 Switches	A 2–Bit Address Selects One of 4 Switches	A 3–Bit Address Selects Varying Combinations of the 6 Switches	4 Independently Controlled Switches
Single Device	●			
Dual Device		●		
Triple Device			●	
Quad Device				●
1–to–1 Multiplexing				●
2–to–1 Multiplexing			●	
4–to–1 Multiplexing		●		
8–to–1 Multiplexing	●			
Active–High ON/OFF Control				●
Common Address Inputs		●	●	
2–Bit Binary Address		●		
3–Bit Binary Address	●		●	
Address Latch with Active–Low Latch Enable				
Common Switch Enable	●	●	●	
Active–Low Enable	●	●	●	
Active–High Enable				
Separate Analog and Control Reference Power Supplies	●	●	●	
Switched Tubs (for R_{ON} and Prop. Delay Improvement)				●

ANALOG SWITCHES/MULTIPLEXERS/DEMULTIPLEXERS (Continued)

HC Devices Have CMOS–Compatible Inputs.

Device	HC 4316A	HC 4851A	HC 4852A
# Pins	16	20	20
Description	4 Independently Controlled Switches (Has a Separate Analog Lower Power Supply)	A 3–Bit Address Selects One of 8 Switches (Has Injection Current Protection)	A 3–Bit Address Selects Varying Combinations of the 6 Switches (Has Injection Current Protection)
Single Device Dual Device Triple Device Quad Device	 ●	● 	 ●
1–to–1 Multiplexing 2–to–1 Multiplexing 4–to–1 Multiplexing 8–to–1 Multiplexing	● 	 ●	 ●
Active–High ON/OFF Control	●		
Common Address Inputs 2–Bit Binary Address 3–Bit Binary Address	 	 ●	● ● ●
Common Switch Enable Active–Low Enable Active–High Enable	● ●	● ●	● ●
Separate Analog and Control Reference Power Supplies	●	●	●
Switched Tubs (for R_{ON} and Prop. Delay Improvement)			
njection Current Protection		●	●

SHIFT REGISTERS

Device Number MC74	Function	Functional Equivalent LSTTL Device 74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC164A	8–Bit Serial–Input/Parallel–Output Shift Register	LS164		LS	14
HC165A	8–Bit Serial– or Parallel–Input/Serial–Output Shift Register	LS165	*4021	LS	16
HC589A	8–Bit Serial– or Parallel–Input/Serial–Output Shift Register with 3–State Output				16
HC595A	8–Bit Serial–Input/Serial– or Parallel–Output Shift Register with Latched 3–State Outputs				16

*Suggested alternative

HC Devices Have CMOS–Compatible Inputs.

Device	HC 164A	HC 165A	HC 589A	HC 595A
# Pins	14	16	16	16
4–Bit Register				
8–Bit Register	●	●	●	●
Serial Data Input	●	●	●	●
Parallel Data Inputs		●	●	
Serial Output Only		●	●	
Parallel Outputs	●			●
Inverting Output		●		
Noninverting Output	●	●	●	●
Serial Shift/Parallel Load Control		●	●	
Shifts One Direction Only	●	●	●	●
Shifts Both Directions				
Positive–Transition Clocking	●	●	●	●
Active–High Clock Enable		●		
Input Data Enable	●			
Data Latch with Active–High Latch Clock			●	
Output Latch with Active–High Latch Clock				●
3–State Outputs			●	●
Active–Low Output Enable			●	●
Active–Low Reset	●			●

COUNTERS

Device Number MC74	Function	Functional Equivalent LSTTL Device 74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC161A	Presettable 4–Bit Binary Counter with Asynchronous Reset	LS161,LS161A		LS	16
HC163A	Presettable 4–Bit Binary Counter with Synchronous Reset	LS161,LS161A		LS	16
HC390A	Dual 4–Stage Binary Ripple Counter with ÷ 2 and ÷ 5 Sections				16
HC393A	Dual 4–Stage Binary Ripple Counter	LS393	*4520	LS	14
HC4020A	14–Stage Binary Ripple Counter		4020	CMOS	16
HC4040A	12–Stage Binary Ripple Counter		4040	CMOS	16
HC4060A	14–Stage Binary Ripple Counter with Oscillator		4060	CMOS	16

*Suggested alternative

HC Devices Have CMOS–Compatible Inputs.

Device	HC 161A	HC 163A	HC 390A	HC 393A	HC 4020A	HC 4040A	HC 4060A
# Pins	16	16	16	14	16	16	16
Single Device	●	●			●	●	●
Dual Device			●	●			
Ripple Counter			●	●	●	●	●
Number of Ripple Counter Internal Stages			4	4	14	12	14
Number of Stages with Available Outputs			4	4	12	12	10
Count Up	●	●	●	●	●	●	●
4–Bit Binary Counter	●	●		●			
BCD Counter			●				
Decimal Counter							
Separate ÷ 2 Section			●				
Separate ÷ 5 Section			●				
On–Chip Oscillator Capability							●
Positive–Transition Clocking	●	●					
Negative–Transition Clocking			●	●	●	●	●
Active–High Clock Enable							
Active–Low Clock Enable							
Active–High Count Enable	●●	●●					
Active–High Reset	●	●	●	●	●	●	●
4–Bit Binary Preset Data Inputs	●	●					
BCD Preset Data Inputs							
Active–Low Load Preset	●	●					
Carry Output	●	●					

●● implies the device has two such enables

MISCELLANEOUS DEVICES

Device Number MC74	Function	Functional Equivalent LSTTL Device 74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC4046A	Phase–Locked Loop		4046	CMOS	16
HC4538A	Dual Precision Monostable Multivibrator (Retriggerable, Resettable)		4538,4528	CMOS	16

CHAPTER 2
Design Considerations

INTRODUCTION

CMOS devices have been used for many years in applications where the primary concerns were low power consumption, wide power–supply range, and high noise immunity. However, metal–gate CMOS (MC14000 series) is too slow for many applications. Applications requiring high–speed devices, such as microprocessor memory decoding, had to go to the faster families such as LSTTL. This meant sacrificing the best qualities of CMOS. The next step in the logic evolution was to introduce a family of devices that were fast enough for such applications, while retaining the advantages of CMOS. The results of this change can be seen in 1 where HSCMOS devices are compared to standard (metal–gate) CMOS, LSTTL, and ALS.

The ON Semiconductor CMOS evolutionary process shown in Figure 1 indicates that one advantage of the silicon–gate process is device size. The High–Speed CMOS (HSCMOS) device is about half the size of the metal–gate predecessor, yielding significant chip area savings. The silicon–gate process allows smaller gate or channel lengths due to the self–aligning gate feature. This process uses the gate to define the channel during processing, eliminating registration errors and, therefore, the need for gate overlaps. The elimination of the gate overlap significantly lowers the gate capacitance, resulting in higher speed capability. The smaller gate length also results in higher drive capability per unit gate width, ensuring more efficient use of chip area. Immunity enhancements to electrostatic discharge (ESD) damage and latch up are ongoing. Precautions should still be taken, however, to guard against electrostatic discharge and latch up.

ON Semiconductors's High–Speed CMOS family has a broad range of functions from basic gates, flip–flops, and counters to bus–compatible devices. The family is made up of devices that are identical in pinout and are functionally equivalent to LSTTL devices, as well as the most popular metal–gate devices not available in TTL. Thus, the designer has an excellent alternative to existing families without having to become familiar with a new set of device numbers.

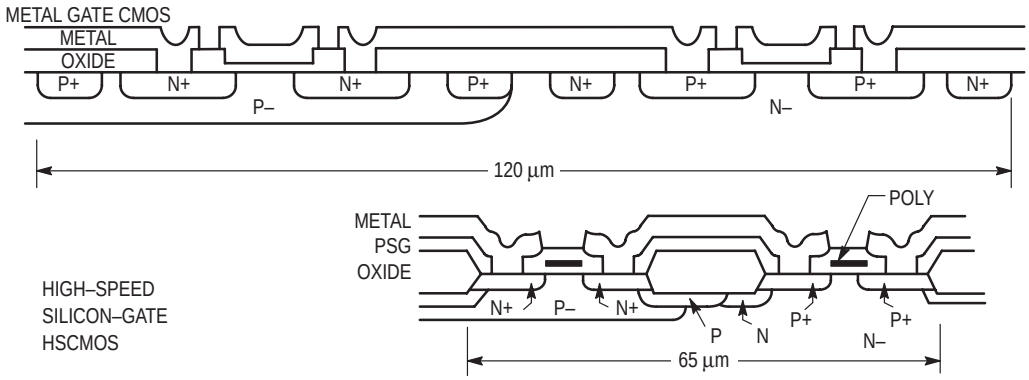


Figure 1. CMOS Evolution

HANDLING PRECAUTIONS

High–Speed CMOS devices, like all MOS devices, have an insulated gate that is subject to voltage breakdown. The gate oxide for HSCMOS devices breaks down at a gate–source potential of about 100 volts. Some device inputs are protected by a resistor–diode network (Figure 2). New input protection structure deletes the poly resistor (Figure 3) Using the test setup shown in Figure 4, the inputs typically withstand a > 2 kV discharge.

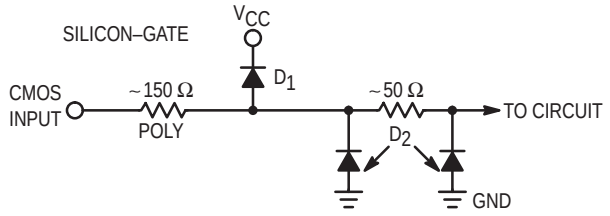


Figure 2. Input Protection Network

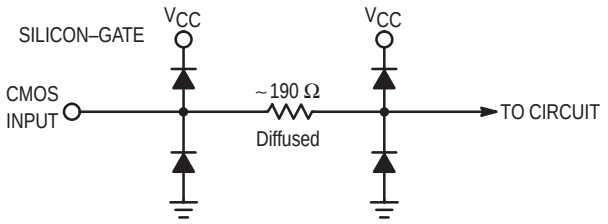


Figure 3. New Input Protection Network

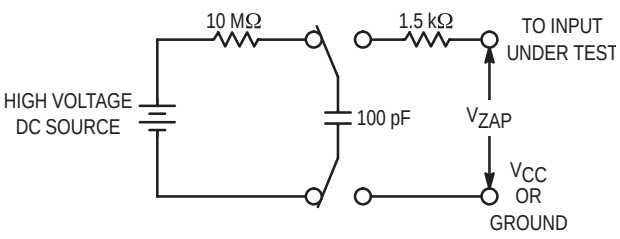


Figure 4. Electrostatic Discharge Test Circuit

Table 1. Logic Family Comparisons

General Characteristics (1) (All Maximum Ratings)

Characteristic	Symbol	TTL		CMOS		Unit
		LS	ALS	MC14000	Hi–Speed	
Operating Voltage Range	$V_{CC/EE/DD}$	5 ± 5%	5 ± 5%	3.0 to 18	2.0 to 6.0	V
Operating Temperature Range	T_A	0 to + 70	0 to + 70	– 40 to + 85	– 55 to + 125	°C
Input Voltage (limits)	V_{IH} min	2.0	2.0	3.5[4]	3.5[4]	V
	V_{IL} max	0.8	0.8	1.5[4]	1.0[4]	V
Output Voltage (limits)	V_{OH} min	2.7	2.7	V_{DD} – 0.05	V_{CC} – 0.1	V
	V_{OL} max	0.5	0.5	0.05	0.1	V
Input Current	I_{INH}	20	20	± 0.3	± 1.0	µA
	I_{INL}	– 400	– 200			
Output Current @ V_O (limit) unless otherwise specified	I_{OH}	– 0.4	– 0.4	– 2.1 @ 2.5 V	– 4.0 @ V_{CC} – 0.8 V	mA
	I_{OL}	8.0	8.0	0.44 @ 0.4 V	4.0 @ 0.4 V	mA
DC Noise Margin Low/High	DCM	0.3/0.7	0.3/0.7	1.45[4]	0.90/1.35[4]	V
DC Fanout	—	20	20	50(1)[2]	50(10)[2]	—

Speed/Power Characteristics (1) (All Typical Ratings)

Characteristic	Symbol	TTL		CMOS		Unit
		LS	ALS	MC14000	Hi–Speed	
Quiescent Supply Current/Gate	I_G	0.4	0.2	0.0001	0.0005	mA
Power/Gate (Quiescent)	P_G	2.0	1.0	0.0006	0.001	mW
Propagation Delay	t_p	9.0	7.0	125	8.0	ns
Speed Power Product	—	18	7.0	0.075	0.01	pJ
Clock Frequency (D–F/F)	f_{max}	33	35	4.0	40	MHz
Clock Frequency (Counter)	f_{max}	40	45	5.0	40	MHz

Propagation Delay (1)

Characteristic		TTL		CMOS		Unit
		LS	ALS	MC14000	Hi–Speed	
Gate, NOR or NAND:	**Product No.**	SN74LS00	SN74ALS00	MC14001B	74HC00	—
t_{PLH}/t_{PHL}[5]	Typical	(10)[3]	(5)[3]	25	(8)[3] 10	ns
	Maximum	(15)[3]	10	250	(15)[3] 20	
Flip–Flop, D–type:	**Product No.**	SN74LS74	SN74ALS74	MC14013B	74HC74	—
t_{PLH}/t_{PHL}[5] (Clock to Q)	Typical	(25)[3]	(12)[3]	175	(23)[2] 25	ns
	Maximum	(40)[3]	20	350	(30)[3] 32	
Counter:	**Product No.**	SN74LS163	SN74ALS163	MC14163B	74HC163	—
t_{PLH}/t_{PHL}[5] (Clock to Q)	Typical	(18)[3]	(10)[3]	350	(20)[3] 22	ns
	Maximum	(27)[3]	24	700	(27)[3] 29	

NOTES:

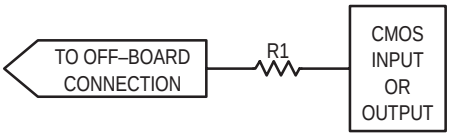
1. Specifications are shown for the following conditions:
   a) V_{DD} (CMOS) = 5.0 V ± 10% for dc tests, 5.0 V for ac tests; V_{CC} (TTL) = 5.0 V ± 5% for dc tests, 5.0 V for ac tests
   b) Basic Gates: LS00 or equivalent
   c) T_A = 25°C
   d) C_L = 50 pF (ALS, HC), 15 pF (LS, 14000 and Hi–Speed)
   e) Commercial grade product
2. ( ) fanout to LSTTL
3. ( ) C_L = 15 pF
4. DC input voltage specifications are proportional to supply voltage over operating range.
5. The number specified is the larger of t_{PLH} and t_{PHL} for each device.

The input protection network consists of large ESD protection diodes, a diffused resistor, and two small “dummy” transistors. Outputs have a similar ESD protection network except for the series resistor. Although the on–chip protection circuitry guards against ESD damage, additional protection may be necessary once the chip is placed in circuit. Both an external series resistor and ground and V_{CC} diodes, similar to the input protection structure, are recommended if there is a potential of ESD, voltage transients, etc. Several monolithic diode arrays are available from ON Semiconductor, such as the MAD130 (dual 10 diode array) or the MAD1104 (dual 8 diode array). These diodes, in chip form, not only provide the necessary protection, but also save board space as opposed to using discrete diodes.

Static damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged pins are the easiest to detect. An ESD–damaged pin that has been completely destroyed may exhibit a low–impedance path to V_{CC} or GND. Another common failure mode is a fused or open circuit. The effect of both failure modes is that the device no longer properly responds to input signals. Less severe cases are more difficult to detect because they show up as intermittent failures or as degraded performance. Generally, another effect of static damage is increased chip leakage currents (I_{CC}).

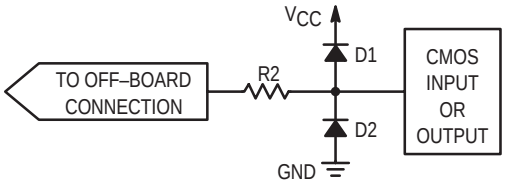
Although the input network does offer significant protection, these devices are not immune to large static voltage discharges that can be generated while handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4 to 15 kV range (depending on humidity, surface conditions, etc.). Therefore, the following precautions should be observed.

1. Wrist straps and equipment logs should be maintained and audited on a regular basis. Wrist straps malfunction and may go unnoticed. Also, equipment gets moved from time to time and grounds may not be reconnected properly.
2. Do not exceed the Maximum Ratings specified by the data sheet.
3. All unused device inputs should be connected to V_{CC} or GND.
4. All low impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the CMOS device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
5. Circuit boards containing CMOS devices are merely extensions of the devices, and the same handling precautions apply. Contacting edge connectors wired directly to device inputs can cause damage. Plastic wrapping should be avoided. When external connectors to a PC board are connected to an input or output of a CMOS device, a resistor should be used in series with the input or output. This resistor helps limit accidental damage if the PC board is removed and brought into contact with static generating materials. The limiting factor for the series resistor is the added delay. The delay is caused by the time constant formed by the series resistor and input capacitance. Note that the maximum input rise and fall times should not be exceeded. In Figure 5, two possible networks are shown using a series resistor to reduce ESD damage. For convenience, an equation is given for added propagation delay and rise time effects due to series resistance size.



Advantage: Requires minimal area

Disadvantage: R1 > R2 for the same level of protection; therefore, rise and fall times, propagation delays, and output drives are severely affected.



Advantage: R2 < R1 for the same level of protection. Impact on ac and dc characteristics is minimized.

Disadvantage: More board area, higher initial cost.

NOTE: These networks are useful for protecting the following:

A digital inputs and outputs
B analog inputs and outputs
C 3–state outputs
D bidirectional (I/O) ports

Propagation Delay and Rise Time vs. Series Resistance

$$R \approx \frac{t}{C \cdot k}$$

where:

R=the maximum allowable series resistance in ohms

t= the maximum tolerable propagation delay or rise time in seconds

C= the board capacitance plus the driven input capacitance in farads

k= 0.7 for propagation delay calculations

k= 2.3 for rise time calculations

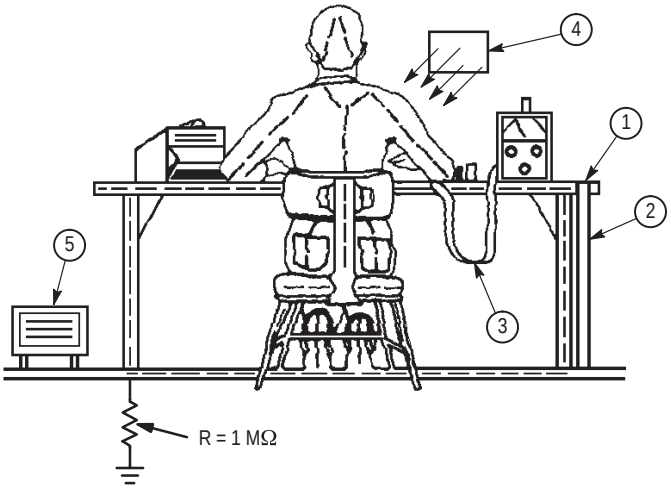
Figure 5. Networks for Minimizing ESD and Reducing CMOS Latch Up Susceptibility

6. All CMOS devices should be stored or transported in materials that are antistatic or conductive. CMOS devices must not be inserted into conventional plastic “snow”, Styrofoam, or plastic trays, but should be left in their original container until ready for use.
7. All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, because a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are essential and should be tested daily. See Figure 6 for an example of a typical work station.
8. Nylon or other static generating materials should not come in contact with CMOS devices.
9. If automatic handlers are being used, high levels of static electricity may be generated by the movement of the device, the belts, or the boards. Reduce static buildup by using ionized air blowers, anti–static sprays, and room humidifiers. All conductive parts of machines which come into contact with the top, bottom, or sides of IC packages must be grounded to earth ground.
10. Cold chambers using CO_2 for cooling should be equipped with baffles, and the CMOS devices must be contained on or in conductive material.
11. When lead straightening or hand soldering is necessary, provide ground straps for the apparatus used and be sure that soldering iron tips are grounded.
12. The following steps should be observed during wave solder operations:
    a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to earth ground.
    b. The loading and unloading work benches should have conductive tops grounded to earth ground.
    c. Operators must comply with precautions previously explained.
    d. Completed assemblies should be placed in antistatic or conductive containers prior to being moved to subsequent stations.
13. The following steps should be observed during board–cleaning operations:
    a. Vapor degreasers and baskets must be grounded to earth ground.
    b. Brush or spray cleaning should not be used.
    c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic or conductive container.
    d. Cleaned assemblies should be placed in antistatic or conductive containers immediately after removal from the cleaning basket.
    e. High velocity air movement or application of solvents and coatings should be employed only when a static eliminator using ionized air is directed at the printed circuit board.
14. The use of static detection meters for production line surveillance is highly recommended.
15. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
16. Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
17. Double check test equipment setup for proper polarity of V_{CC} and GND before conducting parametric or functional testing.
18. Do not recycle shipping rails. Repeated use causes deterioration of their antistatic coating. Exception: carbon rails (black color) may be recycled to some extent. This type of rail is conductive and antistatic.

RECOMMENDED READING

“Requirements for Handling Electrostatic–Discharge Sensitive (ESDS) Devices” EIA Standard EIA–625
Available by writing to:
Global Engineering Documents
15 Inverness Way East
Englewood, Colorado 80112
Or by calling:
1–800–854–7179 in the USA or CANADA or
(303) 397–7956 International

S. Cherniak, “A Review of Transients and Their Means of Suppression”, Application Note–843, ON Semiconductor Products Inc., 1982.



NOTES:
1. 1/16 inch conductive sheet stock covering bench-top worl area.
2. Ground strap.
3. Wrist strap In contact with skin.
4. Static neutralizer. (ionized air blower directed at work. Primarily for use in areas where direct grounding i impractical.
5. Room humidifier. Primarily for use in areas where th relative humidity is less than 45%. Caution: buildin heating and cooling systems usually dry the air causin the relative humidity inside a building to be less tha outside humidity.

Figure 6. Typical Manufacturing Work Station

POWER SUPPLY SIZING

CMOS devices have low power requirements and the ability to operate over a wide range of supply voltages. These two characteristics allow CMOS designs to be implemented using inexpensive power supplies without cooling fans. In addition, batteries may be used as either a primary power source or as a backup.

The maximum recommended power supply voltage for HC devices is 6.0 V and 5.5 V for HCT devices. Figure 7 offers some insight as to how this specification was derived. In the figure, V_S is the maximum power supply voltage and I_S is the sustaining current for the latch–up mode. The value of V_S was chosen so that the secondary breakdown effect may be avoided. The low–current junction avalanche region is between 10 and 14 volts at T_A = 25°C.

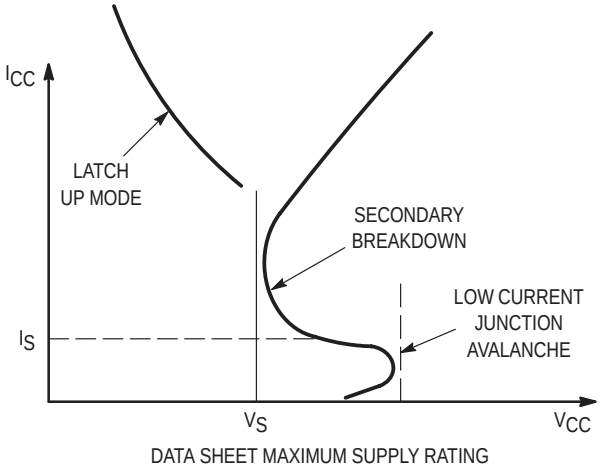


Figure 7. Secondary Breakdown Characteristics

In an ideal system design, the power supply should be designed to deliver only enough current to ensure proper operation of all devices. The obvious benefit of this type of design is cost savings.

BATTERY SYSTEMS

HSCMOS devices can be used with battery or battery backup systems. A few precautions should be taken when designing battery–operated systems.

1. The recommended power supply voltages should be observed. For battery backup systems such as the one in Figure 8, the battery voltage must be at least 2.7 volts (2 volts for the minimum power supply voltage and 0.7 volts to account for the voltage drop across the series diode).
2. Inputs that might go above the battery backup voltage should use the HC4049 or HC4050 buffers (Figure 8). If line power is interrupted, CMOS System A and Buffer A lose power. However, CMOS System B and Buffer B remain active due to the battery backup. Buffer A protects System A from System B by blocking active inputs while the circuit is not powered up. Also, if the power supply voltage drops below the battery voltage, Buffer A acts as a level translator for the outputs from System B. Buffer B acts to protect System B from any overvoltages which might exist. Both buffers may be replaced with current–limiting resistors, however power consumption is increased and propagation delays are lengthened.
3. Outputs that are subject to voltage levels above V_{CC} or below GND should be protected with a series resistor and/or clamping diodes to limit the current to an acceptable level.

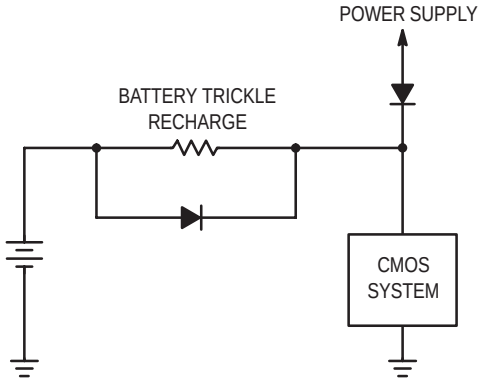


Figure 8. Battery Backup System

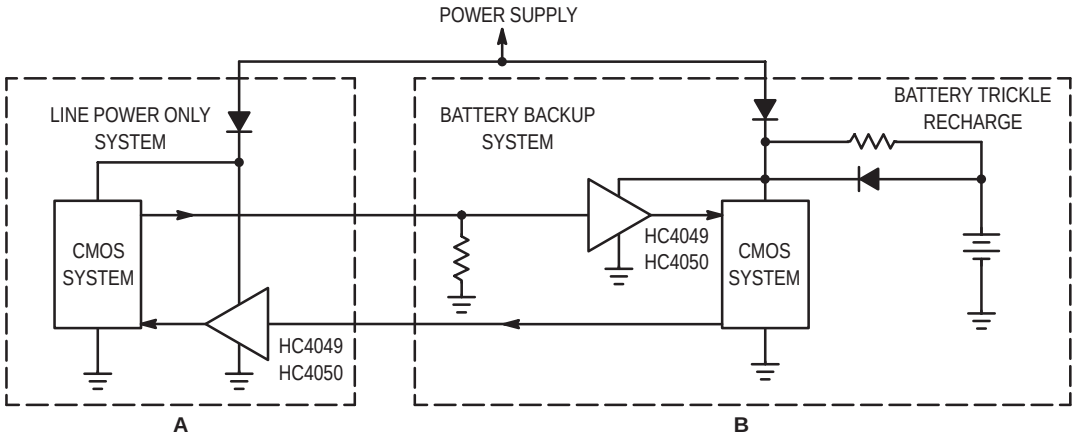


Figure 9. Battery Backup Interface

C_{PD} POWER CALCULATION

Power consumption for HSCMOS is dependent on the power–supply voltage, frequency of operation, internal capacitance, and load. The power consumption may be calculated for each package by summing the quiescent power consumption, $I_{CC} \bullet V_{CC}$, and the switching power required by each device within the package. For large systems, the most timely method is to bread–board the circuit and measure the current required under a variety of conditions.

The device dynamic power requirements can be calculated by the equation:

$$P_D = (C_L + C_{PD})\, V_{CC}{}^2 f$$

where: P_D = power dissipated in μW

C_L = total load capacitance present at the output in pF

C_{PD} = a measure of internal capacitances, called power dissipation capacitance, given in pF

V_{CC} = supply voltage in volts

f = frequency in MHz

If the devices are tested at a sufficiently high frequency, the dc supply current contributes a negligible amount to the overall power consumption and can therefore be ignored. For this reason, the power consumption is measured at 1 MHz and the following formula is used to determine the device's C_{PD} value:

$$C_{PD} = \frac{I_{CC}\ (\text{dynamic})}{V_{CC} \bullet f} - C_L$$

The resulting power dissipation is calculated using C_{PD} as follows under no–load conditions.

(HC) $P_D = C_{PD} V_{CC}{}^2 f + V_{CC} I_{CC}$

(HCT) $P_D = C_{PD} V_{CC}{}^2 f + V_{CC} I_{CC} + \Delta I_{CC} V_{CC} (\delta_1 + \delta_2 + \ldots + \delta_n)$

where the previously undefined variable, δ_n is the duty cycle of each input applied at TTL/NMOS levels.

The power dissipation for analog switches switching digital signals is the following:

(HC) $P_D = C_{PD} V_{CC}{}^2 f_{in} + (C_S + C_L) V_{CC}{}^2 f_{out} + V_{CC} I_{CC}$

where: C_S = digital switch capacitance, and

f_{out} = output frequency

In order to determine the C_{PD} of a single section of a device (i.e., one of four gates, or one of two flip–flops in a package), ON Semiconductor uses the following procedures as defined by JEDEC. Note: "biased" as used below means "tied to V_{CC} or GND."

Gates:	Switch one input while the remaining input(s) are biased so that the output(s) switch.
Latches:	Switch the enable and data inputs such that the latch toggles.
Flip–Flops:	Switch the clock pin while changing the data pin(s) such that the output(s) change with each clock cycle.
Decoders/ Demultiplexers:	Switch one address pin which changes two outputs.
Data Selectors/ Multiplexers:	Switch one address input with the corresponding data inputs at opposite logic levels so that the output switches.
Analog Switches:	Switch one address/select pin which changes two switches. The switch inputs/outputs should be left open. For digital applications where the switch inputs/outputs change between V_{CC} and GND, the respective switch capacitance should be added to the load capacitance.
Counters:	Switch the clock pin with the other inputs biased so that the device counts.
Shift Registers:	Switch the clock while alternating the input so that the device shifts alternating 1s and 0s through the register.
Transceivers:	Switch only one data input. Place transceivers in a single direction.
Monostables:	The pulse obtained with a resistor and no external capacitor is repeatedly switched.
Parity Generators:	Switch one input.
Encoders:	Switch the lowest priority output.
Display Drivers:	Switch one input so that approximately one–half of the outputs change state.
ALUs/Adders:	Switch the least significant bit. The remaining inputs are biased so that the device is alternately adding 0000 (binary) or 0001 (binary) to 1111 (binary).

On HSCMOS data sheets, C_{PD} is a typical value and is given either for the package or for the individual device (i.e., gates, flip–flops, etc.) within the package. An example of calculating the package power requirement is given using the 74HC00, as shown in Figure 10.

From the data sheet:

I_{CC} = 2 μA at room temperature (per package)

C_{PD} = 22 pF per gate

$$P_D = (C_{PD} + C_L)V_{CC}^2 f + V_{CC}I_{CC}$$

$$P_{D1} = (22\text{ pF} + 50\text{ pF})(5\text{ V})^2(1\text{ kHz})\ 1.8\ \mu W$$

$$P_{D2} = (22\text{ pF} + 50\text{ pF})(5\text{ V})^2(1\text{ MHz})\ 1800\ \mu W$$

$$P_{D3} = (22\text{ pF})\ (5\text{ V})^2(0\text{ Hz}) = 0\ \mu W$$

$$P_{D4} = (22\text{ pF})(5\text{ V})^2(0\text{ Hz}) = 0\ \mu W$$

$$P_D(\text{total}) = V_{CC}I_{CC} + PD1 + PD2 + PD3 + PD4$$

$$= 10\ \mu W + 1.8\ \mu W + 1800\ \mu W + 0\ \mu W$$

$$= 1812\ \mu W$$

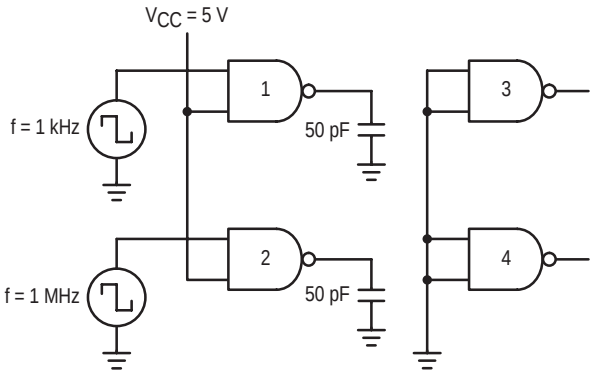


Figure 10. Power Consumption Calculation Example

As seen by this example, the power dissipated by CMOS devices is dependent on frequency. When operating at very high frequencies, HSCMOS devices can consume as much power as LSTTL devices, as shown in Figure 11. The power savings of HSCMOS is realized when used in a system where only a few of the devices are actually switching at the system frequency. The power consumption savings comes from the fact that for CMOS, only the devices that are switching consume significant power.

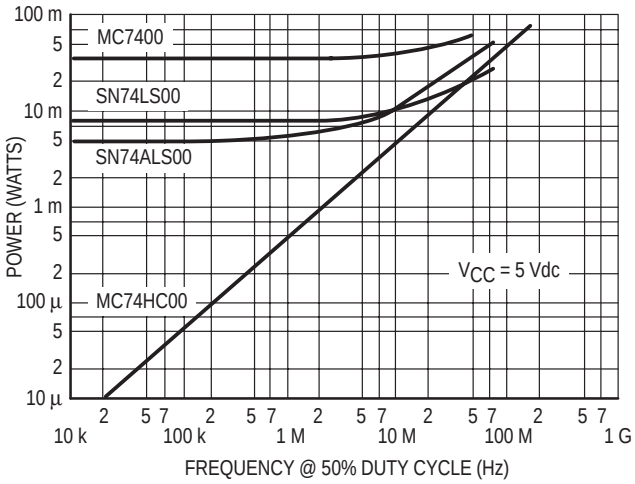


Figure 11. Power Consumption Vs. Input Frequency for TTL, LSTTL, ALs, and HSCMOS

INPUTS

A basic knowledge of input and output structures is essential to the HSCMOS designer. This section deals with the various input characteristics and application rules regarding their use. Output characteristics are discussed in the section titled **Outputs**.

All standard HC, HCU and HCT inputs, while in the recommended operating range ($GND \le V_{in} \le V_{CC}$), can be modeled as shown in Figure 12. For input voltages in this range, diodes D1 and D2 are modeled as resistors representing the high–impedance of reverse biased diodes. The maximum input current is 1 μA, worst case over temperature, when the inputs are at V_{CC} or GND, and V_{CC} = 6 V.

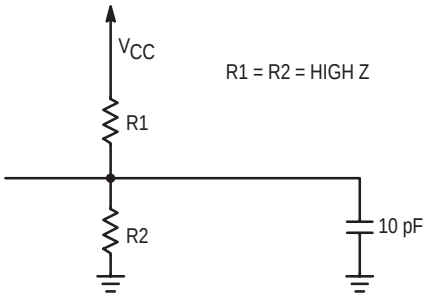


Figure 12. Input Model for $GND \le V_{in} \le V_{CC}$

When CMOS inputs are left open–circuited, the inputs may be biased at or near the typical CMOS switchpoint of 0.45 V_{CC} for HC devices or 1.3 V for HCT devices. At this switchpoint, both the P–channel and the N–channel transistors are conducting, causing excess current drain. Due to the high gain of the buffered devices (see Figure 13), the device can go into oscillation from any noise in the system, resulting in even higher current drain.

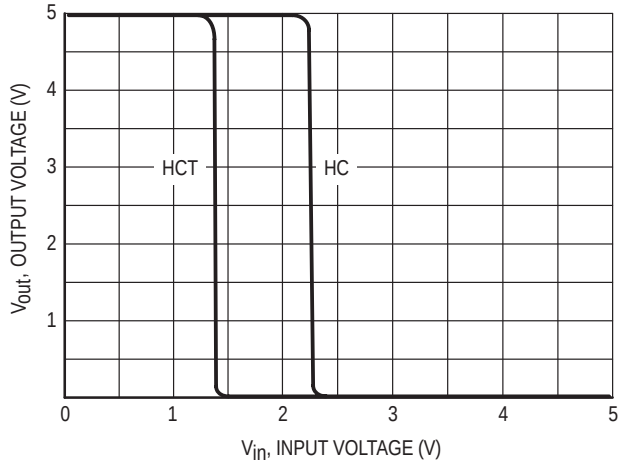


Figure 13. Typical Transfer Characteristics for Buffered Devices

For these reasons, all unused HC/HCT inputs should be connected either to V_{CC} or GND. For applications with inputs going to edge connectors, a 100 kΩ resistor to GND should be used, as well as a series resistor (R_S) for static protection and current limiting (see **Handling Precautions**, this chapter, for series resistor consideration). The resistors should be configured as in Figure 14.

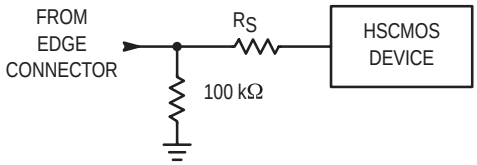


Figure 14. External Protection

For inputs outside of the recommended operating range, the CMOS input is modeled as in Figure 15 and Figure 16.

Current flows through diode D1 or D2 whenever the input voltage exceeds V_{CC} or drops below GND enough to forward bias either D1 or D2. The device inputs are guaranteed to withstand from GND – 0.5 V to V_{CC} + 0.5 V and a maximum current of 20 mA. If this maximum rating is exceeded, the device could go into a latch–up condition. (See **CMOS Latch Up**, this chapter.) Voltage should never be applied to any input or output pin before power has been applied to the device's power pins. Bias on input or output pins should be removed before removing the power. However, if the input current is limited to less than 20 mA, and this current only lasts for a brief period of time (< 100 ms), no damage to the device occurs.

Another specification that should be noted is the maximum input rise (t_r) and fall (t_f) times. Figure 17 shows the results of exceeding the maximum rise and fall times recommended by ON Semiconductor or contained in JEDEC Standard No. 7A. The reason for the oscillation on the output is that as the voltage passes through the switching threshold region with a slow rise time, any noise that is on the input line is amplified, and is passed through to the output. This oscillation may have a low enough frequency to cause succeeding stages to switch, giving unexpected results. If input rise or fall times are expected to exceed the maximum specified rise or fall times, Schmitt–triggered devices such as ON Semiconductor's HC14A and HC132A are recommended.

OUTPUTS

All HSCMOS outputs, with the exception of the HCU04A, are buffered to ensure consistent output voltage and current specifications across the family. All buffered outputs have guaranteed output voltages of V_{OL} = 0.1 V and $V_{OH} = V_{CC} - 0.1$ V for $|I_{out}| \le 20$ μA ($\le$ 20 HSCMOS loads).

The output drives for standard drive devices are such that 74HC/HCT devices can drive ten LSTTL loads and maintain a $V_{OL} \le 0.4$ V and $V_{OH} \ge V_{CC} - 0.8$ V across the full temperature range; bus–driver devices can drive fifteen LSTTL loads under the same conditions.

The outputs of all HSCMOS devices are limited to externally forced output voltages of $-0.5 \le V_{out} \le V_{CC}$ + 0.5 V. For externally forced voltages outside this range a

latch up condition could be triggered. (See **CMOS Latch Up**, this chapter.)

The maximum rated output current given on the individual data sheets is 25 mA for standard outputs and 35 mA for bus drivers. The output short circuit currents of these devices typically exceed these limits. The outputs can, however, be shorted for short periods of time for logic testing, if the maximum package power dissipation is not violated. (See individual data sheets for maximum power dissipation ratings.)

For applications that require driving high capacitive loads where fast propagation delays are needed (e.g., driving power MOSFETS), devices within the same package may be paralleled. Paralleling devices in different packages may result in devices switching at different points on the input voltage waveform, creating output short circuits and yielding undesirable output voltage waveforms.

As a design aid, output characteristic curves are given for both P–channel source and N–channel sink currents. The curves given include expected minimum curves for T_A = 25°C, 85°C, and 125°C, as well as typical values for T_A = 25°C. For temperatures < 25°C, use the 25°C curves. These curves, Figure 18 through Figure 29, are intended as design aids, not as guarantees. Unused output pins should be open–circuited (floating).

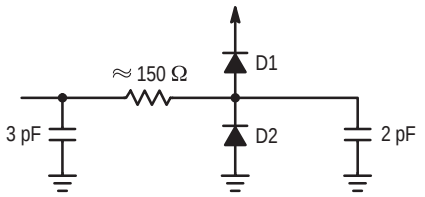


Figure 15. Input Model for $V_{in} > V_{CC}$ or $V_{in} < GND$

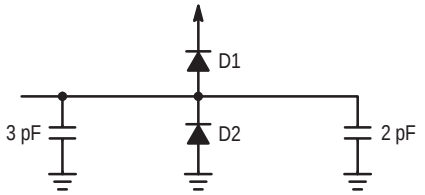


Figure 16. Input Model for New ESD Enhanced Circuits

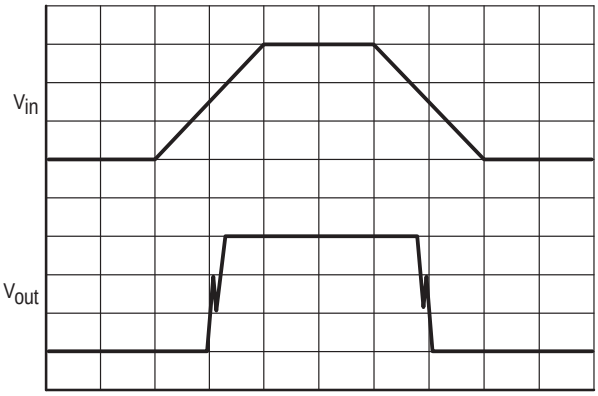


Figure 17. Maximum Rise Time Violation

STANDARD OUTPUT CHARACTERISTICS

N–CHANNEL SINK CURRENT

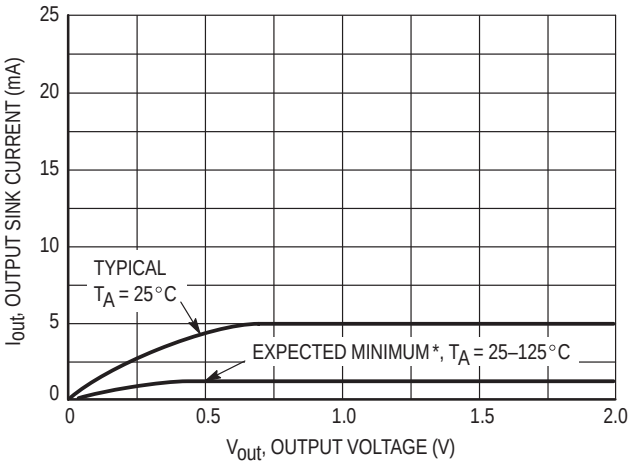


Figure 18. V_{GS} = 2.0 V

P–CHANNEL SOURCE CURRENT

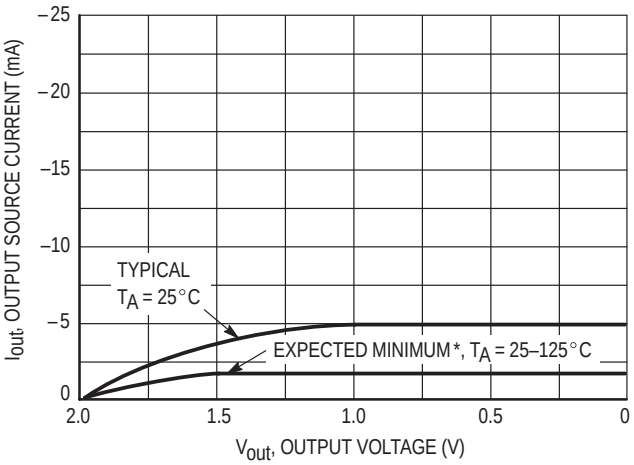


Figure 19. V_{GS} = – 2.0 V

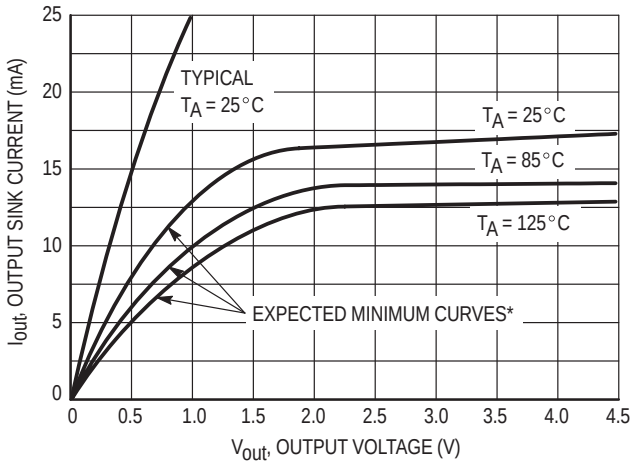


Figure 20. V_{GS} = 4.5 V

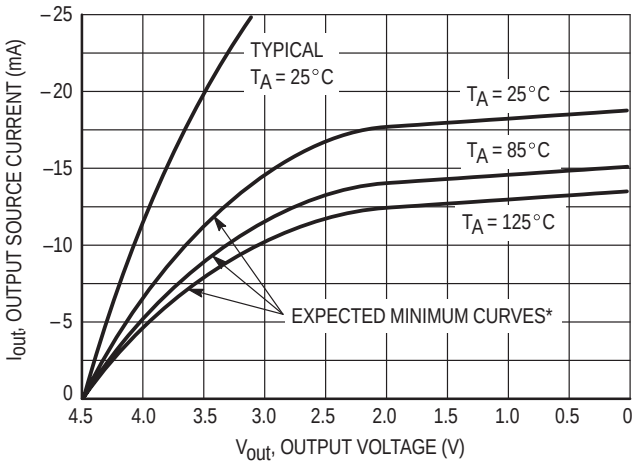


Figure 21. V_{GS} = – 4.5 V

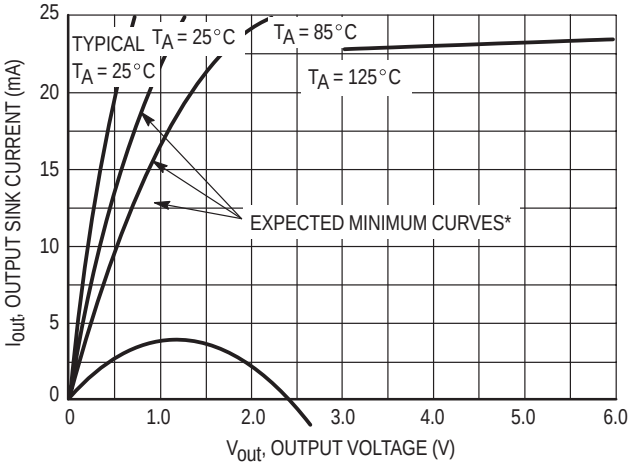


Figure 22. V_{GS} = 6.0 V

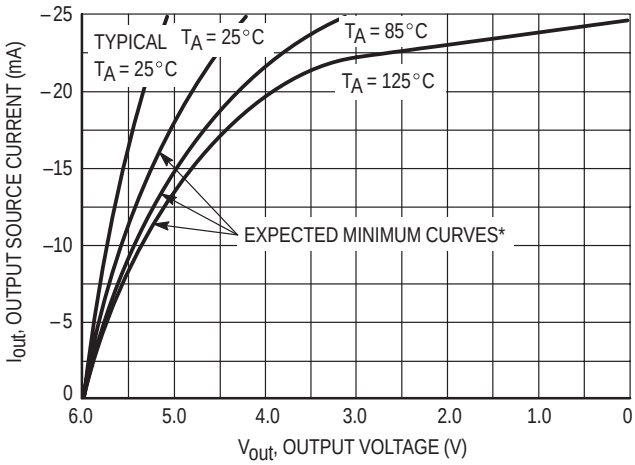


Figure 23. V_{GS} = – 6.0 V

*The expected minimum curves are not guarantees, but are design aids.

BUS–DRIVER OUTPUT CHARACTERISTICS

N–CHANNEL SINK CURRENT

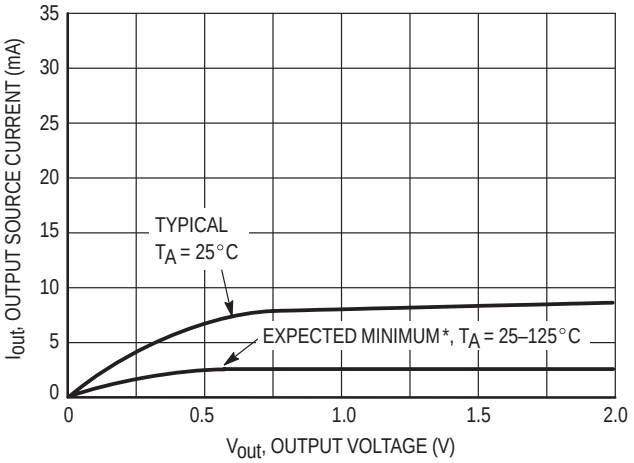


Figure 24. V_{GS} = 2.0 V

P–CHANNEL SOURCE CURRENT

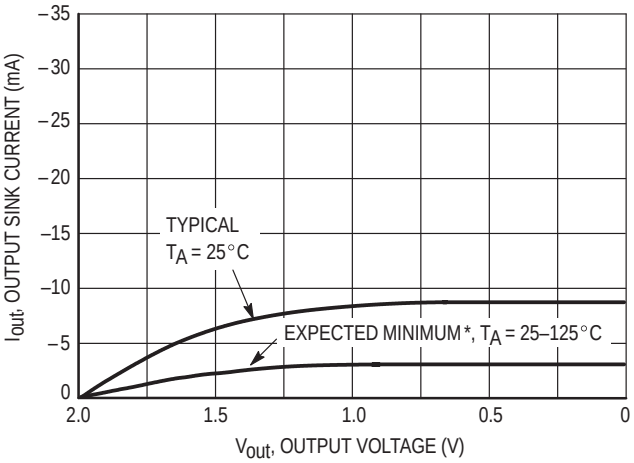


Figure 25. V_{GS} = – 2.0 V

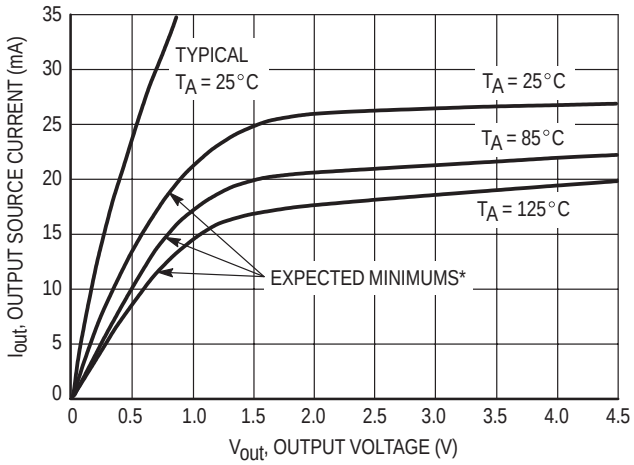


Figure 26. V_{GS} = 4.5 V

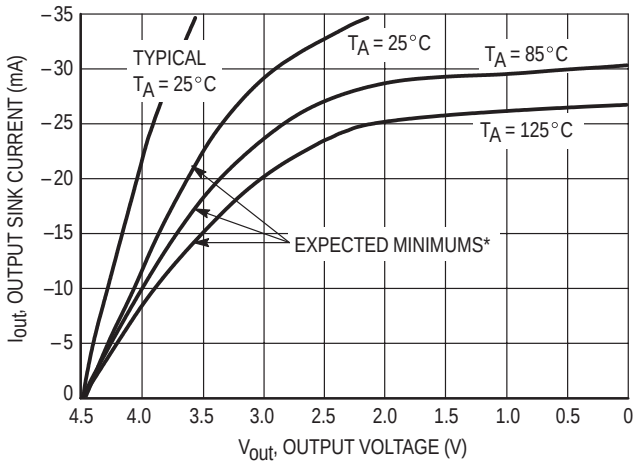


Figure 27. V_{GS} = – 4.5 V

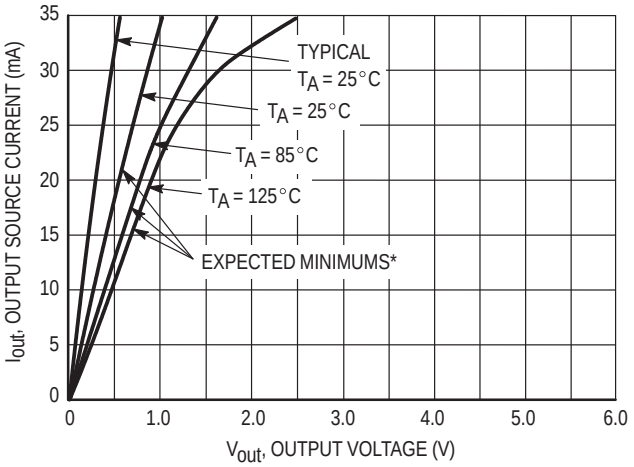


Figure 28. V_{GS} = 6.0 V

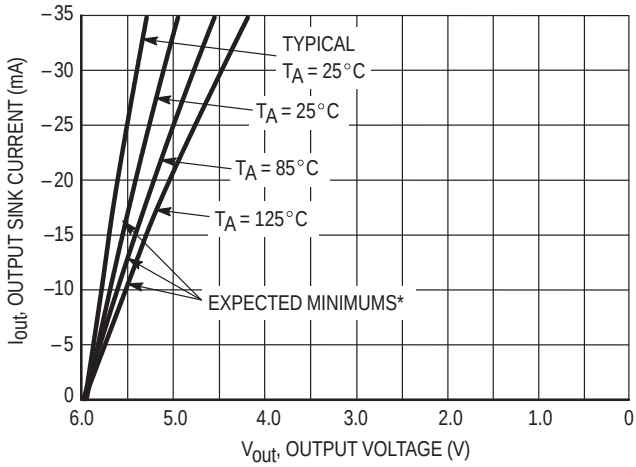


Figure 29. V_{GS} = – 6.0 V

*The expected minimum curves are not guarantees, but are design aids.

3–STATE OUTPUTS

Some HC/HCT devices have outputs that can be placed into a high–impedance state. These 3–state output devices are very useful for gang connecting to a common line or bus. When enabled, these output pins can be considered as ordinary output pins; as such, all specifications and precautions of standard output pins should be followed. When disabled (high–impedance state), these outputs can be modeled as in Figure 30. Output leakage current (10 μA worst case over temperature) as well as 3–state output capacitance must be considered in any bus design.

When power is interrupted to a 3–state device, the bus voltage is forced to between GND and V_{CC} + 0.7 V regardless of the previous output state.

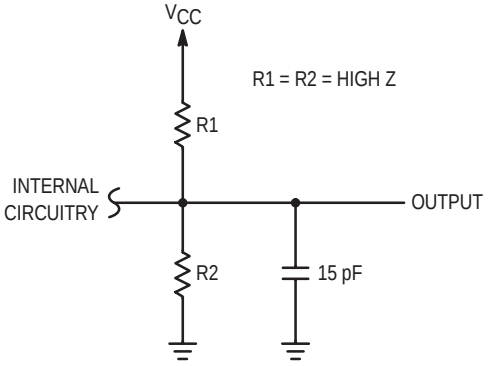


Figure 30. Model for Disabled Outputs

OPEN–DRAIN OUTPUTS

ON Semiconductor provides several devices that are designed only to sink current to GND. These open–drain output devices are fabricated using only an N–channel transistor and a diode to V_{CC} (Figure 31). The purpose of the diode is to provide ESD protection. Open–drain outputs can be modeled as shown in Figure 32.

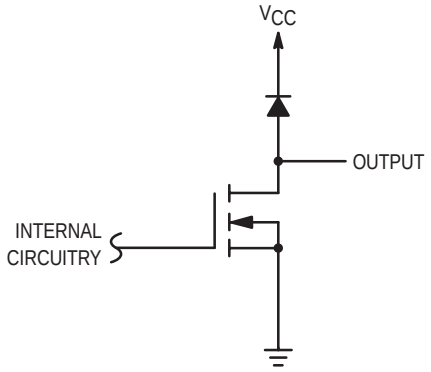


Figure 31. Open–Drain Output

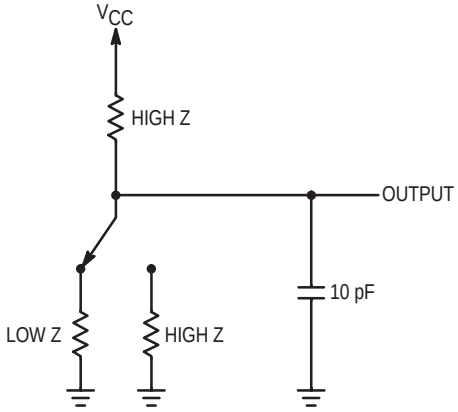


Figure 32. Model of Open–Drain Output

INPUT/OUTPUT PINS

Some HC/HCT devices contain pins that serve both as inputs and outputs of digital logic. These pins are referred to as digital I/O pins. The logic level applied to a control pin determines whether these I/O pins are selected as inputs or outputs.

When I/O pins are selected as outputs, these pins may be considered as standard CMOS outputs. When selected as inputs, except for an increase in input leakage current and input capacitance, these pins should be considered as standard CMOS inputs. These increases come from the fact that a digital I/O pin is actually a combination of an input and a 3–state output tied together (see Figure 33).

As stated earlier, all HC/HCT inputs must be connected to an appropriate logic level. This could pose a problem if an I/O pin is selected as an input while connected to an improperly terminated bus.

ON Semiconductor recommends terminating HC/HCT–type buses with resistors to V_{CC} or GND of between 1 kΩ to 1 MΩ in value. The choice of resistor value is a trade–off between speed and power consumption (see **Bus Termination**, this chapter).

Some ON Semiconductor devices have analog I/O pins. These analog I/O pins should not be confused with digital I/O pins. Analog I/O pins may be modeled as in Figure 34. These devices can be used to pass analog signals, as well as digital signals, in the same manner as mechanical switches.

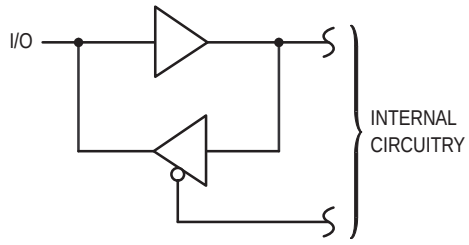


Figure 33. Typical Digital I/O Pin

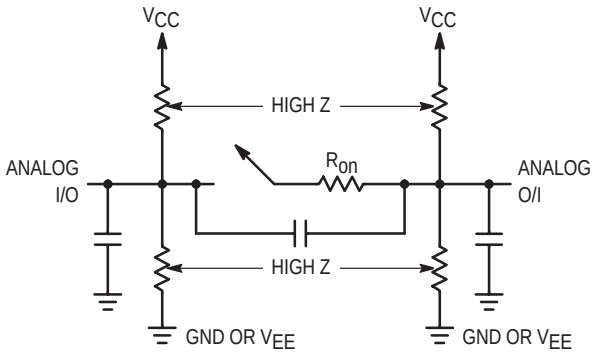


Figure 34. Analog I/O Pin

BUS TERMINATION

Because buses tend to operate in harsh, noisy environments, most bus lines are terminated via a resistor to V_{CC} or ground. This low impedance to V_{CC} or ground (depending on preference of a pull–up or pull–down logic level) reduces bus noise pickup. In certain cases a bus line may be released (put in a high–impedance state) by disabling all the 3–state bus drivers (see Figure 35). In this condition all HC/HCT inputs on the bus would be allowed to float. A CMOS input or 1/0 pin (when selected as an input) should never be allowed to float. (This is one reason why an HCT device may not be a drop–in replacement of an LSTTL device.) A floating CMOS input can put the device into the linear region of operation. In this region excessive current can flow and the possibility of logic errors due to oscillation may occur (see **Inputs**, this chapter). Note that when a bus is properly terminated with pull–up resistors, HC devices, instead of HCT devices, can be driven by an NMOS or LSTTL bus driver. HC devices are preferred over HCT devices in bus applications because of their higher low level input noise margin. (With a 5 V supply the typical HC switch point is 2.3 V while the switch point of HCT is only 1.3 V.)

Some popular LSTTL bus termination designs may not work for HSCMOS devices. The outputs of HSCMOS may not be able to drive the low value of termination used by some buses. (This is another reason why an HCT device may not be a drop in replacement for an LSTTL device.) However, because low power operation is one of the main reasons for using CMOS, an optimized CMOS bus termination is usually advantageous.

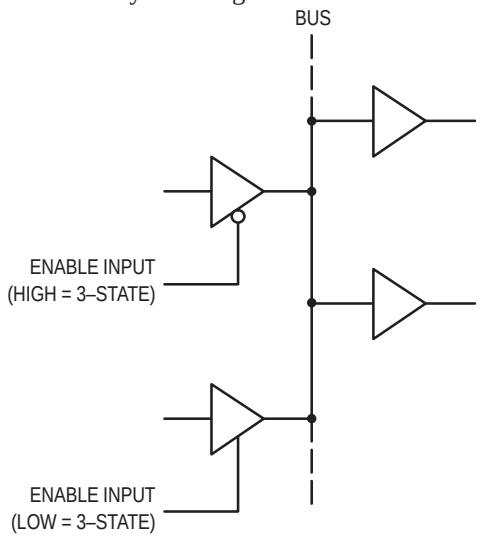


Figure 35. Typical Bus Line with 3–State Bus Drivers

The choice of termination resistances is a trade–off between speed and power consumption. The speed of the bus is a function of the RC time constant of the termination resistor and the parasitic capacitance associated with the bus. Power consumption is a function of whether a pull–up or pull–down resistor is used and the output state of the device that has control of the bus (see Figure 36). The lower the termination resistor the faster the bus operates, but more power is consumed. A large value resistor wastes less power, but slows the bus down. ON Semiconductor recommends a termination resistor value between 1 kΩ and 1 MΩ. An alternative to a passive resistor termination would be an active–type termination (see Figure 37). This type termination holds the last logic level on the bus until a driver can once again take control of the bus. An active termination has the advantage of consuming a minimal amount of power. Most HC/HCT bus drivers do not have built–in hysteresis. Therefore, heavily loaded buses can slow down rise and fall signals and exceed the input rise/fall time defined in JEDEC Standard No. 7A. In this event, devices with Schmitt–triggered inputs should be used to condition these slow signals.

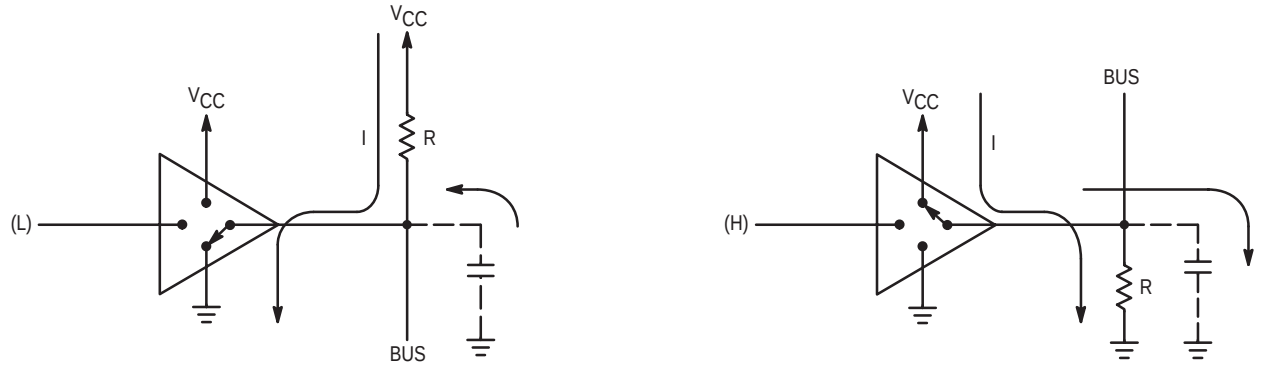


Figure 36.

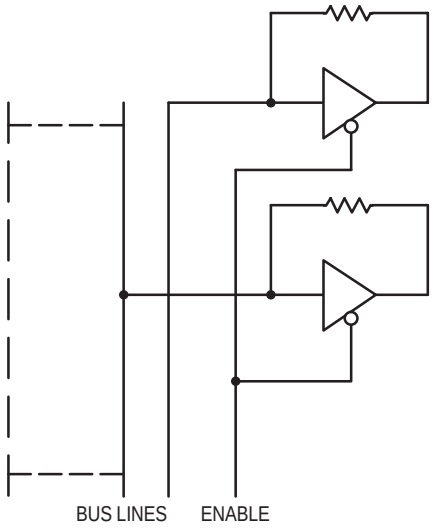


Figure 37. Using Active Termination (HC125)

TRANSMISSION LINE TERMINATION

When data is transmitted over long distances, the line on which the data travels can be considered a transmission line. (Long distance is relative to the data rate being transmitted.) Examples of transmission lines include high–speed buses, long PCB lines, coaxial and ribbon cables. All transmission lines should be properly terminated into a low–impedance termination. A low–impedance termination helps eliminate noise, ringing, overshoot, and crosstalk problems. Also a low–impedance termination reduces signal degradation because the small values of parasitic line capacitance and inductance have lesser effect on a low–impedance line.

The value of the termination resistor becomes a trade–off between power consumption, data rate speeds, and transmission line distance. The lower the resistor value, the faster data can be presented to the receiving device, but the more power the resistor consumes. The higher the resistor value, the longer it will take to charge and discharge the transmission line through the termination resistor ($T = R \bullet C$).

Transmission line distance becomes more critical as data rates increase. As data rates increase, incident (and reflective) waves begin to resemble that of RF transmission line theory. However, due to the nonlinearity of CMOS digital logic, conventional RF transmission theory is not applicable.

HC devices are preferred over HCT devices due to the fact that HC devices have higher switch points than HCT devices. This higher switch point allows HC devices to achieve better incident wave switching on lower impedance lines.

HC/HCT may not have enough drive capability to interface with some of the more popular LSTTL transmission lines. (Possible reason why an HCT device may not be a drop–in replacement of an equivalent TTL device.) This does not pose a major problem since having larger value termination resistors is desirable for CMOS type transmission lines.

By increasing the termination resistance value, the CMOS advantage of low power consumption can be realized. ON Semiconductor recommends a minimum termination resistor value as shown in Figure 38. The termination resistor should be as close to the receiving unit as possible. Another method of terminating the line driver, as well as the receiving unit, is shown in Figure 39. Note that the resistor values in Figure 39 are twice the resistor value of Figure 38; this gives a net equivalent termination value of Figure 38. Even higher values of resistors may be used for either termination method. This reduces power consumption, but at the expense of speed and possible signal degradation.

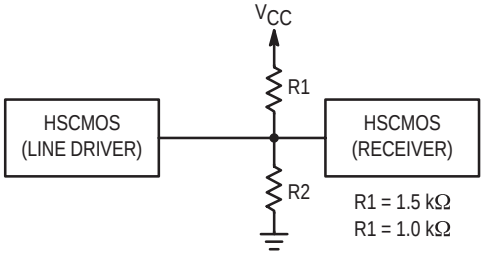


Figure 38. Termination Resistors at the Receiver

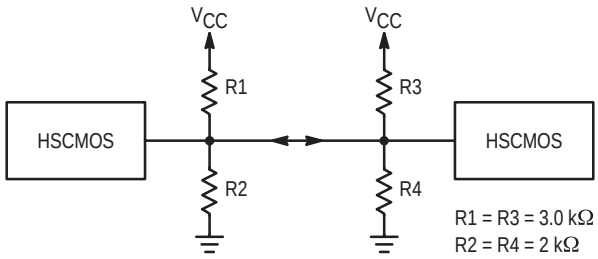


Figure 39. Termination Resistors at Both the Line Driver and Receiver

CMOS LATCH UP

Typically, HSCMOS devices do not latch up with currents of 75 mA forced into or out of the inputs or 300 mA for the outputs under worst case conditions (T_A = 125°C and V_{CC} = 6 V). Under dc conditions for the inputs, the input protection network typically fails, due to grossly exceeding the maximum input voltage rating of – 0.5 to V_{CC} + 0.5 V before latch–up currents are reached. For most designs, latch up will not be a problem, but the designer should be aware of it, what causes it, and how it can be prevented.

Figure 40 shows the layout of a typical CMOS inverter and Figure 41 shows the parasitic bipolar devices that are formed. The circuit formed by the parasitic transistors and resistors is the basic configuration of a silicon controlled rectifier, or SCR. In the latch–up condition, transistors Q1 and Q2 are turned on, each providing the base current necessary for the other to remain in saturation, thereby latching the device on. Unlike a conventional SCR, where the device is turned on by applying a voltage to the base of the NPN transistor, the parasitic SCR is turned on by applying a voltage to the emitter of either transistor. The two emitters that trigger the SCR are the same point, the CMOS output. Therefore, to latch up the CMOS device, the output voltage must be greater than V_{CC} + 0.5 V or less than – 0.5 V and have sufficient current to trigger the SCR. The latch–up mechanism is similar for the inputs.

Once a CMOS device is latched up, if the supply current is not limited, the device can be destroyed or its reliability can be degraded. Ways to prevent such an occurrence are listed below.

1. Industrial controllers driving relays or motors is an environment in which latch up is a potential problem. Also, the ringing due to inductance of long transmission lines in an industrial setting could provide enough energy to latch up CMOS devices. Opto–isolators, such as ON Semiconductor's MOC3011, are recommended to reduce chances of latch up. See the ON Semiconductor Master Selection Guide for a complete listing of ON Semiconductor opto–isolators.
2. Ensure that inputs and outputs are limited to the maximum rated values.
   $-1.5 \le V_{in} \le V_{CC}$ +1.5 V referenced to GND or
   $-0.5 \le V_{in} \le V_{CC}$ +0.5 V referenced to GND
   $-0.5 \le V_{out} \le V_{CC}$ +0.5 V referenced to GND
   $|I_{in}| \le$ 20 mA
   $|I_{out}| \le$ 25 mA for standard outputs
   $|I_{out}| \le$ 35 mA for bus–driver outputs
3. If voltage transients of sufficient energy to latch up the device are expected on the inputs or outputs, external protection diodes can be used to clamp the voltage. Another method of protection is to use a series resistor to limit the expected worst case current to the maximum ratings value. See **Handling Precautions** for other possible protection circuits and a discussion of ESD prevention.
4. Sequence power supplies so that the inputs or outputs of HSCMOS devices are not active before the supply pins are powered up (e.g., recessed edge connectors and/or series resistors may be used in plug–in board applications).
5. Voltage regulating and filtering should be used in board design and layout to ensure that power supply lines are free of excessive noise.
6. Limit the available power supply current to the devices that are subject to latch–up conditions. This can be accomplished with the power–supply filtering network or with a current–limiting regulator.

RECOMMENDED READING

Paul Mannone, "Careful Design Methods Prevent CMOS Latch–Up", EDN, January 26, 1984.

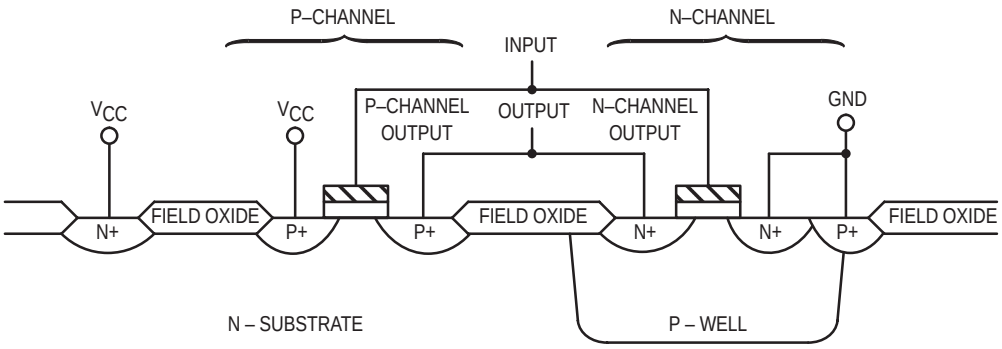


Figure 40. CMOS Wafer Cross Section

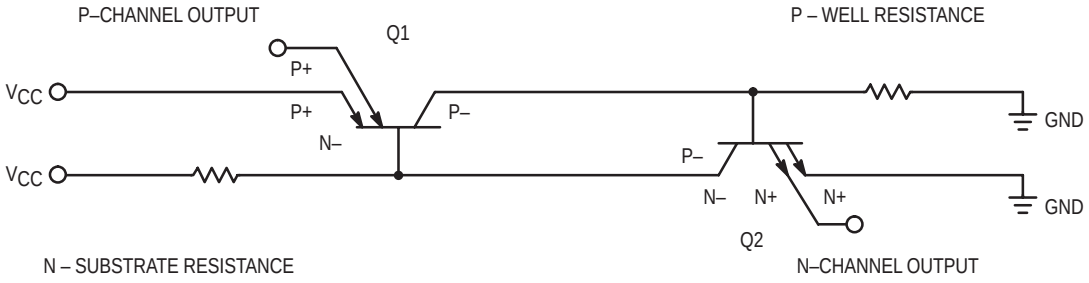


Figure 41. Latch–Up Circuit Schematic

MAXIMUM POWER DISSIPATION

The maximum power dissipation for ON Semiconductor HSCMOS packages is 750 mW for both ceramic and plastic DIPs and 500 mW for SOIC packages. The deratings are – 10 mW/°C from 65°C for plastic DIPs, and – 7 mW/°C from 65°C for SOIC packages. This is illustrated in Figure 42.

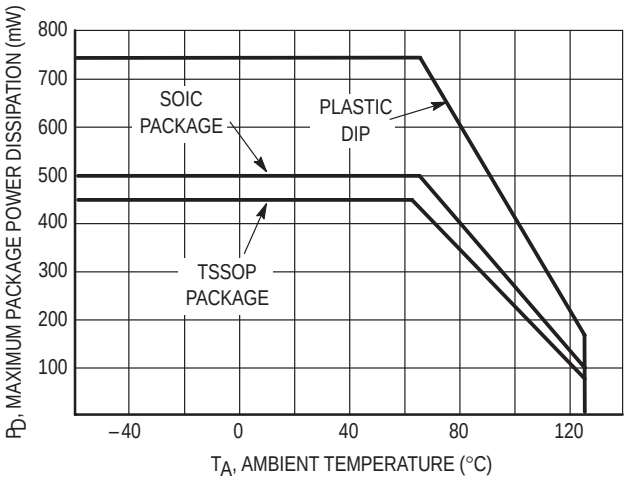


Figure 42. Maximum Package Power Dissipation versus Temperature

Internal heat generation in HSCMOS devices comes from two sources, namely, the quiescent power and dynamic power consumption.

In the quiescent state, either the P–channel or N–channel transistor in each complementary pair is off except for small source–to–drain leakage due to the inputs being either at V_{CC} or ground. Also, there are the small leakage currents flowing in the reverse–biased input protection diodes and the parasitic diodes on the chip. The specification which takes all leakage into account is called Maximum Quiescent Supply Current (per package), or I_{CC}, and is shown on all data sheets.

The three factors which directly affect the value of quiescent power dissipation are supply voltage, device complexity, and temperature. On the data sheets, I_{CC} is specified only at V_{CC} = 6.0 V because this is the worst–case supply voltage condition. Also, larger or more complex devices consume more quiescent power because these devices contain a proportionally greater reverse–biased diode junction area and more off (leaky) FETs.

Finally, as can be seen from the data sheets, temperature increases cause I_{CC} increases. This is because at higher temperatures, leakage currents increase.

HC QUIESCENT POWER DISSIPATION

When HC device inputs are virtually at V_{CC} or GND potential (as in a totally CMOS system), quiescent power dissipation is minimized. The equation for HC quiescent power dissipation is given by:

$$P_D = V_{CC}I_{CC}$$

Worst–case I_{CC} occurs at V_{CC} = 6.0 V. The value of I_{CC} at V_{CC} = 6.0 V, as specified in the data sheets, is used for all power supply voltages from 2 to 6 V.

HCT QUIESCENT POWER DISSIPATION

Although HCT devices belong to the CMOS family, their input voltage specifications are identical to those of LSTTL. HCT parts can therefore be either judiciously substituted for or mixed with LS devices in a system.

TTL output voltages are V_{OL} = 0.4 V (max) and V_{OH} = 2.4 to 2.7 V (min).

Slightly higher I_{CC} current exists when an HCT device is driven with V_{OL} = 0.4 V (max) because this voltage is high enough to partially turn on the N–channel transistor. However, when being driven with a TTL V_{OH}, HCT devices exhibit large additional current flow (ΔI_{CC}) as specified on HCT device data sheets. ΔI_{CC} current is caused by the off–rail input voltage turning on both the P and N channels of the input buffer. This condition offers a relatively low impedance path from V_{CC} to GND. Therefore, the HCT quiescent power dissipation is dependent on the number of inputs applied at the TTL V_{IH} logic voltage level.

The equation for HCT quiescent power dissipation is given by:

$$P_D = I_{CC}V_{CC} + \eta\Delta I_{CC}V_{CC}$$

where η = the number of inputs at the TTL V_{IH} level.

HC AND HCT DYNAMIC POWER DISSIPATION

Dynamic power dissipation is calculated in the same way for both HC and HCT devices. The three major factors which directly affect the magnitude of dynamic power dissipation are load capacitance, internal capacitance, and switching transient currents.

The dynamic power dissipation due to capacitive loads is given by the following equation:

$$P_D = C_L V_{CC}^2 f$$

where P_D = power in μW, C_L = capacitive load in pF, V_{CC} = supply voltage in volts, and f = output frequency driving the load capacitor in MHz.

All CMOS devices have internal parasitic capacitances that have the same effect as external load capacitors. The magnitude of this internal no–load power dissipation capacitance, C_{PD}, is specified as a typical value.

Finally, switching transient currents affect the dynamic power dissipation. As each gate switches, there is a short period of time in which both N– and P–channel transistors are partially on, creating a low–impedance path from V_{CC} to ground. As switching frequency increases, the power dissipation due to this effect also increases.

The dynamic power dissipation due to C_{PD} and switching transient currents is given by the following equation:

$$P_D = C_{PD}V_{CC}^2 f$$

Therefore, the total dynamic power dissipation is given by:

$$P_D = (C_L + C_{PD})V_{CC}^2 f$$

Total power dissipation for HC and HCT devices is merely a summation of the dynamic and quiescent power dissipation elements. When being driven by CMOS logic voltage levels (rail to rail), the total power dissipation for both HC and HCT devices is given by the equation:

$$P_D = V_{CC}I_{CC} + (C_L + C_{PD})V_{CC}^2 f$$

When being driven by LSTTL logic voltage levels, the total power dissipation for HCT devices is given by the equation:

$$P_D = V_{CC}I_{CC} + V_{CC}\Delta I_{CC}(\delta, + \delta_2 + \ldots + \delta_n) + (C_L + C_{PD})V_{CC}^2 f$$

where δ_n = duty cycle of LSTTL output applied to each input of an HCT device.

THERMAL MANAGEMENT

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the IC junction temperatures low.

Electrical power dissipated in any integrated circuit is a source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature of 25°C in still air. The temperature increase, then, depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point. See page 29 for the calculation of CMOS power consumption.

The temperature at the junction is a function of the packaging and mounting system's ability to remove heat generated in the circuit — from the junction region to the ambient environment. The basic formula for converting power dissipation to estimated junction temperature is:

$$T_J = T_A + P_D(\overline{\theta}_{JC} + \overline{\theta}_{CA}) \qquad (1)$$

or

$$T_J = T_A + P_D(\overline{\theta}_{JA}) \qquad (2)$$

where

T_J = maximum junction temperature

T_A = maximum ambient temperature

P_D = calculated maximum power dissipation including effects of external loads (see Power Dissipation on page 40).

$\overline{\theta}_{JC}$ = average thermal resistance, junction to case

$\overline{\theta}_{CA}$ = average thermal resistance, case to ambient

$\overline{\theta}_{JA}$ = average thermal resistance, junction to ambient

This ON Semiconductor recommended formula has been approved by RADC and DESC for calculating a "practical" maximum operating junction temperature for MIL-M-38510 (JAN) devices.

Only two terms on the right side of equation (1) can be varied by the user — the ambient temperature, and the device case-to-ambient thermal resistance, $\overline{\theta}_{CA}$. (To some extent the device power dissipation can also be controlled, but under recommended use the V_{CC} supply and loading dictate a fixed power dissipation.) Both system air flow and the package mounting technique affect the $\overline{\theta}_{CA}$ thermal resistance term. $\overline{\theta}_{JC}$ is essentially independent of air flow and external mounting method, but is sensitive to package material, die bonding method, and die area.

For applications where the case is held at essentially a fixed temperature by mounting on a large or temperature-controlled heat sink, the estimated junction temperature is calculated by:

$$T_J = T_C + P_D(\overline{\theta}_{JC}) \qquad (3)$$

where T_C = maximum case temperature and the other parameters are as previously defined.

The maximum and average $\overline{\theta}_{JC}$ resistance values for standard IC packages are given in 2.

Table 2. Thermal Resistance Values for Standard I/C Packages

Thermal Resistance In Still Air								
Package Description								
No. Leads	Body Style	Body Material	Body W × L	Die Bonds	Die Area (Sq. Mils)	Flag Area (Sg. Mils)	θ_{JC} (°C/Watt)	
							Avg.	Max.
14	DIL	Epoxy	1/4″ × 3/4″	Epoxy	4096	6,400	38	61
16	DIL	Epoxy	1/4″ × 3/4″	Epoxy	4096	12,100	34	54
20	DIL	Epoxy	0.35″ × 0.35″	Epoxy	4096	14,400	N/A	N/A

NOTES:
1. All plastic packages use copper lead frames.
2. Body style DIL is "Dual-In-Line."
3. Standard Mounting Method: Dual-In-Line Socket or P/C board with no contact between bottom of package and socket or P/C board.

AIR FLOW

The effect of air flow over the packages on $\overline{\theta}_{JA}$ (due to a decrease in $\overline{\theta}_{CA}$) reduces the temperature rise of the package, therefore permitting a corresponding increase in power dissipation without exceeding the maximum permissible operating junction temperature.

Even though different device types mounted on a printed circuit board may each have different power dissipations, all will have the same input and output levels provided that each is subject to identical air flow and the same ambient air temperature. This eases design, since the only change in levels between devices is due to the increase in ambient temperatures as the air passes over the devices, or differences in ambient temperature between two devices.

The majority of users employ some form of air-flow cooling. As air passes over each device on a printed circuit board, it absorbs heat from each package. This heat gradient from the first package to the last package is a function of the air flow rate and individual package dissipations. 3 provides gradient data at power levels of 200 mW, 250 mW, 300 mW, and 400 mW with an air flow rate of 500 Ifpm. These figures show the proportionate increase in the junction temperature of each dual in-line package as the air passes over each device. For higher rates of air flow the change in junction temperature from package to package down the airstream will be lower due to greater cooling.

3. Thermal Gradient of Junction Temperature (16-Pin Dual-In-Line Package)

Power Dissipation (mW)	Junction Temperature Gradient (°C/Package)
200	0.4
250	0.5
300	0.63
400	0.88

Devices mounted on 0.062″ PC board with Z axis spacing of 0.5″.
Air flow is 500 lfpm along the Z axis.

4 is graphically illustrated in Figure 43 which shows that the reliability for plastic and ceramic devices is the same until elevated junction temperatures induce intermetallic failures in plastic devices. Early and mid-life failure rates of plastic devices are not effected by this intermetallic mechanism.

PROCEDURE

After the desired system failure rate has been established for failure mechanisms other than intermetallics, each device in the system should be evaluated for maximum junction temperature. Knowing the maximum junction temperature, refer to 4 or Equation (1) on page 41 to determine the continuous operating time required to 0.1% bond failures due to intermetallic formation. At this time, system reliability departs from the desired value as indicated in Figure 43.

Air flow is one method of thermal management which should be considered for system longevity. Other commonly used methods include heat sinks for higher powered devices, refrigerated air flow and lower density board stuffing. Since $\overline{\theta}_{CA}$ is entirely dependent on the application, it is the responsibility of the designer to determine its value. This can be achieved by various techniques including simulation, modeling, actual measurement, etc.

The material presented here emphasizes the need to consider thermal management as an integral part of system design and also the tools to determine if the management methods being considered are adequate to produce the desired system reliability.

4. Device Junction Temperature versus Time to 0.1% Bond Failures

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

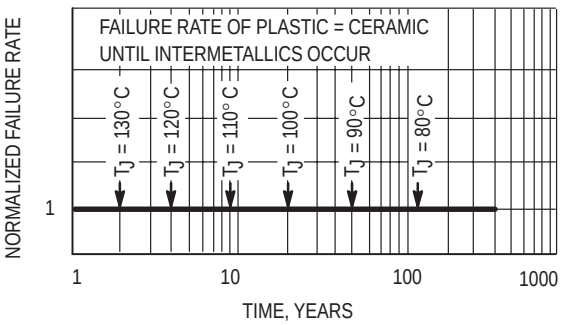


Figure 43. Failure Rate versus Time Junction Temperature

CAPACITIVE LOADING EFFECTS ON PROPAGATION DELAY

In addition to temperature and power–supply effects, capacitive loading effects should be taken into account. The additional propagation delay may be calculated if the short circuit current for the device is known. Expected minimum numbers may be determined from 5.

From the equation

$$i = \frac{Cdv_C}{dt}$$

this approximation follows:

$$I = \frac{C\Delta V}{\Delta t}$$

so

$$\Delta t = \frac{C\Delta V}{I}$$

or

$$\Delta t = \frac{C(0.5\ V_{CC})}{I}$$

because the propagation delay is measured to the 50% point of the output waveform (typically 0.5 V_{CC}).

This equation gives the general form of the additional propagation delay. To calculate the propagation delay of a device for a particular load capacitance, C_L, the following equation may be used.

$$t_{PT} = t_P + 0.5\ V_{CC}\ (C_L - 50\ pF)/I_{OS}$$

where t_{PT} = total propagation delay

t_P = specified propagation delay with 50 pF load

C_L = actual load capacitance

I_{OS} = short circuit current (5)

An example is given here for t_{PHL} of the 74HC00 driving a 150 pF load.

$$V_{CC} = 4.5\ V$$

$$t_{PHL}\ (50\ pF) = 18\ ns$$

$$C_L = 150\ pF$$

$$I_{OS} = 17.3\ mA$$

$$t_{PHL}\ (150\ pF) = 18\ ns + \frac{(0.5)(4.5\ V)(150\ pF - 50\ pF)}{17.3\ mA}$$

$$= 18\ ns + 13\ ns$$

$$= 31\ ns$$

Another example for C_L = 0 pF and all other parameters the same.

$$t_{PHL}\ (0\ pF) = 18\ ns + \frac{(0.5)(4.5\ V)(0\ pF - 50\ pF)}{17.3\ mA}$$

$$= 18\ ns + (-6.5\ ns)$$

$$t_{PHL} = 11.5\ ns$$

This method gives the expected propagation delay and is intended as a design aid, not as a guarantee.

Table 5. Expected Minimum Short Circuit Currents*

Parameter	V_{CC}	Standard Drivers			Bus Drivers			Unit
		25°C	85°C	125°C	25°C	85°C	125°C	
Output Short Circuit Source Current	2.0	1.89	1.83	1.80	3.75	3.64	3.60	mA
	4.5	18.5	15.0	13.4	37.0	30.0	26.6	
	6.0	35.2	28.0	24.6	70.6	56.1	49.2	
Output Short Circuit Sink Current	2.0	1.55	1.55	1.55	2.45	2.45	2.43	mA
	4.5	17.3	14.0	12.5	27.2	22.1	19.6	
	6.0	33.4	26.5	23.2	52.6	41.7	36.5	

*These values are intended as design aids, not as guarantees.

TEMPERATURE EFFECTS ON DC AND AC PARAMETERS

One of the inherent advantages of CMOS devices is that characteristics of the N– and P–channel transistors, such as drive current, channel resistance, propagation delay, and output transition time, track each other over a wide temperature range. Figure 44 shows the temperature relationships for these parameters. To illustrate the effects of temperature on noise margin, Figure 45 shows the typical transfer characteristics for devices with buffered inputs and outputs. Note that the typical switch point is at 45% of the supply voltage and is minimally affected by temperature.

The graphs in this section are intended to be design aids, not guarantees.

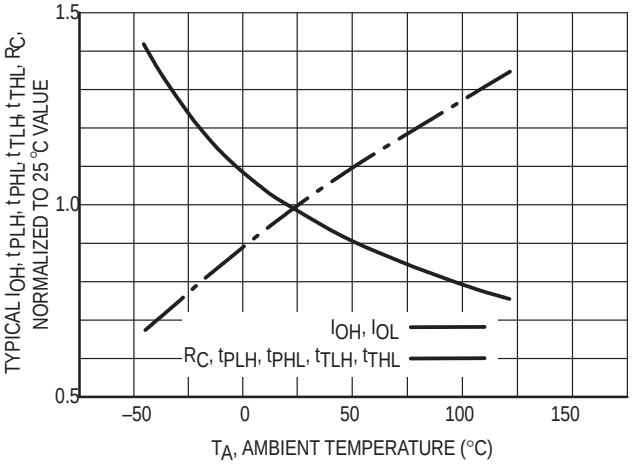


Figure 44. Characteristics of Drive Current, Channel Resistance, and AC Parameters Over Temperature

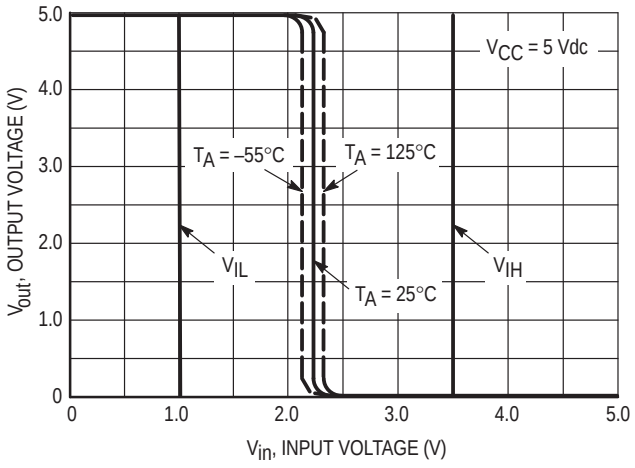


Figure 45. Temperature Effects on the HC Transfer Characteristics

SUPPLY VOLTAGE EFFECTS ON DRIVE CURRENT AND PROPAGATION DELAY

The transconductive gain, I_{out}/V_{in}, of MOSFETs is proportional to the gate voltage minus the threshold voltage, $V_G - V_T$. The gate voltage at the input of the final stage of buffered devices is approximately the power supply voltage, V_{CC} or GND. Because $V_G = V_{CC}$ or GND, the output drive current is proportional to the supply voltage. Propagation delays for CMOS devices are also affected by the power supply voltage, because most of the delay is due to charging and discharging internal capacitances. Figure 46 and Figure 47 show the typical variation of current drive and propagation delay, normalized to V_{CC} = 4.5 V for 2.0 ≤ V_{CC} ≤ 6.0 V. These curves may be used with the tables on each data sheet to arrive at parametric values over the voltage range.

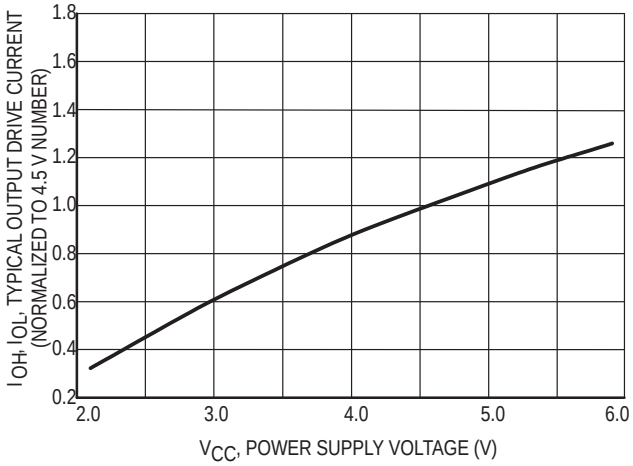


Figure 46. Drive Current versus V_{CC}

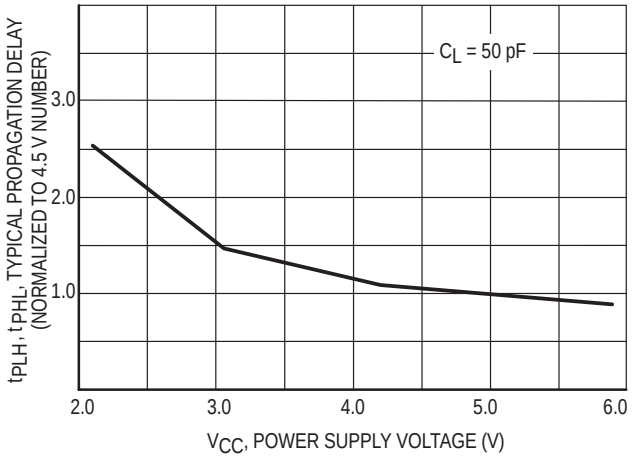


Figure 47. Propagation Delay versus V_{CC}

DECOUPLING CAPACITORS

The switching waveforms shown in Figure 48 and Figure 49 show the current spikes introduced to the power supply and ground lines. This effect is shown for a load capacitance of less than 5 pF and for 50 pF. For ideal power supply lines with no series impedance, the spikes would pose no problem. However, actual power supply and ground lines do possess series impedance, giving rise to noise problems. For this reason, care should be taken in board layouts, ensuring low impedance paths to and from logic devices.

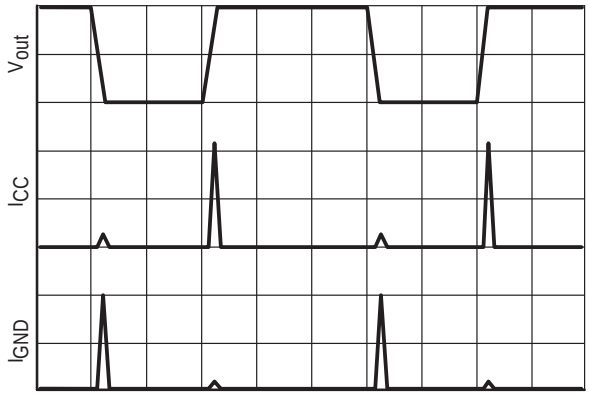
To absorb switching spikes, the following HSCMOS devices should be bypassed with good quality 0.022 μF to 0.1 μF decoupling capacitors:

1. Bypass every device driving a bus with all outputs switching simultaneously.
2. Bypass all synchronous counters.
3. Bypass devices used as oscillator elements.
4. Bypass Schmitt–trigger devices with slow input rise and fall times. The slower the rise and fall time, the larger the bypass capacitor. Lab experimentation is suggested.

Bypass capacitors should be distributed over the circuit board. In addition, boards could be decoupled with a 1 μF capacitor.

BUFFERED DEVICE: INPUT t_r, $t_f \leq 500$ ns, $C_L < 5$ pF

Figure 48. Switching Currents for $C_L < 5$ pF



BUFFERED DEVICE: INPUT t_r, $t_f \leq 500$ ns, $C_L < 5$ pF

Figure 49. Switching Currents for $C_L = 50$ pF

INTERFACING

HSCMOS devices have a wide operating voltage range (V_{CC} = 2 to 6 V) and sufficient current drive to interface with most other logic families available today. In this section, various interface schemes are given to aid the designer (see Figure 50 through Figure 55). The various types of CMOS devices with their input/output levels and comments are given in 6.

ON Semiconductor presently has available several CMOS memories and microprocessors (see 7) which are designed to directly interface with High–Speed CMOS. With these devices now available, the designer has an attractive alternative to LSTTL/NMOS, and a total HSCMOS system is now possible. (See SG102, CMOS System IC Selection Guide, for more information.)

Device designators are as follows:

HC This is a high–speed CMOS device with CMOS input switching levels and buffered CMOS outputs. The numbering of devices with this designator follows the LSTTL numbering sequence. These devices are functional and pinout equivalents of LSTTL devices (e.g., HC00A, HC245A, etc.). Exceptions to this are devices that are functional and pinout equivalents to metal–gate CMOS devices (e.g., HC4066, HC4538A, etc.).

HCU This is an unbuffered high–speed CMOS device with only one stage between the input and output. Because this is an unbuffered device, input and output levels may differ from buffered devices. At present, the family contains only one unbuffered device, the HCU04A.

HCT This is a high–speed CMOS device with an LSTTL–to–CMOS input buffer stage. These devices are designed to interface with LSTTL outputs operating at V_{CC} = 5 V ± 10%. HCT devices have fully buffered CMOS outputs that directly drive HSCMOS or LSTTL devices.

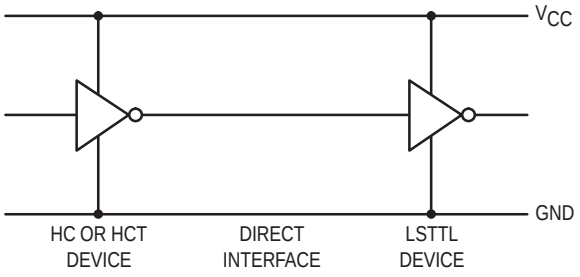


Figure 50. HC to LSTTL Interfacing

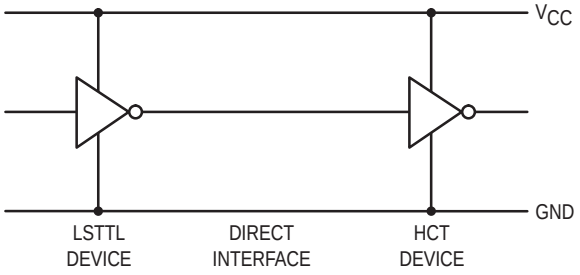


Figure 51. LSTTL to HCT Interfacing

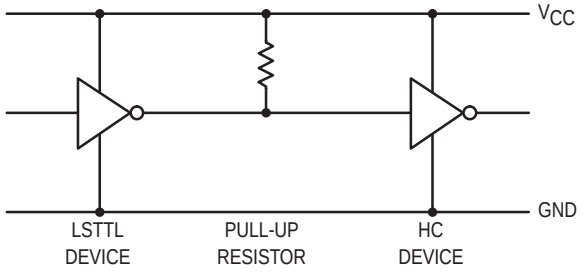


Figure 52. LSTTL to HC Interfacing

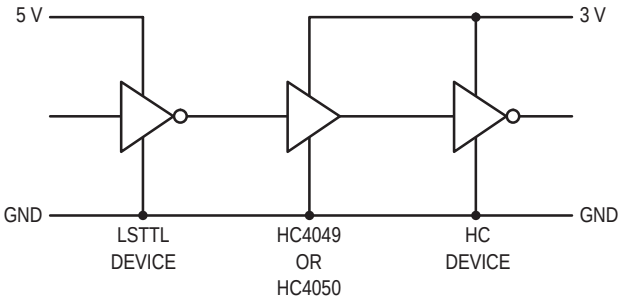
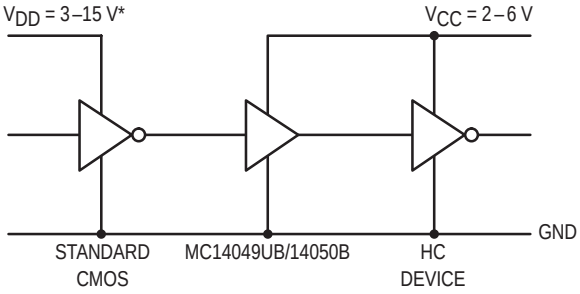


Figure 53. LSTTL to Low–Voltage HSCMOS



*V_{OH} must be greater than V_{IH} of low voltage Device;
V_{DD} = 3–18 V may be used if interfacing to 14049UB/14050B.

Figure 54. High Voltage CMOS to HSCMOS

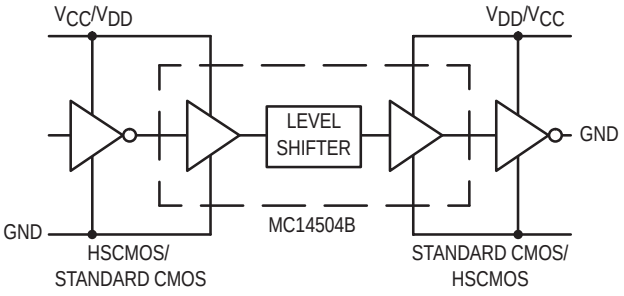


Figure 55. Up/Down Level Shifting Using the MC14504B

Table 6. Interfacing Guide

Device	Input Level	Output Level	Comments
HCXXX	CMOS	CMOS	LSTTL Functional and Pinout Equivalent Devices
HC4XXX	CMOS	CMOS	CMOS Functional and Pinout Equivalent Devices
HCUXX	CMOS	CMOS	Used in Linear Applications
HCTXXX	TTL	CMOS	HSCMOS Device with TTL–to–CMOS Input Buffering
MC14049UB MC14050B	$-0.5 \le V_{in} \le 18$ V	CMOS	Metal–Gate CMOS High–to–Low Level Translators, CMOS Switching Levels
MC14504B	CMOS or TTL	CMOS	Metal–Gate CMOS High–to–Low or Low–to–High Level Translator

Table 7. CMOS Memories and Microprocessors

CMOS Memories	CMOS Microprocessors	
MCM6147	MC68HC01	MC146805G2
MCM61L47	MC68HC03	MC146805H2
MCM68HC34	MC68HC11A8	MC1468705F2
	MC68HC11D4	MC1468705G2
	MC68HC811A2	MC68HC05C4
	MC68HC811D4	MC68HSC05C4
	MC68HC04P3	MC68HC05C8
	MC146805E2	MC68HC805C4
	MC146805F2	MC68HC000

RECOMMENDED READING

S. Craig, “Using High–Speed CMOS Logic for Microprocessor Interfacing”, Application Note–868, ON Semiconductor Products Inc., 1982.

TYPICAL PARAMETRIC VALUES

Given a fixed voltage and temperature, the electrical characteristics of High–Speed CMOS devices depend primarily on design, layout, and processing variations inherent in semiconductor fabrication.

A preliminary evaluation of each device type essentially guarantees that the design and layout of the device conforms to the criteria and standards set forth in the design goals. With very few exceptions, device electrical parameters, once established, do not vary due to design and layout.

Of much more concern is processing variation. A digital processing line is allowed to deviate over a fairly broad processing range. This allows the manufacturer to incur reduced processing costs. These reduced processing costs are passed on to the consumer in the form of lower device prices.

Processing variation is the range from worst case to best case processing and is defined as the process window. This window is established with the aid of statistical process control (SPC). With SPC, when a processing parameter approaches the process window limit, that parameter is adjusted toward the middle of the window. This keeps process variations within a predetermined tolerance.

ON Semiconductor characterizes each device type over this process window. Each device type is characterized by allowing experimental lots to be processed using worst case and best case processing. The worst case processed lots usually determine the minimum or maximum guaranteed limit. (Whether the limit is a guaranteed minimum or maximum depends on the particular parameter being measured.)

In production, these limits are guaranteed by probe and final test and therefore appear independent of process variation to the end user. However, this does not hold true for the mean value of the total devices processed. The mean value, commonly referred to as a typical value, shifts over processing and therefore varies from lot to lot or even wafer to wafer within a lot.

As with all processing or manufacturing, the total devices being produced fit the normal distribution or bell curve of Figure 56. In order to guarantee a valid typical value, a typical number plus a tolerance, would have to be specified and tested (see Figure 57). However, this would greatly increase processing costs which would have to be absorbed by the consumer.

In some cases, the device's actual values are so small that the resolution of the automatic test equipment determines the guaranteed limit. An example of this is quiescent supply current and input leakage current.

Most manufacturers provide typical numbers by one of two methods. The first method is to simply double or halve, depending on the parameter, the guaranteed limit to determine a typical number. This would theoretically put all processed lots in the middle of the process window. Another approach to typical numbers is to use a typical value that is derived from the aforementioned experimental lots. However, neither method accurately reflects the mean value of devices any one consumer can expect to receive.

Therefore, the use of typical parametric numbers for design purposes does not constitute sound engineering design practice. Worst case analysis dictates the use of guaranteed minimum or maximum values. The only possible exception would be when no guaranteed value is given. In this case a typical value may be used as a ballpark figure.

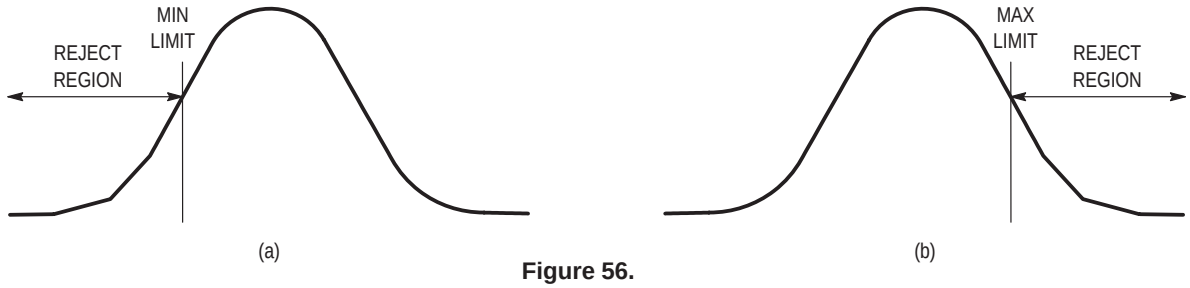


Figure 56.

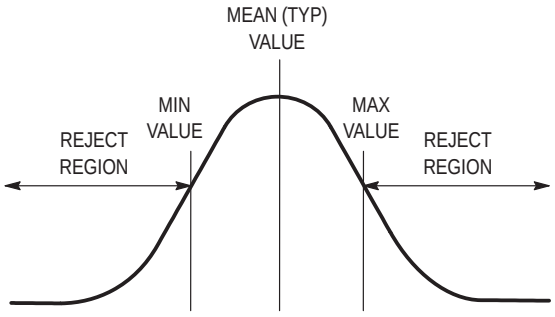


Figure 57.

REDUCTION OF ELECTROMAGNETIC INTERFERENCE (EMI)

Electromagnetic interference (EMI) and radio frequency interference (RFI) are phenomena inherent in all electrical systems covering the entire frequency spectrum. Although the characteristics have been well documented, EMI remains difficult to deal with due to numerous variables. EMI should be considered at the beginning of a design, and taken into account during all stages, including production and beyond.

These entities must be present for EMI to be a factor: (1) a source of EMI, (2) a transmission medium for EMI, and (3) a receiver of EMI. Several sources include relays, FM transmitters, local oscillators in receivers, power lines, engine ignitions, arc welders, and lighting. EMI transmission paths include ground connections, cables, and the space between conductors. Some receivers of EMI are radar receivers, computers, and television receivers.

For microprocessor based equipment, the source of emissions is usually a current loop on a PC board. The chips and their associated loop areas also function as receivers of EMI. The fact is that PC boards which radiate high levels of EMI are also more likely to act as receivers of EMI.

All logic gates are potential transmitters and receivers of emissions. Noise immunity and noise margin are two criterion which measure a gate's immunity to noise which could be caused by EMI. CMOS technology, as opposed to the other commonly used logic families, offers the best value for noise margin, and is therefore an excellent choice when considering EMI.

The electric and magnetic fields associated with ICs are proportional to the current used, the current loop area, and the switching transition times. CMOS technology is preferred due to smaller currents. Also, the current loop area can be reduced by the use of surface mount packages.

In a system where several pieces of equipment are connected by cables, at least five coupling paths should be taken into account to reduce EMI. They are: (1) common ground impedance coupling (a common impedance is shared between an EMI source and receiver), (2) common–mode, field–to–cable coupling (electromagnetic fields enter the loop found by two pieces of equipment, the cable connecting them, and the ground plane), (3) differential–mode, field–to–cable coupling (electromagnetic fields enter the loop formed by two pieces of equipment and the cable connecting them), (4) crosstalk coupling (signals in one transmission line are coupled into another transmission line), and (5) a conductive path through power lines.

Shielding is a means of reducing EMI. Some of the more commonly used shields against EMI and RFI contain stainless steel fiber–filled polycarbonate, aluminum flake–filled polycarbonate/ABS coated with nickel and copper electrolysis plating or cathode sputtering, nickel coated graphite fiber, and polyester SMC with carbon–fiber veil. Several manufacturers who make conductive compounds and additives are listed below.

SHIELDING MANUFACTURERS

General Electric Co., Plastics Group, Pittsfield, MA

Mobay Chemical Corp., Pittsburgh, PA

Wilson–Fiberfil International, Evansville, IN

American Cyanamid Co., Wayne, NJ

Fillite U.S.A., Inc., Huntington, WV

Transnet Corp., Columbus, OH

ON Semiconductor does not recommend, or in any way warrant the manufacturers listed here. Additionally, no claim is made that this list is by any means complete.

RECOMMENDED READING

D. White, K. Atkinson, and J. Osburn, "Taming EMI in Microprocessor Systems", *IEEE Spectrum*, Vol. 22, Number 12, Dec. 1985.

D. White and M. Mardiguian, *EMI Control Methodology and Procedures*, 1985.

H. Denny, *Grounding for the Control of EMI*.

M. Mardiguian, *How to Control Electrical Noise*.

D. White, *Shielding Design Methodology and Procedures*.

For more information on this subject, contact:

Interference Control Technologies
Don White Consultants, Inc., Subsidiary
State Route 625
P.O. Box D
Gainesville, VA 22065

HYBRID CIRCUIT GUIDELINES

High–Speed CMOS devices, when purchased in chip (die) form, are useful in hybrid circuits. Most high–speed devices are fabricated with P wells and N substrates. Therefore, the substrates should be tied to V_{CC} (+ supply).

Several devices however, are fabricated with N wells and P substrates. In this case, the substrates should be tied to GND. The best solution to alleviate confusion about the substrate is the use of nonconductive or insulative substrates. This averts the necessity of tying the substrate off to either V_{CC} or GND.

For more information on hybrid technology, contact:

International Society for Hybrid Microelectronics
P.O. Box 3255
Montgomery, AL 36109

SCHMITT–TRIGGER DEVICES

Schmitt–trigger devices exhibit the effect of hysteresis. Hysteresis is characterized by two different switching threshold levels, one for positive–going input transitions and the other for negative–going input transitions.

Schmitt triggers offer superior noise immunity when compared to standard gates and inverters. Applications for Schmitt triggers include line receivers, sine to square wave converters, noise filters, and oscillators. ON Semiconductor offers six versatile Schmitt–trigger devices in the High–Speed CMOS logic family (see 8).

The typical voltage transfer characteristics of a standard CMOS inverter and a CMOS Schmitt–trigger inverter are compared in Figure 58 and Figure 59. The singular transfer threshold of the standard inverter is replaced by two distinct thresholds in a Schmitt–trigger inverter. During a positive–going transition of V_{in}, the output begins to go low after the V_{T+} threshold is reached. During a negative–going V_{in} transition, V_{out} begins to go high after the V_{T-} threshold is reached. The difference between V_{T+} and V_{T-} is defined as V_H, the hysteresis voltage.

As a direct result of hysteresis, Schmitt–trigger circuits provide excellent noise immunity and the ability to square up signals with long rise and fall times. Positive–going input noise excursions must rise above the V_{T+} threshold before they affect the output. Similarly, negative–going input noise excursions must drop below the V_{T-} threshold before they affect the output.

The HC132A can be used as a direct replacement for the HC00A NAND gate, which does not have Schmitt–trigger capability. The HC132A has the same pin assignment as the HC00A. Schmitt–trigger logic elements act as standard logic elements in the absence of noise or slow rise and fall times, making direct substitution possible.

Versatility and low cost are attractive features of CMOS Schmitt triggers. With six Schmitt triggers per HC14A package, one trigger can be used for a noise elimination application while the other five function as standard inverters. Similarly, each of the four triggers in the HC132A can be used as either Schmitt triggers or NAND gates or some combination of both.

Table 8. Schmitt–Trigger Devices

HC14A	Hex Schmitt–Trigger Inverter
HCT14A	Hex Schmitt–Trigger Inverter with LSTTL Inputs
HC132A	Quad 2–Input NAND Gate with Schmitt–Trigger Inputs

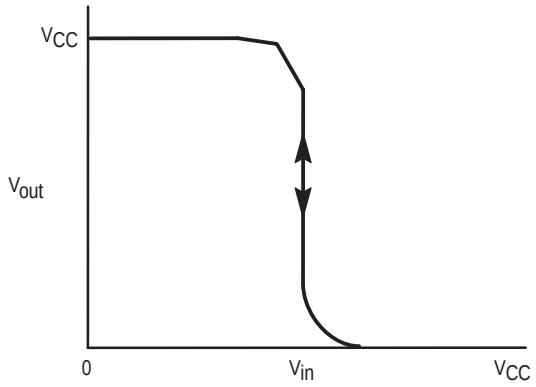


Figure 58. Standard Inverter Transfer Characteristic

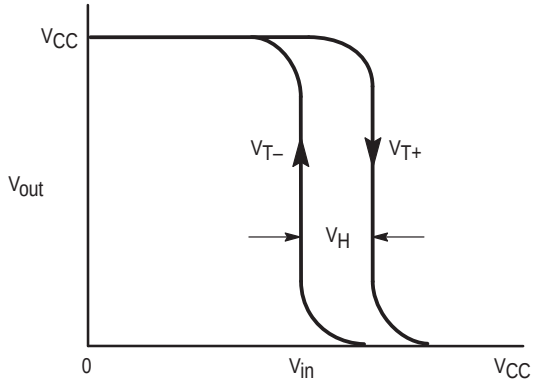


Figure 59. Schmitt–Trigger Inverter Transfer Characteristic

OSCILLATOR DESIGN WITH HIGH–SPEED CMOS

Oscillator design is a fundamental requirement of many systems and several types are discussed in this section. In general, an oscillator is comprised of two parts: an active network and a feedback network. The active network is usually in the form of an amplifier, or an unbuffered inverter, such as the HCU04. The feedback network is mainly comprised of resistors, capacitors, and depending upon the application, a quartz crystal or ceramic resonator.

Buffered inverters are never recommended in oscillator applications due to their high gain and added propagation delay. For this reason ON Semiconductor manufactures the HCU04A, which is an unbuffered hex inverter.

Oscillators for use in digital systems fall into two general categories, RC oscillators and crystal or ceramic resonator oscillators. Crystal oscillators have the best performance, but are more costly, especially for nonstandard frequencies. RC oscillators are more useful in applications where stability and accuracy are not of prime importance. Where high performance at low frequencies is desired, ceramic resonators are sometimes used.

RC OSCILLATORS

The circuit in Figure 60 shows a basic RC oscillator using the HCU04A. When the input voltage of the first inverter reaches the threshold voltage, the outputs of the two inverters change state, and the charging current of the capacitor changes direction. The frequency at which this circuit oscillates depends upon R1 and C. The equation to calculate these component values is given in Figure 60.

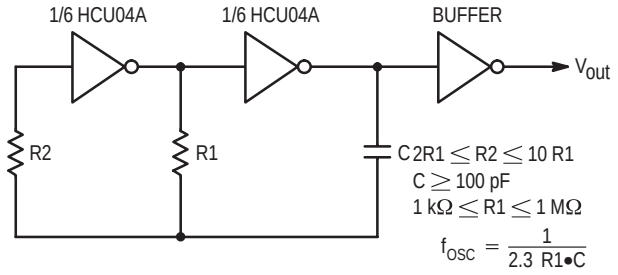


Figure 60. RC Oscillator

Certain constraints must be met while designing this type of oscillator. Stray capacitance and inductance must be kept to a minimum by placing the passive components as close to the chip as possible. Also, at higher frequencies, the HCU04A's propagation delay becomes a dominant effect and affects the cycle time. A polystyrene capacitor is recommended for optimum performance.

CRYSTAL OSCILLATORS

Crystal oscillators provide the required stability and accuracy which is necessary in many applications. The crystal can be modeled as shown in Figure 62.

The power dissipated in a crystal is referred to as the drive level and is specified in mW. At low drive levels, the resonant resistance of the crystal can be so large as to cause start–up problems. To overcome this problem, the amplifier (inverter) should provide enough amplification, but not too much as to overdrive the crystal.

Figure 61 shows a Pierce crystal oscillator circuit, which is a popular configuration with CMOS.

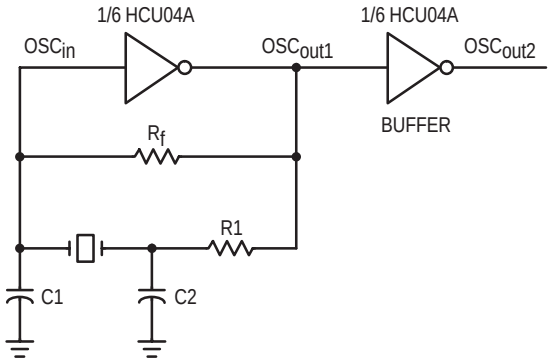
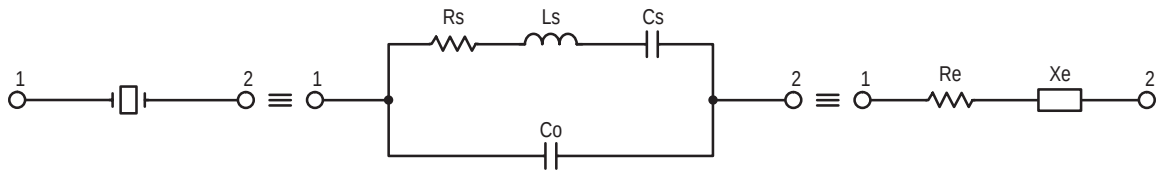


Figure 61. Pierce Crystal Oscillator Circuit

Choosing R1

Power is dissipated in the effective series resistance of the crystal. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 limits the drive level.



Values are supplied by the crystal manufacturer
(parallel resonant crystal)

Figure 62. Equivalent Crystal Networks

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency at OSC Out 2. The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or RI

must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Selecting R_f

The feedback resistor (R_f) typically ranges up to 20 MD. R_f determines the gain and bandwidth of the amplifier. Proper bandwidth ensures oscillation at the correct frequency plus roll–off to minimize gain at undesirable frequencies, such as the first overtone. R_f must be large enough so as not to affect the phase of the feedback network in an appreciable manner.

RECOMMENDED READING

D. Babin, "Designing Crystal Oscillators", Machine Design, March 7, 1985.
D. Babin, "Guidelines for Crystal Oscillator Design", Machine Design, April 25, 1985.

PRINTED CIRCUIT BOARD LAYOUT

Noise generators on the power supply lines should be decoupled. The two major sources of noise on the power supply lines are peak current in output stages during switching and the charging and discharging of parasitic capacitances.

A good power distribution network is essential before decoupling can provide any noise reduction. Avoid using jumpers for ground and power connections; the inductance they introduce into the lines permits coupling between outputs. Therefore, use of PC boards with premanufactured ground connections is advised to connect the device pins to ground.

However, the optimum solution is to use multi–layer PC boards where different layers are used for the supply rails and interconnections. Even with double–sided boards, placing the power and ground lines on opposite sides of the board whenever possible is recommended. The multi–wire board is a less expensive approach than the multi–layer PC board, while retaining the same noise reduction characteristics. As a rule of thumb, there should be several ground pins per connector to give good ground distribution.

The precautions for ground lines also apply to V_{CC} lines: 1) separate power stabilization for each board; 2) isolate noise sources; and 3) avoid the use of large, single voltage regulators.

After all of these precautions, decoupling is an added measure to reduce supply noise. See the **Decoupling Capacitors** section.

Definitions and Glossary of Terms

HC vs. HCT

ON Semiconductor's High–Speed CMOS is intended to give the designer an alternative to LSTTL. HSCMOS, with the faster speed advantage over metal–gate CMOS (MC14000 series) and the lower power consumption advantage over LSTTL, is an optimum choice for new midrange designs. With the advent of high–speed CMOS microprocessors and memories, the ability to design a 100% CMOS system is now possible.

HCT devices offer a short–term solution to the TTL/NMOS–to–CMOS interface problem. To achieve this interface capability, some CMOS advantages had to be compromised. These compromises include power consumption, operating voltage range, and noise immunity.

In most cases HCT devices are drop–in replacements of TTL devices with significant advantages over the TTL devices. However, in some cases, an equivalent HCT device may not replace a TTL device without some form of circuit modification.

The wise designer uses HCT devices to perform logic level conversions only. In new designs, the designer wants all the advantages of a true CMOS system and designs using only HC devices.

GLOSSARY OF TERMS

C_{in} Input Capacitance — The parasitic capacitance associated with a given input pin.

C_L Load Capacitance — The capacitor value which loads each output during testing and/or evaluation. This capacitance is assumed to be attached to each output in a system. This includes all wiring and stray capacitance.

C_{out} Output Capacitance — The capacitance associated with a three–state output in the high–impedance state.

C_{PD} Power Dissipation Capacitance — Used to determine device dynamic power dissipation, i.e., $P_D = C_{PD}V_{CC}^2f + V_{CC}I_{CC}$. See **POWER SUPPLY SIZING** for a discussion of C_{PD}.

f_{max} Maximum Clock Frequency — The maximum clocking frequency attainable with the following input and output conditions being met:

Input Conditions — (HC) $t_r = t_f$ = 6 ns, voltage swing from GND to V_{CC} with 50% duty cycle. **(HCT)** $t_r = t_f$ = 6 ns, voltage swing from GND to 3.0 V with 50% duty cycle.

Output Conditions — (HC and HCT) waveform must swing from 10% of ($V_{OH} - V_{OL}$) to 90% of ($V_{OH} - V_{OL}$) and be functionally correct under the given load condition: C_L = 50 pF, all outputs.

V_{CC} Positive Supply Voltage — + dc supply voltage (referenced to GND). The voltage range over which ICs are functional.

V_{in} Input Voltage — DC input voltage (referenced to GND).

V_{out} Output Voltage — DC output voltage (referenced to GND).

V_{IH} Minimum High Level Input Voltage — The worst case voltage that is recognized by a device as the HIGH state.

V_{IL} Maximum Low Level Input Voltage — The worst case voltage that is recognized by a device as the LOW state.

V_{OH} Minimum High Level Output Voltage — The worst case high–level voltage at an output for a given output current (I_{out}) and supply voltage (V_{CC}).

V_{OL} Maximum Low Level Output Voltage — The worst case low–level voltage at an output for a given output current (I_{out}) and supply voltage (V_{CC}).

V_{T+} Positive–Going Input Threshold Voltage — The minimum input voltage of a device with hysteresis which is recognized as a high level. (Assumes ramp up from previous low level.)

V_{T-} Negative–Going Input Threshold Voltage — The maximum input voltage of a device with hysteresis which is recognized as a low level. (Assumes ramp down from previous high level).

V_H Hysteresis Voltage — The difference between V_{T+} and V_{T-} of a given device with hysteresis. A measure of noise rejection.

I_{CC} IC Quiescent Supply Current — The current into the V_{CC} pin when the device inputs are static at V_{CC} or GND and outputs are not connected.

ΔI_{CC} Additional Quiescent Supply Current — The current into the V_{CC} pin when one of the device inputs is at 2.4 V with respect to GND and the other inputs are static at V_{CC} or GND. The outputs are not connected.

I_{in} Input Current — The current into an input pin with the respective input forced to V_{CC} or GND. A negative sign indicates current is flowing out of the pin (source). A positive sign or no sign indicates current is flowing into the pin (sink).

I_{out} Output Current — The current out of an output pin. A negative sign indicates current is flowing out of the pin (source). A positive sign or no sign indicates current is flowing into the pin (sink).

I_{IH} Input Current (High) — The input current when the input voltage is forced to a high level.

I_{IL} **Input Current (Low) —** The input current when the input voltage is forced to a low level.

I_{OH} **Output Current (High) —** The output current when the output voltage is at a high level.

I_{OL} **Output Current (Low) —** The output current when the output voltage is at a low level.

I_{OZ} **Three–State Leakage Current —** The current into or out of a three–state output in the high–impedance state with that respective output forced to V_{CC} or GND.

t_{PLH} **Low–to–High Propagation Delay (HC) —** The time interval between the 0.5 V_{CC} level of the controlling input waveform and the 50% level of the output waveform, with the output changing from low level to high level. **(HCT) —** The time interval between the 1.3 V level (with respect to GND) of the controlling input waveform and the 1.3 V level (with respect to GND) of the output waveform, with the output changing from low level to high level.

t_{PHL} **High–to–Low Propagation Delay (HC) —** The time interval between the 0.5 V_{CC} level of the controlling input waveform and the 50% level of the output waveform, with the output changing from high level to low level. **(HCT) —** The time interval between the 1.3 V level (with respect to GND) of the controlling input waveform and the 1.3 V level (with respect to GND) of the output waveform, with the output changing from high level to low level.

t_{PLZ} **Low–Level to High–Impedance Propagation Delay (Disable Time) —** The time interval between the 0.5 V_{CC} level for HC devices (1.3 V with respect to GND for HCT devices) of the controlling input waveform and the 10% level of the output waveform, with the output changing from the low level to high–impedance (off) state.

t_{PHZ} **High–Level to High–impedance Propagation Delay (Disable Time) —** The time interval between the 0.5 V_{CC} level for HC devices (1.3 V with respect to GND for HCT devices) of the controlling input waveform and the 90% level of the output waveform, with the output changing from the high level to high–impedance (off) state.

t_{PZL} **High–Impedance to Low–Level Propagation Delay (Enable Time) —** The time interval between 0.5 V_{CC} level (HC) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% level (HC) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high–impedance (off) state to a low level.

t_{PZH} **High–Impedance to High–Level Propagation Delay (Enable Time) —** The time interval between the 0.5 V_{CC} level (HC) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% level (HC) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high–impedance (off) state to a high level.

t_{TLH} **Output Low–to–High Transition Time —** The time interval between the 10% and 90% voltage levels of the rising edge of a switching output.

t_{THL} **Output High–to–Low Transition Time —** The time interval between the 90% and 10% voltage levels of the falling edge of a switching output.

t_{su} **Setup Time —** The time interval immediately preceeding the active transition of a clock or latch enable input, during which the data to be recognized must be maintained (valid) at the input to ensure proper recognition. A negative setup time indicates that the data at the input may be applied sometime after the active clock or latch transition and still be recognized. For HC devices, the setup time is measured from the 50% level of the data waveform to the 50% level of the clock or latch input waveform. For HCT devices, the setup time is measured from the 1.3 V level (with respect to GND) of the data waveform to the 1.3 V level (with respect to GND) of the clock or latch input waveform.

t_h **Hold Time —** The time interval immediately following the active transition of a clock or latch enable input, during which the data to be recognized must be maintained (valid) at the input to ensure proper recognition. A negative hold time indicates that the data at the input may be changed prior to the active clock or latch transition and still be recognized. For HC devices, the hold time is measured from the 50% level of the clock or latch input waveform to the 50% level of the data waveform. For HCT devices, the hold time is measured from the 1.3 V level (with respect to GND) of the clock or latch input waveform to the 1.3 V level (with respect to GND) of the data waveform.

t_{rec} **Recovery Time (HC) —** The time interval between the 50% level of the transition from active to inactive state of an asynchronous control input and the 50% level of the active clock or latch enable edge required to guarantee proper operation of a device. **(HCT) —** The time interval between the 1.3 V level (with respect to GND) of the transition from active to inactive state of an asynchronous control input and the 1.3 V level (with respect to GND) of the active clock or latch edge required to guarantee proper operation of a logic device.

t_W **Pulse Width (HC) —** The time interval between 50% levels of an input pulse required to guarantee proper operation of a logic device. **(HCT) —** The time interval between 1.3 V levels (with respect to GND) of an input pulse required to guarantee proper operation of a logic device.

t_r **Input Rise Time (HC) —** The time interval between the 10% and 90% voltage levels on the rising edge of an input signal. **(HCT) —** The time interval between the 0.3 V level and 2.7 V level (with respect to GND) on the rising edge of an input signal.

t_f **Input Fall Time (HC) —** The time interval between the 90% and 10% voltage levels on the falling edge of an input signal. **(HCT) —** The time interval between the 2.7 V level and 0.3 V level (with respect to GND) on the falling edge of an input signal.

APPLICATIONS ASSISTANCE FORM

In the event that you have any questions or concerns about the performance of any ON Semiconductor device listed in this catalog, please contact your local ON Semiconductor sales office or the ON Semiconductor Help line for assistance. If further information is required, you can request direct factory assistance.

Please fill out as much of the form as is possible if you are contacting ON Semiconductor for assistance or are sending devices back to ON Semiconductor for analysis. Your information can greatly improve the accuracy of analysis and can dramatically improve the correlation response and resolution time.

Items 4 thru 8 of the following form contains important questions that can be invaluable in analyzing application or device problems. It can be used as a self-help diagnostic guideline or for a baseline of information gathering to begin a dialog with ON Semiconductor representatives.

ON Semiconductor Device Correlation/Component Analysis Request Form

— Please fill out entire form and return with devices to ON Semiconductor, R&QA Dept., 5005 E. McDowell, Phoenix, AZ 85008.

1) Name of Person Requesting Correlation: _____

   Phone No: _____ Job Title: _____ Company: _____

2) Alternate Contact: _____ Phone/Position: _____

3) Device Type (user part number): _____

4) Industry Generic Device Type: _____

5) # of devices tested/sampled: _____

   # of devices in question*: _____

   # returned for correlation: _____

   * In the event of 100% failure, does Customer have other date codes of ON Semiconductor devices that pass inspection?

     Yes _____ No _____ Please specify passing date code(s) if applicable _____

   If none, does customer have viable alternate vendor(s) for device type?

     Yes _____ No _____ Alternate vendor's name _____

6) Date code(s) and Serial Number(s) of devices returned for correlation — If possible, please provide one or two "good" units (ON Semiconductor's and/or other vendor) for comparison: _____

7) Describe USER process that device(s) are questionable in:

   _____ Incoming component inspection {test system = ?}: _____

   _____ Design prototyping: _____

   _____ Board test/burn-in: _____

   _____ Other (please describe): _____

   _____

8) Please describe the device correlation operating parameters as completely as possible for device(s) in question:

> Describe all pin conditions (e.g. floating, high, low, under test, stimulated but not under test, whatever ...), including any input or output loading conditions (resistors, caps, clamps, driving devices or devices being driven ...). Potentially critical information includes:

   _____ Input waveform timing relationships
   _____ Input edge rates
   _____ Input Overshoot or Undershoot — Magnitude and Duration
   _____ Output Overshoot or Undershoot — Magnitude and Duration

> Photographs, plots or sketches of relevent inputs and outputs with voltages and time divisions clearly identified for all waveforms are greatly desirable.

> V_{CC} and Ground waveforms should be carefully described as these characteristics vary greatly between applications and test systems. Dynamic characteristics of Ground and V_{CC} during device switching can dramatically effect input and internal operating levels. Ground & V_{CC} measurements should be made as physically close to the device in question as possible.

> Are there specific circumstances that seem to make the questionable unit(s) worse? Better?

   _____ Temperature _____

   _____ V_{CC} _____

   _____ Input rise/fall time _____

   _____ Output loading (current/capacitance) _____

   _____ Others _____

> ATE functional data should include pattern with decoding key and critical parameters such as V_{CC}, input voltages, Func step rate, voltage expected, time to measure.

CHAPTER 3
Data Sheets

MC74HC00A

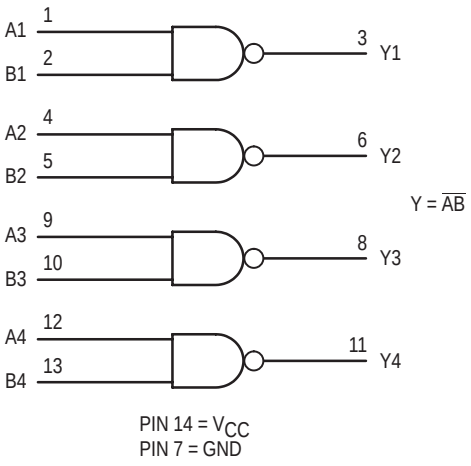
Quad 2-Input NAND Gate

High–Performance Silicon–Gate CMOS

The MC74HC00A is identical in pinout to the LS00. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

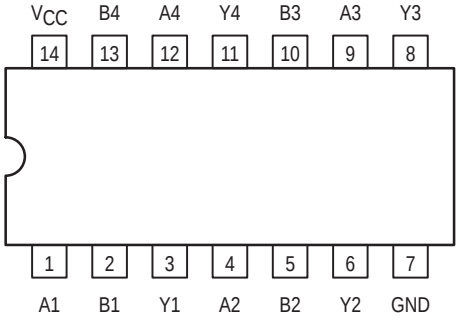
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2 to 6V
- Low Input Current: 1μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 32 FETs or 8 Equivalent Gates

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

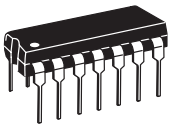
Pinout: 14–Lead Packages (Top View)



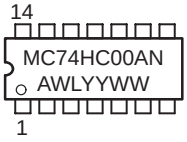
ON Semiconductor

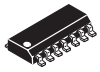
http://onsemi.com

MARKING DIAGRAMS

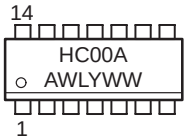


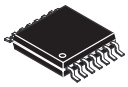
PDIP–14
N SUFFIX
CASE 646





SOIC–14
D SUFFIX
CASE 751A





TSSOP–14
DT SUFFIX
CASE 948G

A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

ORDERING INFORMATION

Device	Package	Shipping
MC74HC00AN	PDIP–14	2000 / Box
MC74HC00AD	SOIC–14	55 / Rail
MC74HC00ADR2	SOIC–14	2500 / Reel
MC74HC00ADT	TSSOP–14	96 / Rail
MC74HC00ADTR2	TSSOP–14	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1V or V_{CC} –0.1V $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1V or V_{CC} – 0.1V $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} =V_{IH} or V_{IL} $\|I_{out}\| \le 2.4mA$ $\|I_{out}\| \le 4.0mA$ $\|I_{out}\| \le 5.2mA$	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 2.4mA$ $\|I_{out}\| \le 4.0mA$ $\|I_{out}\| \le 5.2mA$	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0μA	6.0	1.0	10	40	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V, V_{EE} = 0 V	
C_{PD}	Power Dissipation Capacitance (Per Buffer)*	22	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

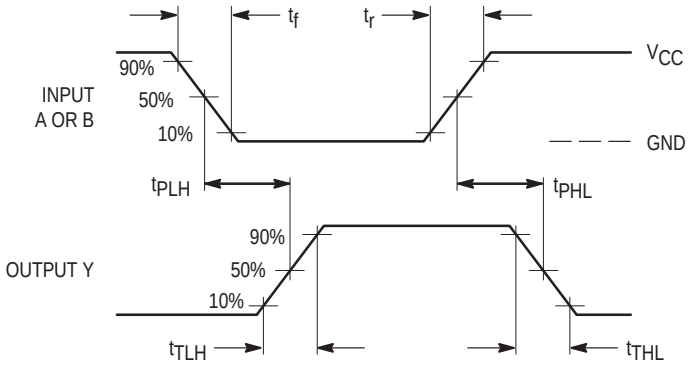
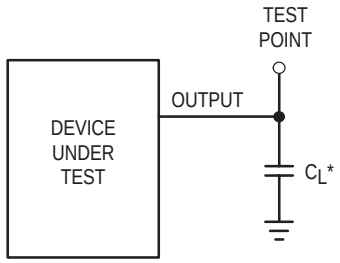


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

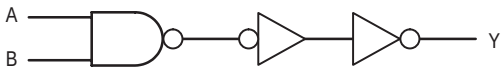


Figure 3. Expanded Logic Diagram
(1/4 of the Device)

MC74HC02A

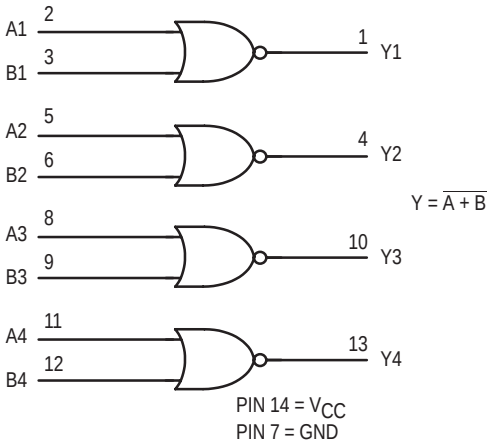
Quad 2-Input NOR Gate

High–Performance Silicon–Gate CMOS

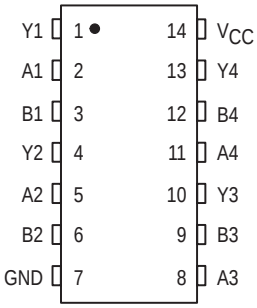
The MC74HC02A is identical in pinout to the LS02. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 40 FETs or 10 Equivalent Gates

LOGIC DIAGRAM



PIN ASSIGNMENT



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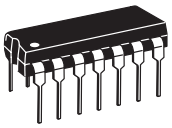
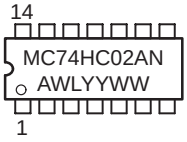
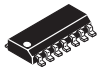
MARKING DIAGRAMS

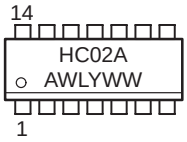


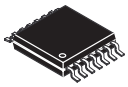
PDIP–14
N SUFFIX
CASE 646





SOIC–14
D SUFFIX
CASE 751A





TSSOP–14
DT SUFFIX
CASE 948G

A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	L
H	L	L
H	H	L

ORDERING INFORMATION

Device	Package	Shipping
MC74HC02AN	PDIP–14	2000 / Box
MC74HC02AD	SOIC–14	55 / Rail
MC74HC02ADR2	SOIC–14	2500 / Reel
MC74HC02ADT	TSSOP–14	96 / Rail
MC74HC02ADTR2	TSSOP–14	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	 260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1) V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 4.0 mA $\|I_{out}\|$ ≤ 5.2 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.7 5.2	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 2.4$ mA $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $\|I_{out}\| = 0$ μA	6.0	1.0	10	40	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, $V_{CC} = 5.0$ V	
C_{PD}	Power Dissipation Capacitance (Per Gate)*	22	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

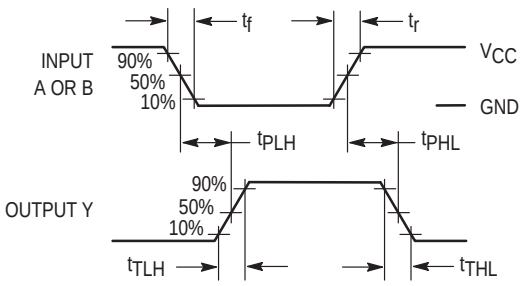
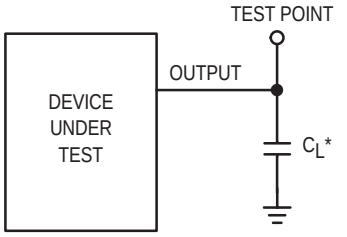


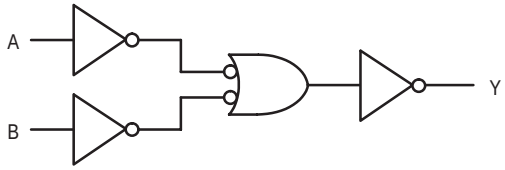
Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM
(1/4 OF THE DEVICE)



MC74HC03A

Quad 2-Input NAND Gate with Open-Drain Outputs

High–Performance Silicon–Gate CMOS

The MC74HC03A is identical in pinout to the LS03. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC03A NAND gate has, as its outputs, a high–performance MOS N–Channel transistor. This NAND gate can, therefore, with a suitable pullup resistor, be used in wired–AND applications. Having the output characteristic curves given in this data sheet, this device can be used as an LED driver or in any other application that only requires a sinking current.

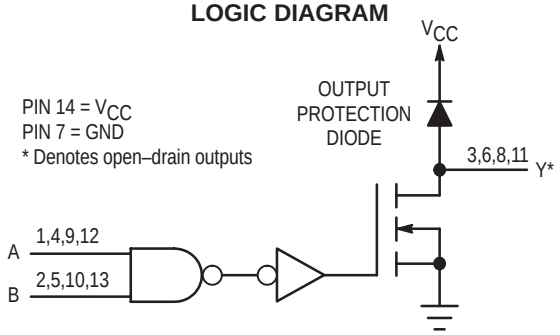
- Output Drive Capability: 10 LSTTL Loads With Suitable Pullup Resistor
- Outputs Directly Interface to CMOS, NMOS and TTL
- High Noise Immunity Characteristic of CMOS Devices
- Operating Voltage Range: 2 to 6V
- Low Input Current: 1μA
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 28 FETs or 7 Equivalent Gates

DESIGN GUIDE

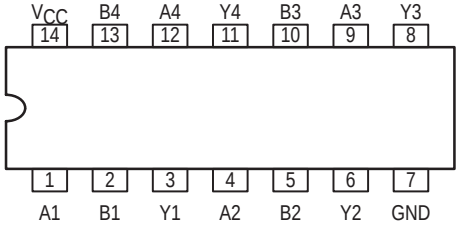
Criteria	Value	Unit
Internal Gate Count*	7.0	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	0.0075	pJ

* Equivalent to a two–input NAND gate

LOGIC DIAGRAM



Pinout: 14–Lead Packages (Top View)



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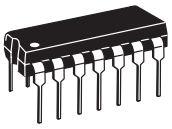
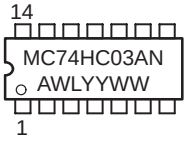
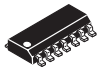
MARKING DIAGRAMS

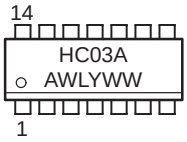


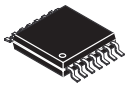
PDIP–14
N SUFFIX
CASE 646





SOIC–14
D SUFFIX
CASE 751A





TSSOP–14
DT SUFFIX
CASE 948G

A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	Z
L	H	Z
H	L	Z
H	H	L

Z = High Impedance

ORDERING INFORMATION

Device	Package	Shipping
MC74HC03AN	PDIP–14	2000 / Box
MC74HC03AD	SOIC–14	55 / Rail
MC74HC03ADR2	SOIC–14	2500 / Reel
MC74HC03ADT	TSSOP–14	96 / Rail
MC74HC03ADTR2	TSSOP–14	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1) V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit –55 to 25°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1V or V_{CC} –0.1V $\|I_{out}\|$ ≤ 20μA	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1V or V_{CC} – 0.1V $\|I_{out}\|$ ≤ 20μA	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
V_{OL}	Maximum Low–Level Output Voltage	V_{out} = 0.1V or V_{CC} – 0.1V $\|I_{out}\|$ ≤ 20μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 2.4mA $\|I_{out}\|$ ≤ 4.0mA $\|I_{out}\|$ ≤ 5.2mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0μA	6.0	1.0	10	40	μA
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	6.0	±0.5	±5.0	±10	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLZ}, t_{PZL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 3.0 4.5 6.0	120 45 24 20	150 60 30 26	180 75 36 31	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)		10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V, V_{EE} = 0 V	
C_{PD}	Power Dissipation Capacitance (Per Buffer)*	8.0	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

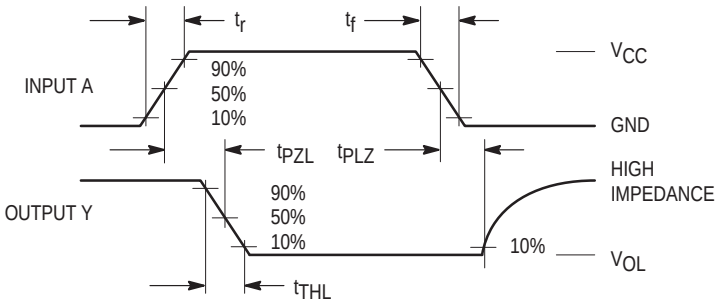
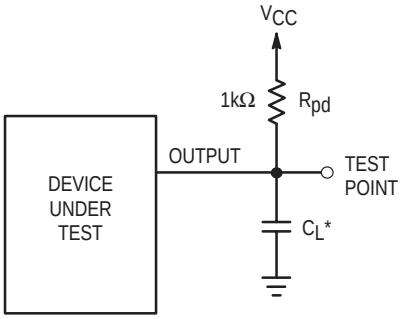
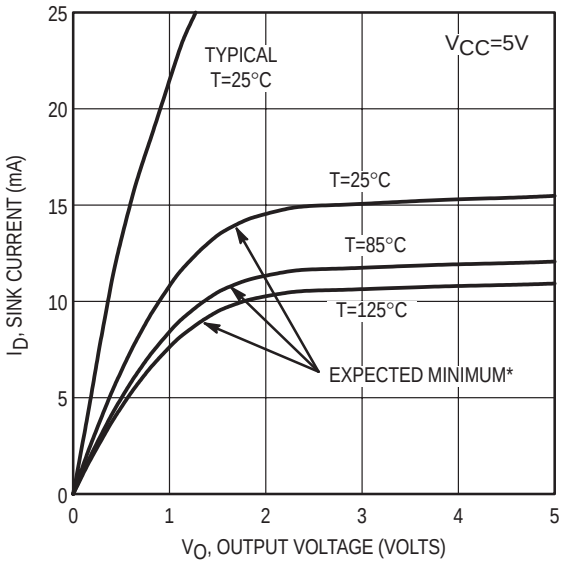


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit



*The expected minimum curves are not guarantees, but are design aids.

Figure 3. Open–Drain Output Characteristics

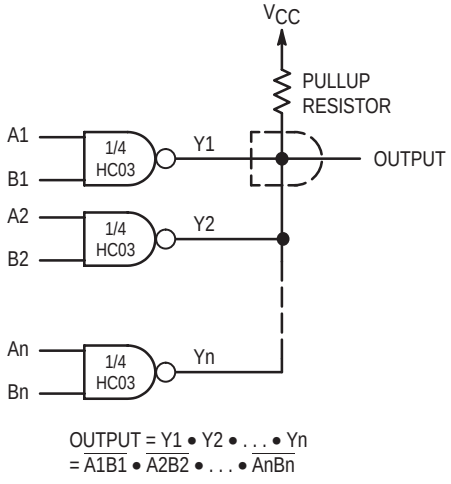


Figure 4. Wired AND

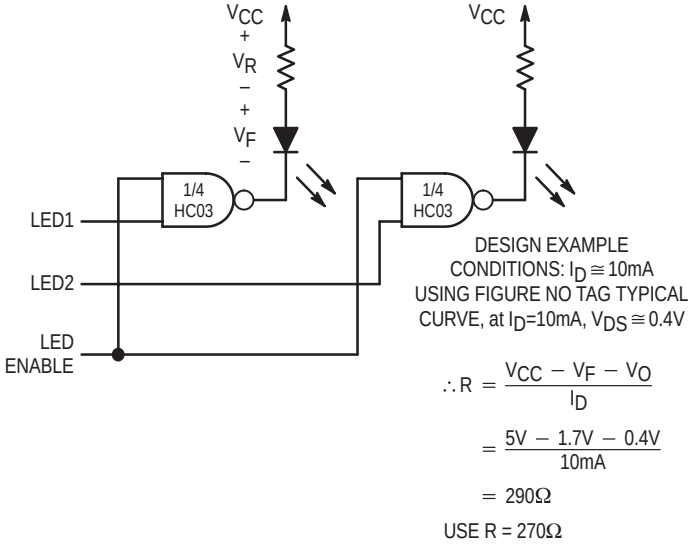


Figure 5. LED Driver With Blanking

MC74HC04A

Hex Inverter

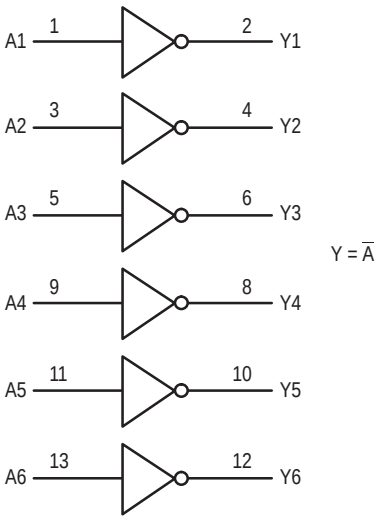
High–Performance Silicon–Gate CMOS

The MC74HC04A is identical in pinout to the LS04 and the MC14069. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

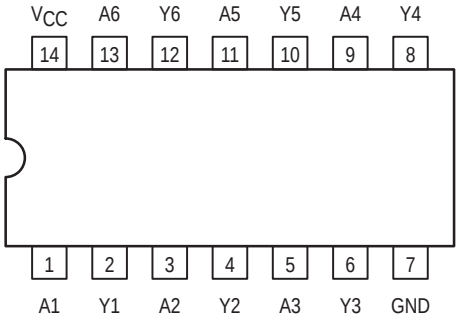
The device consists of six three–stage inverters.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2 to 6V
- Low Input Current: 1μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 36 FETs or 9 Equivalent Gates

LOGIC DIAGRAM



Pinout: 14–Lead Packages (Top View)



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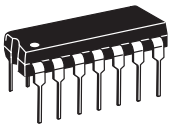
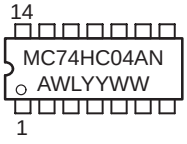
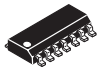
MARKING DIAGRAMS

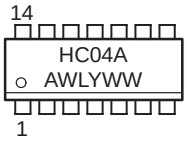


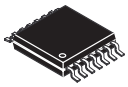
PDIP–14
N SUFFIX
CASE 646



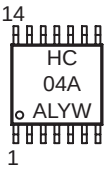


SOIC–14
D SUFFIX
CASE 751A





TSSOP–14
DT SUFFIX
CASE 948G



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

FUNCTION TABLE

Inputs	Outputs
A	**Y**
L	H
H	L

ORDERING INFORMATION

Device	Package	Shipping
MC74HC04AN	PDIP–14	2000 / Box
MC74HC04AD	SOIC–14	55 / Rail
MC74HC04ADR2	SOIC–14	2500 / Reel
MC74HC04ADT	TSSOP–14	96 / Rail
MC74HC04ADTR2	TSSOP–14	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1V or V_{CC} –0.1V $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1V or V_{CC} – 0.1V $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} =V_{IH} or V_{IL} $\|I_{out}\| \le 2.4mA$ $\|I_{out}\| \le 4.0mA$ $\|I_{out}\| \le 5.2mA$	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 2.4mA$ $\|I_{out}\| \le 4.0mA$ $\|I_{out}\| \le 5.2mA$	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0μA	6.0	1.0	10	40	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC CHARACTERISTICS (C_L = 50pF, Input t_r = t_f = 6ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Inverter)*	20	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

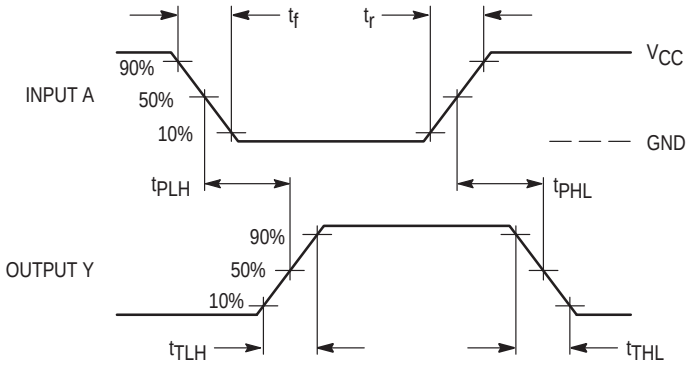
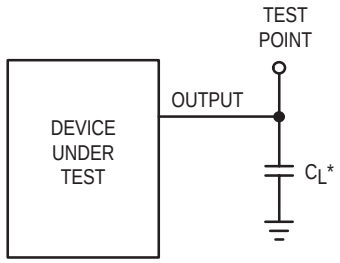


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

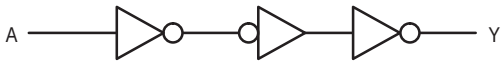


Figure 3. Expanded Logic Diagram
(1/6 of the Device Shown)

MC74HCT04A

Hex Inverter

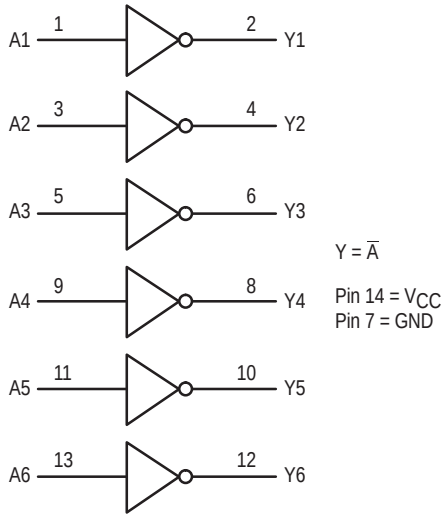
With LSTTL–Compatible Inputs
High–Performance Silicon–Gate CMOS

The MC74HCT04A may be used as a level converter for interfacing TTL or NMOS outputs to High–Speed CMOS inputs.

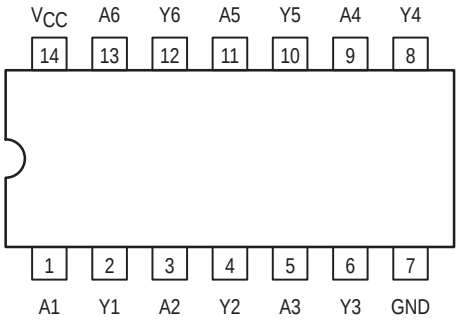
The HCT04A is identical in pinout to the LS04.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS–Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5V
- Low Input Current: 1μA
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 48 FETs or 12 Equivalent Gates

LOGIC DIAGRAM



Pinout: 14–Lead Packages (Top View)



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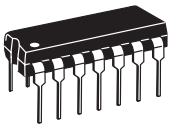
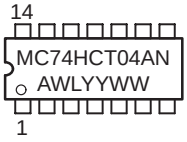
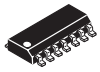
MARKING DIAGRAMS

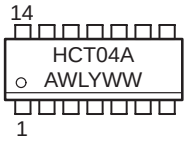


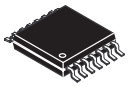
PDIP–14
N SUFFIX
CASE 646



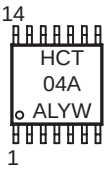


SOIC–14
D SUFFIX
CASE 751A





TSSOP–14
DT SUFFIX
CASE 948G



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

FUNCTION TABLE

Inputs	Outputs
A	Y
L	H
H	L

ORDERING INFORMATION

Device	Package	Shipping
MC74HCT04AN	PDIP–14	2000 / Box
MC74HCT04AD	SOIC–14	55 / Rail
MC74HCT04ADR2	SOIC–14	2500 / Reel
MC74HCT04ADT	TSSOP–14	96 / Rail
MC74HCT04ADTR2	TSSOP–14	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature Range, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise/Fall Time (Figure 1)	0	500	ns

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1V $\|I_{out}\| \le 20\mu A$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage	$V_{out} = V_{CC} - 0.1V$ $\|I_{out}\| \le 20\mu A$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage	$V_{in} = V_{IL}$ $\|I_{out}\| \le 20\mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{in} = V_{IL}$ $\|I_{out}\| \le 4.0mA$	4.5	3.98	3.84	3.70	
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IH}$ $\|I_{out}\| \le 20\mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{in} = V_{IH}$ $\|I_{out}\| \le 4.0mA$	4.5	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	5.5	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0μA	5.5	1	10	40	μA

				≥ –55°C	25 to 125°C	
ΔI_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4V, Any One Input $V_{in} = V_{CC}$ or GND, Other Inputs I_{out} = 0μA	5.5	2.9	2.4	mA

1. Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).
2. Total Supply Current = $I_{CC} + \Sigma\Delta I_{CC}$.

AC CHARACTERISTICS (V_{CC} = 5.0V ±10%, C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	Guaranteed Limit			Unit
		–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	15 17	19 21	22 26	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	15	19	22	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Inverter)*	22	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

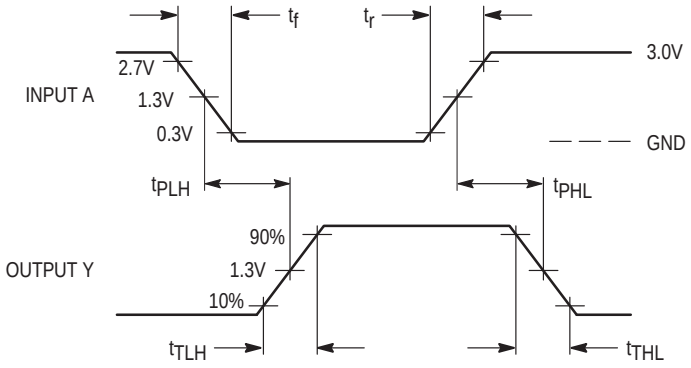
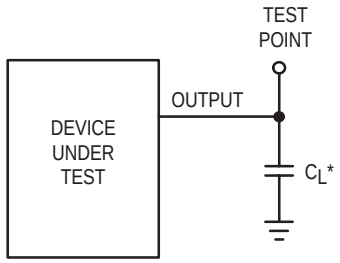


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

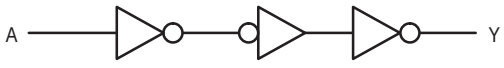


Figure 3. Expanded Logic Diagram
(1/6 of the Device Shown)

MC74HCU04A

Hex Unbuffered Inverter

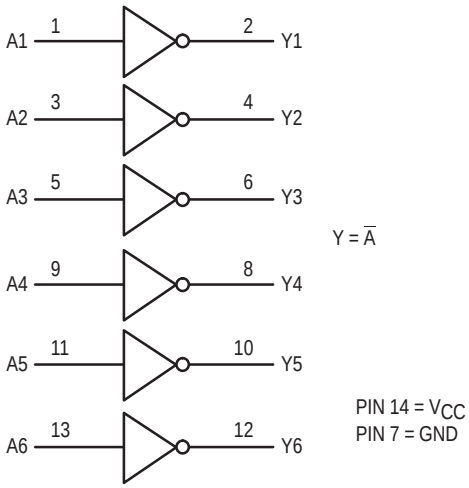
High–Performance Silicon–Gate CMOS

The MC74HCU04A is identical in pinout to the LS04 and the MC14069UB. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six single–stage inverters. These inverters are well suited for use as oscillators, pulse shapers, and in many other applications requiring a high–input impedance amplifier. For digital applications, the HC04A is recommended.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V; 2.5 to 6 V in Oscillator Configurations
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 12 FETs or 3 Equivalent Gates

LOGIC DIAGRAM



FUNCTION TABLE

Inputs A	Outputs Y
L	H
H	L

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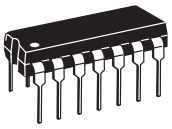
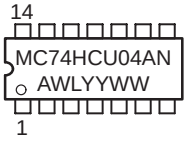
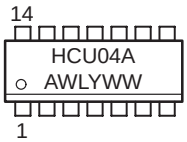
MARKING DIAGRAMS

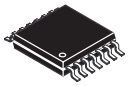


PDIP–14
N SUFFIX
CASE 646

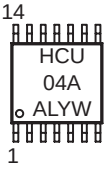


SOIC–14
D SUFFIX
CASE 751A



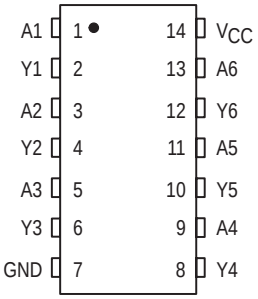


TSSOP–14
DT SUFFIX
CASE 948G



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HCU04AN	PDIP–14	2000 / Box
MC74HCU04AD	SOIC–14	55 / Rail
MC74HCU04ADR2	SOIC–14	2500 / Reel
MC74HCU04ADT	TSSOP–14	96 / Rail
MC74HCU04ADTR2	TSSOP–14	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: –10mW/°C from 65° to 125°C
SOIC Package: –7mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	No Limit	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.5 V* $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.7 2.5 3.6 4.8	1.7 2.5 3.6 4.8	l.7 2.5 3.6 4.8	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = V_{CC} – 0.5 V* $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.3 0.5 0.8 1.1	0.3 0.5 0.8 1.1	0.3 0.5 0.8 1.1	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = GND $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.8 4.0 5.5	1.8 4.0 5.5	1.8 4.0 5.5	V
		V_{in} = GND $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 4.0 mA $\|I_{out}\|$ ≤ 5.2 mA	3.0 4.5 6.0	2.36 3.86 5.36	2.26 3.76 5.26	2.20 3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{CC} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.2 0.5 0.5	0.2 0.5 0.5	0.2 0.5 0.5	V
		V_{in} = V_{CC} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 4.0 mA $\|I_{out}\|$ ≤ 5.2 mA	3.0 4.5 6.0	0.32 0.32 0.32	0.32 0.37 0.37	0.32 0.40 0.40	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0 μA	6.0	1	10	40	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).
*For V_{CC} = 2.0 V, V_{out} = 0.2 V or V_{CC} – 0.2 V.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0 3.0 4.5 6.0	70 40 14 12	90 45 18 15	105 50 21 18	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Inverter)*	15	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

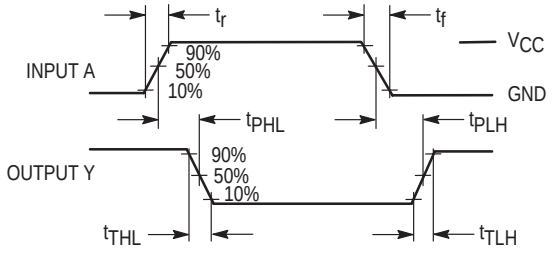
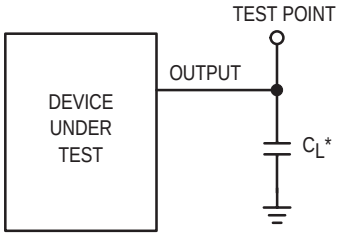


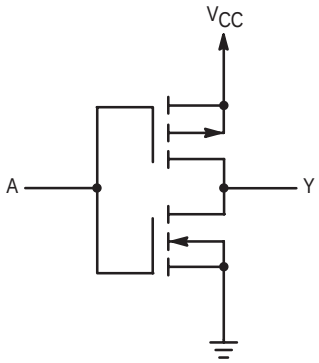
Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

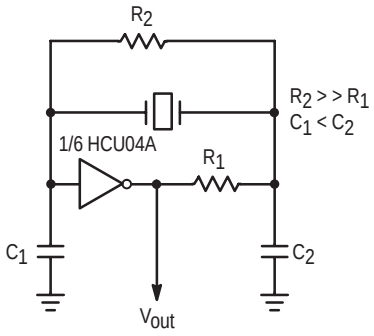
Figure 2. Test Circuit

LOGIC DETAIL
(1/6 of Device Shown)

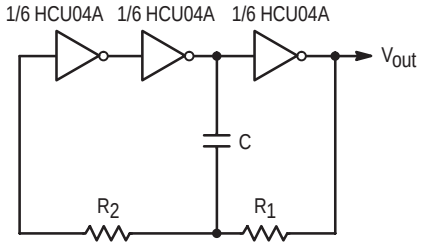


TYPICAL APPLICATIONS

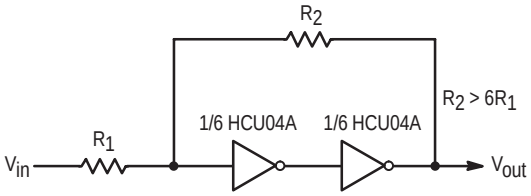
Crystal Oscillator



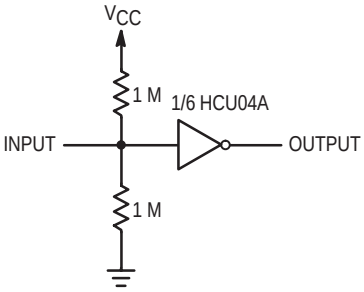
Stable RC Oscillator



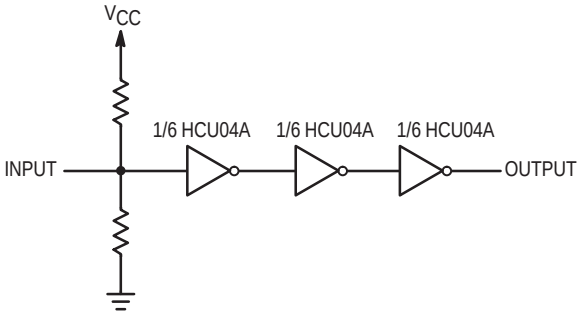
Schmitt Trigger



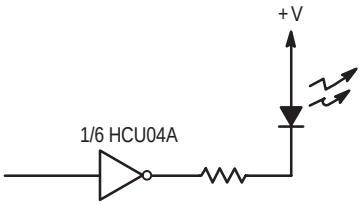
High Input Impedance Single–Stage Amplifier with a 2 to 6 V Supply Range



Multi–Stage Amplifier



LED Driver



For reduced power supply current, use high–efficiency LEDs such as the Hewlett–Packard HLMP series or equivalent.

MC74HC08A

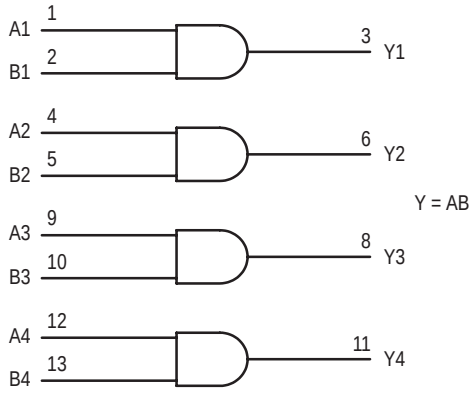
Quad 2-Input AND Gate

High–Performance Silicon–Gate CMOS

The MC74HC08A is identical in pinout to the LS08. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

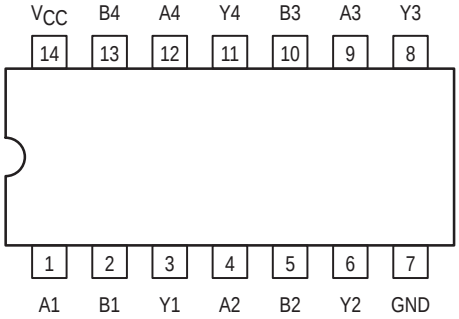
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2 to 6V
- Low Input Current: 1μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 24 FETs or 6 Equivalent Gates

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

Pinout: 14–Lead Packages (Top View)



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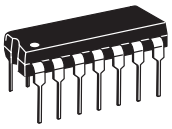
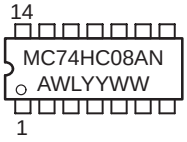
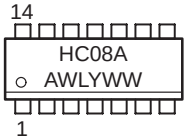
MARKING DIAGRAMS

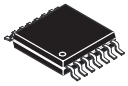


PDIP–14
N SUFFIX
CASE 646



SOIC–14
D SUFFIX
CASE 751A





TSSOP–14
DT SUFFIX
CASE 948G

A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

ORDERING INFORMATION

Device	Package	Shipping
MC74HC08AN	PDIP–14	2000 / Box
MC74HC08AD	SOIC–14	55 / Rail
MC74HC08ADR2	SOIC–14	2500 / Reel
MC74HC08ADT	TSSOP–14	96 / Rail
MC74HC08ADTR2	TSSOP–14	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	 260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1V or V_{CC} –0.1V $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1V or V_{CC} – 0.1V $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} =V_{IH} or V_{IL} $\|I_{out}\| \le 2.4mA$ $\|I_{out}\| \le 4.0mA$ $\|I_{out}\| \le 5.2mA$	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 2.4mA$ $\|I_{out}\| \le 4.0mA$ $\|I_{out}\| \le 5.2mA$	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0μA	6.0	1.0	10	40	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC CHARACTERISTICS (C_L = 50pF, Input t_r = t_f = 6ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V, V_{EE} = 0 V	
C_{PD}	Power Dissipation Capacitance (Per Buffer)*	20	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

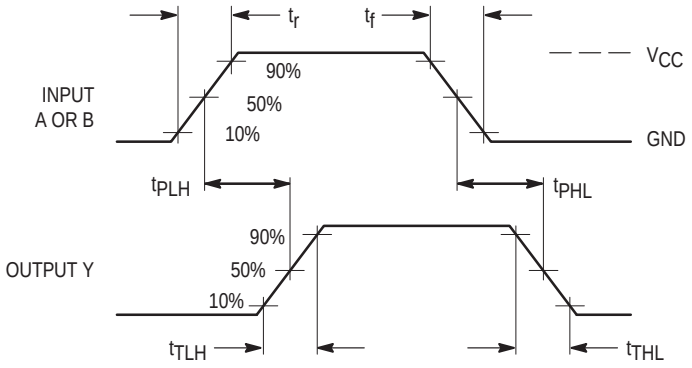
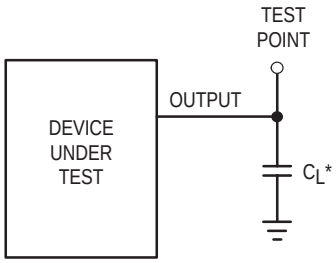


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

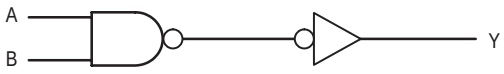


Figure 3. Expanded Logic Diagram
(1/4 of the Device)

MC74HC14A

Hex Schmitt-Trigger Inverter

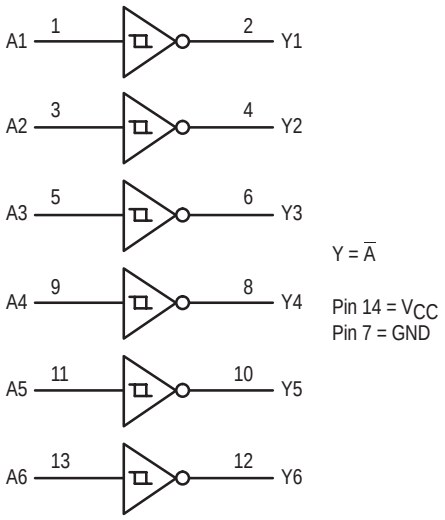
High–Performance Silicon–Gate CMOS

The MC74HC14A is identical in pinout to the LS14, LS04 and the HC04. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

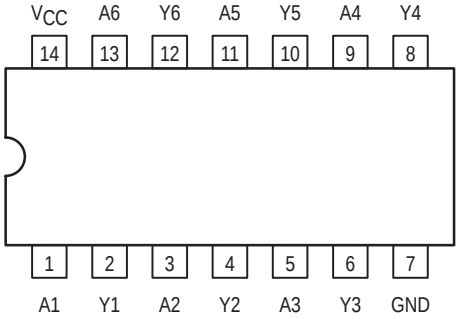
The HC14A is useful to “square up” slow input rise and fall times. Due to hysteresis voltage of the Schmitt trigger, the HC14A finds applications in noisy environments.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2 to 6V
- Low Input Current: 1μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 60 FETs or 15 Equivalent Gates

LOGIC DIAGRAM



Pinout: 14–Lead Packages (Top View)



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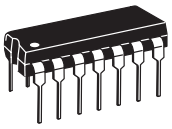
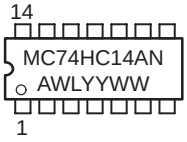
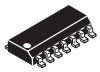
MARKING DIAGRAMS

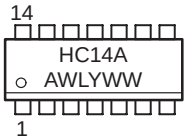


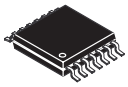
PDIP–14
N SUFFIX
CASE 646



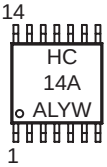


SOIC–14
D SUFFIX
CASE 751A





TSSOP–14
DT SUFFIX
CASE 948G



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

FUNCTION TABLE

Inputs	Outputs
A	**Y**
L	H
H	L

ORDERING INFORMATION

Device	Package	Shipping
MC74HC14AN	PDIP–14	2000 / Box
MC74HC14AD	SOIC–14	55 / Rail
MC74HC14ADR2	SOIC–14	2500 / Reel
MC74HC14ADT	TSSOP–14	96 / Rail
MC74HC14ADTR2	TSSOP–14	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature Range, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise/Fall Time (Figure 1) V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	No Limit* No Limit* No Limit*	ns

*When V_{in} = 50% V_{CC}, I_{CC} > 1mA

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{T+} max	Maximum Positive–Going Input Threshold Voltage (Figure 3)	V_{out} = 0.1V $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	1.50 2.15 3.15 4.20	1.50 2.15 3.15 4.20	1.50 2.15 3.15 4.20	V
V_{T+} min	Minimum Positive–Going Input Threshold Voltage (Figure 3)	V_{out} = 0.1V $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	1.0 1.5 2.3 3.0	0.95 1.45 2.25 2.95	0.95 1.45 2.25 2.95	V
V_{T-} max	Maximum Negative–Going Input Threshold Voltage (Figure 3)	$V_{out} = V_{CC} - 0.1V$ $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	0.9 1.4 2.0 2.6	0.95 1.45 2.05 2.65	0.95 1.45 2.05 2.65	V
V_{T-} min	Minimum Negative–Going Input Threshold Voltage (Figure 3)	$V_{out} = V_{CC} - 0.1V$ $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	0.3 0.5 0.9 1.2	0.3 0.5 0.9 1.2	0.3 0.5 0.9 1.2	V
$V_H$max Note 2	Maximum Hysteresis Voltage (Figure 3)	V_{out} = 0.1V or V_{CC} – 0.1V $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	1.20 1.65 2.25 3.00	1.20 1.65 2.25 3.00	1.20 1.65 2.25 3.00	V
$V_H$min Note 2	Minimum Hysteresis Voltage (Figure 3)	V_{out} = 0.1V or V_{CC} – 0.1V $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	0.20 0.25 0.40 0.50	0.20 0.25 0.40 0.50	0.20 0.25 0.40 0.50	V
V_{OH}	Minimum High–Level Output Voltage	$V_{in} \le V_{T-}$ min $\|I_{out}\| \le 20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} \le V_{T-}$ min $\|I_{out}\| \le 2.4mA$ $\|I_{out}\| \le 4.0mA$ $\|I_{out}\| \le 5.2mA$	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} \ge V_{T+}$ max $\|I_{out}\| \le 20\mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} \ge V_{T+}$ max $\|I_{out}\| \le 2.4mA$ $\|I_{out}\| \le 4.0mA$ $\|I_{out}\| \le 5.2mA$	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0μA	6.0	1.0	10	40	μA

1. Information on typical parametric values along with frequency or heavy load considerations can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).
2. $V_H$min > (V_{T+} min) – (V_{T-} max); $V_H$max = (V_{T+} max) – (V_{T-} min).

AC CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Inverter)*	22	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

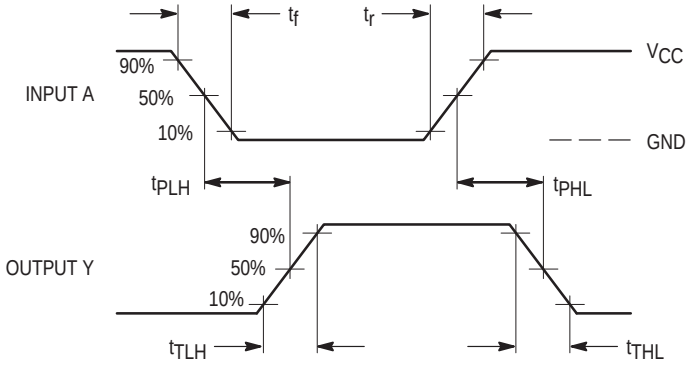
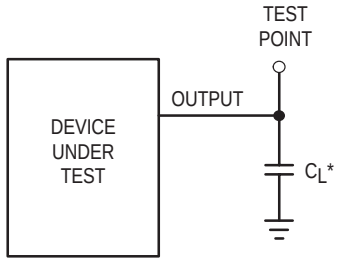


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

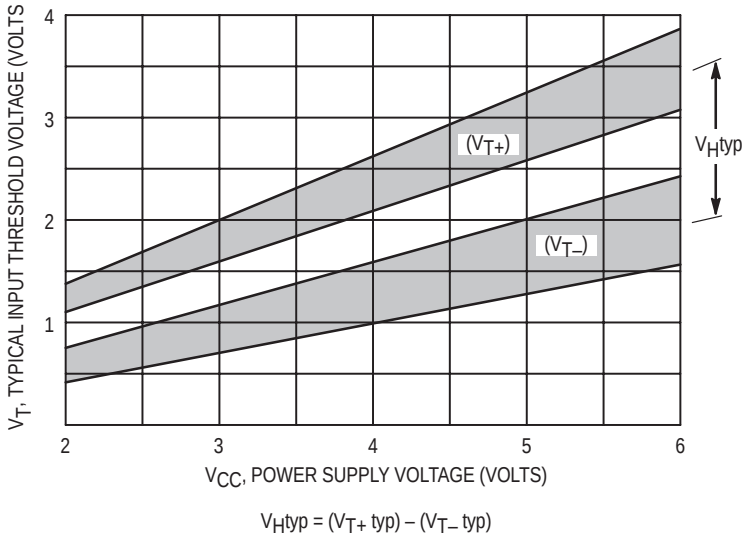


Figure 3. Typical Input Threshold, V_{T+}, V_{T-} versus Power Supply Voltage

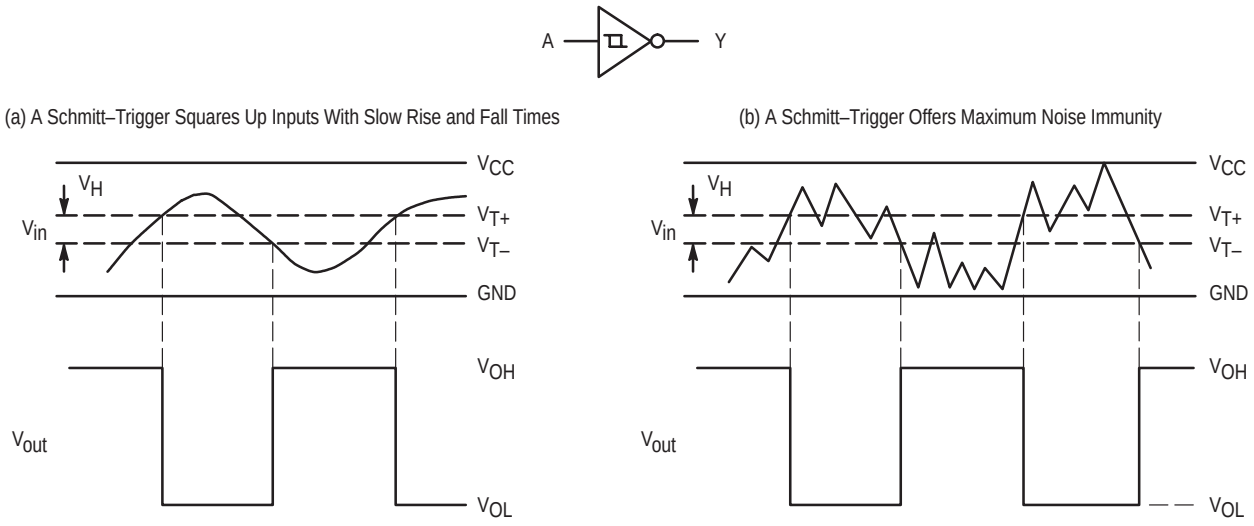


Figure 4. Typical Schmitt–Trigger Applications

MC74HCT14A

Hex Schmitt–Trigger Inverter with LSTTL Compatible Inputs

High–Performance Silicon–Gate CMOS

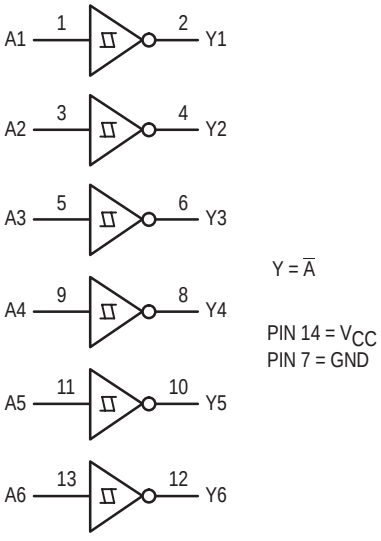
The MC74HCT14A may be used as a level converter for interfacing TTL or NMOS outputs to high–speed CMOS inputs.

The HCT14A is identical in pinout to the LS14.

The HCT14A is useful to “square up” slow input rise and fall times. Due to the hysteresis voltage of the Schmitt trigger, the HCT14A finds applications in noisy environments.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS–Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates

LOGIC DIAGRAM



$Y = \overline{A}$

PIN 14 = V_{CC}
PIN 7 = GND

FUNCTION TABLE

Input A	Output Y
L	H
H	L

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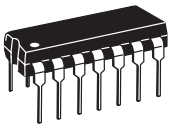
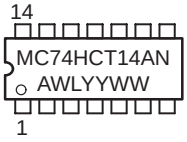
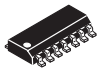
MARKING DIAGRAMS

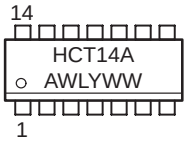


PDIP–14
N SUFFIX
CASE 646



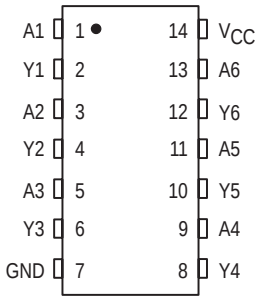


SOIC–14
D SUFFIX
CASE 751A



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HCT14AN	PDIP–14	2000 / Box
MC74HCT14AD	SOIC–14	55 / Rail
MC74HCT14ADR2	SOIC–14	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	 260	°C °C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	*	ns

*No Limit when V_{in} ≈ 50% V_{CC}, I_{CC} > 1 mA.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} Volts	Temperature Limit – 55 to 25°C Min	– 55 to 25°C Max	≤ 85°C Min	≤ 85°C Max	≤ 125°C Min	≤ 125°C Max	Unit
V_{T+} max	Maximum Positive–Going Input Threshold Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5		1.9 2.1		1.9 2.1		1.9 2.1	V
V_{T+} min	Minimum Positive–Going Input Threshold Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	1.2 1.4		1.2 1.4		1.2 1.4		V
$V_{T–}$ max	Maximum Positive–Going Input Threshold Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5		1.2 1.4		1.2 1.4		1.2 1.4	
$V_{T–}$ min	Minimum Positive–Going Input Threshold Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.5 0.6		0.5 0.6		0.5 0.6		
V_H max	Maximum Hysteresis Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5		1.4 1.5		1.4 1.5		1.4 1.5	
V_H min	Minimum Hysteresis Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.4 0.4		0.4 0.4		0.4 0 4		
V_{OH}	Minimum High–Level Output Voltage	V_{in} < VT–min $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	4.4 5.4		4.4 5.4		4.4 5.4		V
		V_{in} < VT–min $\|I_{out}\|$ ≤ 4.0 mA	4.5	3.98		3.84		3.7		

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).
(continued)

DC CHARACTERISTICS (Voltages Referenced to GND) **– continued**

Symbol	Parameter	Test Conditions	V_{CC} Volts	Temperature Limit						Unit
				– 55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} \geq$ VT+max $\|I_{out}\| \leq$ 20 μA	4.5 5.5		0.1 0.1		0.1 0.1		0.1 0.1	V
		$V_{in} \geq$ VT+max $\|I_{out}\| \leq$ 4.0 mA	4.5		0.26		0.33		0.4	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	5.5		± 0.1		± 1.0		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per package)	$V_{in} = V_{CC}$ or GND I_{out} = 0 μA	5.5		1.0		10		40	μA
					≥ – 55°C		25°C to 125°C			
ΔI_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4 V, Any One Input $V_{in} = V_{CC}$ or GND, Other Inputs I_{out} = 0 μA	5.5		2.9		2.4			mA

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Test Conditions		Guaranteed Limit						Unit
				– 55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (L to H)	V_{CC} = 5.0 V ± 10% C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns	Fig. 1 & 2		32		40		48	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time. Any Output	V_{CC} = 5.0 V ± 10% C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns	Fig. 1 & 2		15		19		22	ns

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Inverter)*	32	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

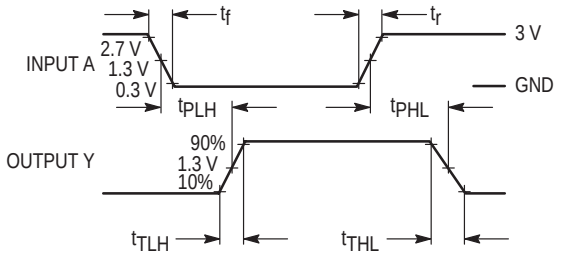
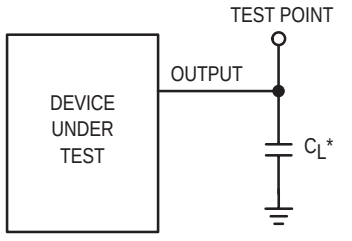


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

MC74HC32A

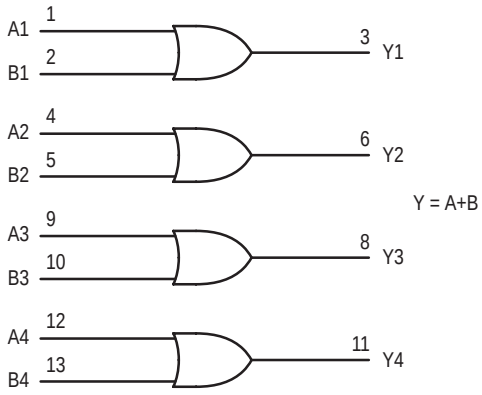
Quad 2-Input OR Gate

High–Performance Silicon–Gate CMOS

The MC74HC32A is identical in pinout to the LS32. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

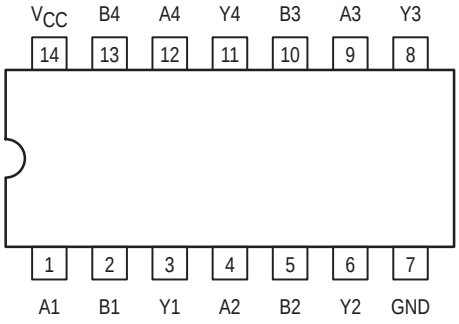
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2 to 6V
- Low Input Current: 1μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 48 FETs or 12 Equivalent Gates

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

Pinout: 14–Lead Packages (Top View)



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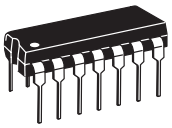
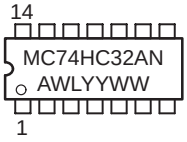
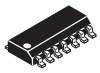
MARKING DIAGRAMS

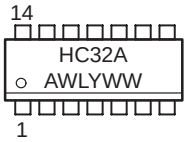


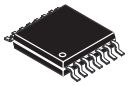
PDIP–14
N SUFFIX
CASE 646



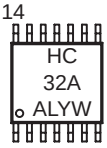


SOIC–14
D SUFFIX
CASE 751A





TSSOP–14
DT SUFFIX
CASE 948G



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	H

ORDERING INFORMATION

Device	Package	Shipping
MC74HC32AN	PDIP–14	2000 / Box
MC74HC32AD	SOIC–14	55 / Rail
MC74HC32ADR2	SOIC–14	2500 / Reel
MC74HC32ADT	TSSOP–14	96 / Rail
MC74HC32ADTR2	TSSOP–14	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1V or V_{CC} –0.1V $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1V or V_{CC} – 0.1V $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} =V_{IH} or V_{IL} $\|I_{out}\| \le 2.4mA$ $\|I_{out}\| \le 4.0mA$ $\|I_{out}\| \le 5.2mA$	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 2.4mA$ $\|I_{out}\| \le 4.0mA$ $\|I_{out}\| \le 5.2mA$	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0μA	6.0	1.0	10	40	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC CHARACTERISTICS (C_L = 50pF, Input t_r = t_f = 6ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V, V_{EE} = 0 V	
C_{PD}	Power Dissipation Capacitance (Per Buffer)*	20	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

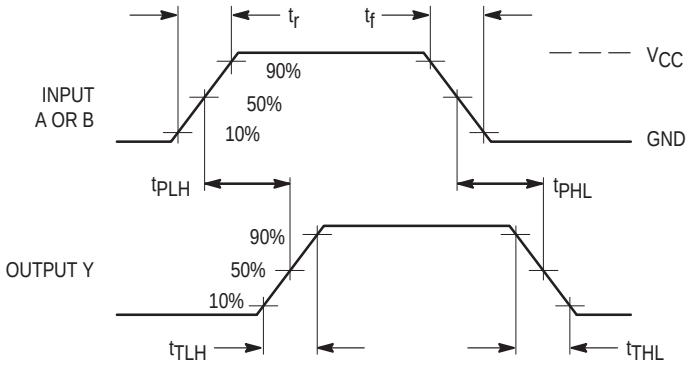
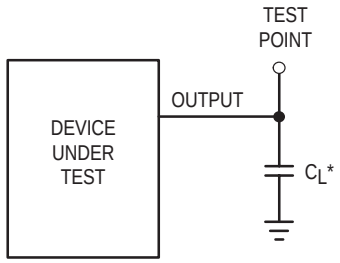


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

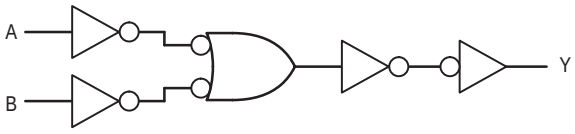


Figure 3. Expanded Logic Diagram
(1/4 of the Device)

MC74HC74A

Dual D Flip-Flop with Set and Reset

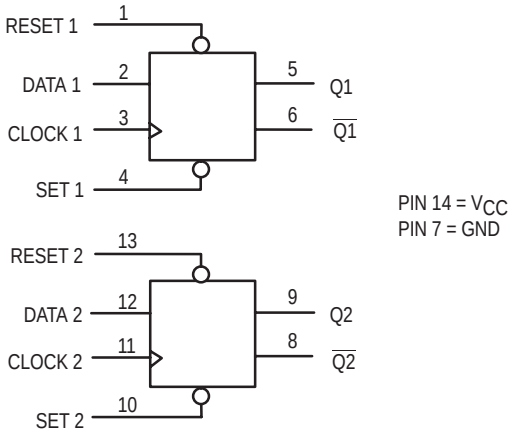
High–Performance Silicon–Gate CMOS

The MC74HC74A is identical in pinout to the LS74. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two D flip–flops with individual Set, Reset, and Clock inputs. Information at a D–input is transferred to the corresponding Q output on the next positive going edge of the clock input. Both Q and $\overline{Q}$ outputs are available from each flip–flop. The Set and Reset inputs are asynchronous.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 128 FETs or 32 Equivalent Gates

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

FUNCTION TABLE

Inputs				Outputs	
Set	Reset	Clock	Data	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H	↓	X	No Change	

*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

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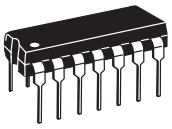
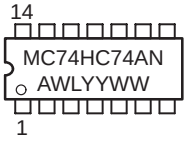
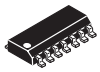
MARKING DIAGRAMS

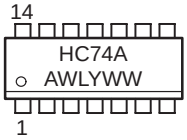


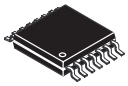
PDIP–14
N SUFFIX
CASE 646





SOIC–14
D SUFFIX
CASE 751A

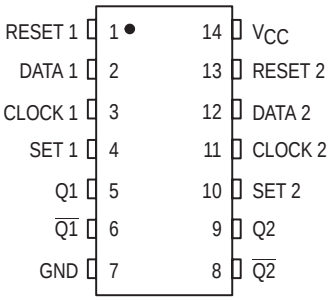




TSSOP–14
DT SUFFIX
CASE 948G

A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HC74AN	PDIP–14	2000 / Box
MC74HC74AD	SOIC–14	55 / Rail
MC74HC74ADR2	SOIC–14	2500 / Reel
MC74HC74ADT	TSSOP–14	96 / Rail
MC74HC74ADTR2	TSSOP–14	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	 260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figures 1, 2, 3)	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 4.0 mA $\|I_{out}\|$ ≤ 5.2 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 2.4$ mA $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μA	6.0	2.0	20	80	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 3.0 4.5 6.0	6.0 15 30 35	4.8 10 24 28	4.0 8.0 20 24	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figures 1 and 4)	2.0 3.0 4.5 6.0	100 75 20 17	125 90 25 21	150 120 30 26	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Set or Reset to Q or $\overline{Q}$ (Figures 2 and 4)	2.0 3.0 4.5 6.0	105 80 21 18	130 95 26 22	160 130 32 27	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, $V_{CC} = 5.0$ V	
C_{PD}	Power Dissipation Capacitance (Per Flip–Flop)*	32	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Data to Clock (Figure 3)	2.0 3.0 4.5 6.0	80 35 16 14	100 45 20 17	120 55 24 20	ns
t_h	Minimum Hold Time, Clock to Data (Figure 3)	2.0 3.0 4.5 6.0	3.0 3.0 3.0 3.0	3.0 3.0 3.0 3.0	3.0 3.0 3.0 3.0	ns
t_{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0 3.0 4.5 6.0	8.0 8.0 8.0 8.0	8.0 8.0 8.0 8.0	8.0 8.0 8.0 8.0	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 3.0 4.5 6.0	60 25 12 10	75 30 15 13	90 40 18 15	ns
t_w	Minimum Pulse Width, Set or Reset (Figure 2)	2.0 3.0 4.5 6.0	60 25 12 10	75 30 15 13	90 40 18 15	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figures 1, 2, 3)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

SWITCHING WAVEFORMS

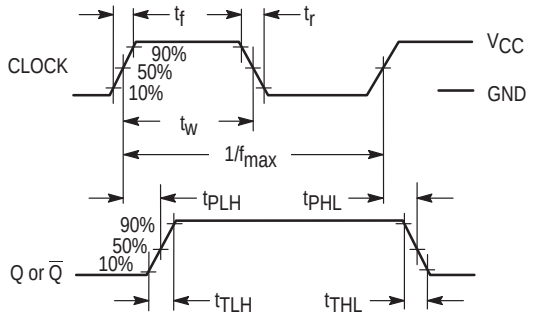


Figure 1.

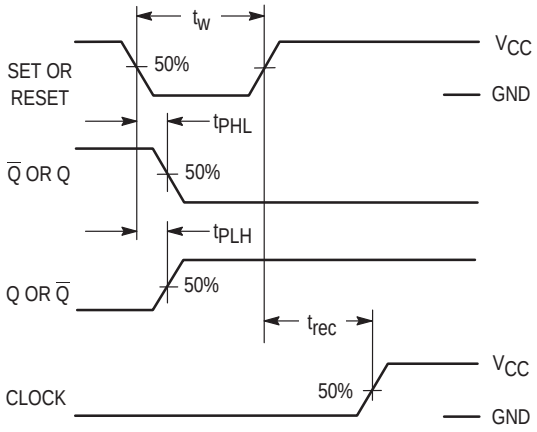


Figure 2.

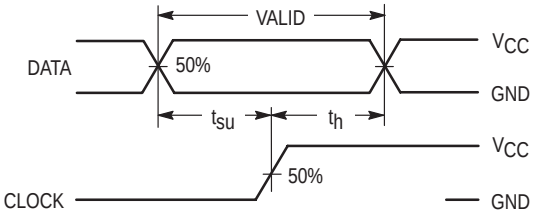
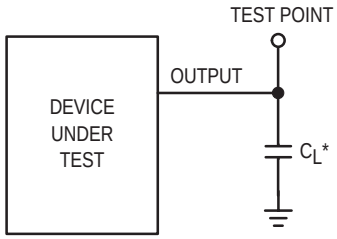


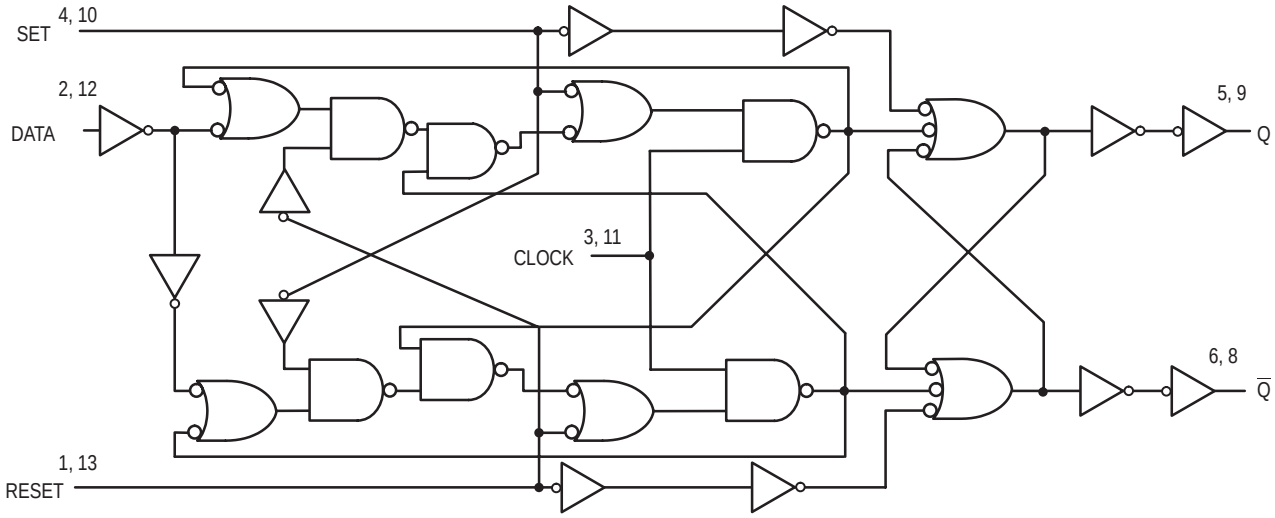
Figure 3.



*Includes all probe and jig capacitance

Figure 4.

EXPANDED LOGIC DIAGRAM



MC74HCT74A

Dual D Flip-Flop with Set and Reset with LSTTL Compatible Inputs

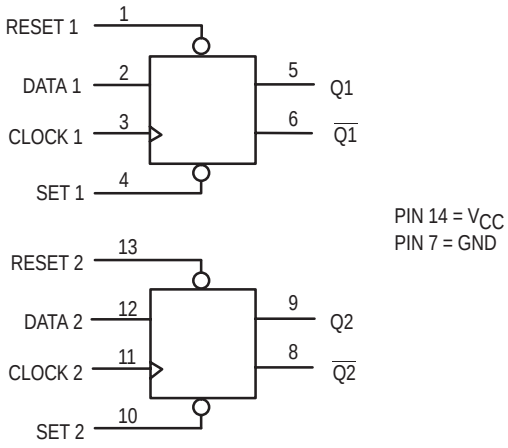
High–Performance Silicon–Gate CMOS

The MC74HCT74A is identical in pinout to the LS74. This device may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

This device consists of two D flip–flops with individual Set, Reset, and Clock inputs. Information at a D–input is transferred to the corresponding Q output on the next positive going edge of the clock input. Both Q and $\overline{Q}$ outputs are available from each flip–flop. The Set and Reset inputs are asynchronous.

- Output Drive Capability: 10 LSTTL Loads
- TTL NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 136 FETs or 34 Equivalent Gates

LOGIC DIAGRAM



Design Criteria	Value	Units
Internal Gate Count*	34	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	.0075	pJ

*Equivalent to a two–input NAND gate.

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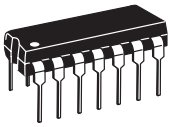
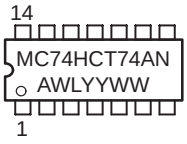
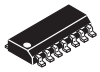
MARKING DIAGRAMS

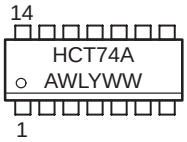


PDIP–14
N SUFFIX
CASE 646



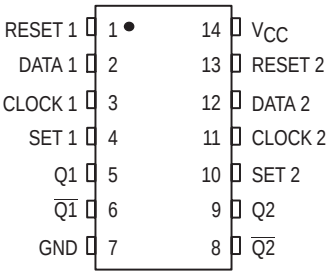


SOIC–14
D SUFFIX
CASE 751A



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

PIN ASSIGNMENT



FUNCTION TABLE

Inputs				Outputs	
Set	Reset	Clock	Data	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H	↓	X	No Change	

*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

ORDERING INFORMATION

Device	Package	Shipping
MC74HCT74AN	PDIP–14	2000 / Box
MC74HCT74AD	SOIC–14	55 / Rail
MC74HCT74ADR2	SOIC–14	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air Plastic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: –10mW/°C from 65° to 125°C
SOIC Package: –7mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 4.0 mA	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 4.0 mA	4.5	0.26	0.33	0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	5.5	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	5.5	2.0	20	80	μA

ΔI_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4 V, Any One Input V_{in} = V_{CC} or GND, Other Inputs I_{out} = 0 μA		≥ –55°C	25°C to 125°C	
			5.5	2.9	2.4	mA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	30	24	20	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figures 1 and 4)	24	30	36	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Set or Reset to Q or $\overline{Q}$ (Figures 2 and 4)	24	30	36	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	15	19	22	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	32	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (V_{CC} = 5.0 V ± 10%, C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Fig.	Guaranteed Limit						Units
			– 55 to 25°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
t_{su}	Minimum Setup Time, Data to Clock	3	15		19		22		ns
t_h	Minimum Hold Time, Clock to Data	3	3		3		3		ns
t_{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock	2	6		8		9		ns
t_w	Minimum Pulse Width, Clock	1	15		19		22		ns
t_w	Minimum Pulse Width, Set or Reset	2	15		19		22		ns
t_r, t_f	Maximum Input Rise and Fall Times	1		500		500		500	ns

SWITCHING WAVEFORMS

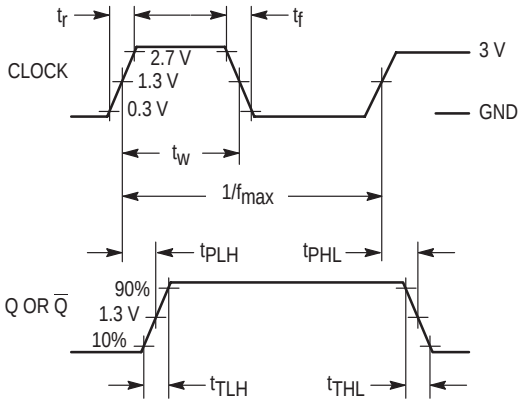


Figure 1.

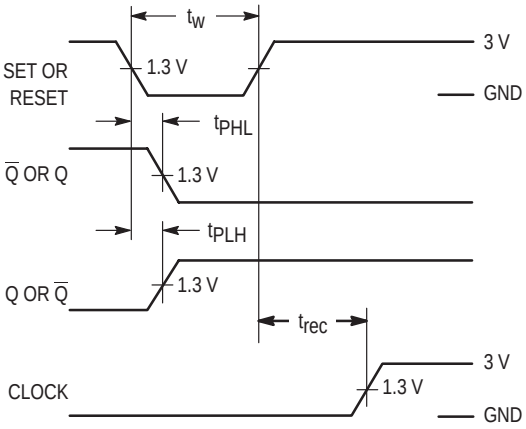


Figure 2.

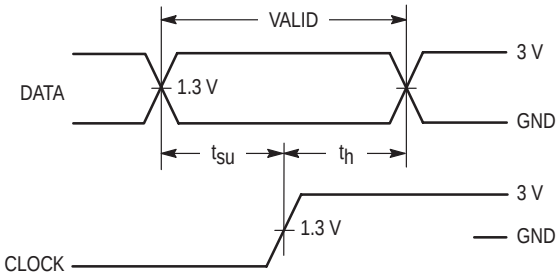
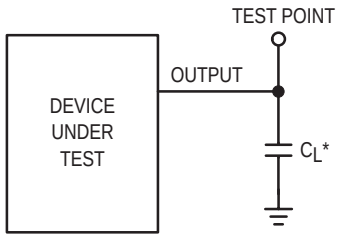


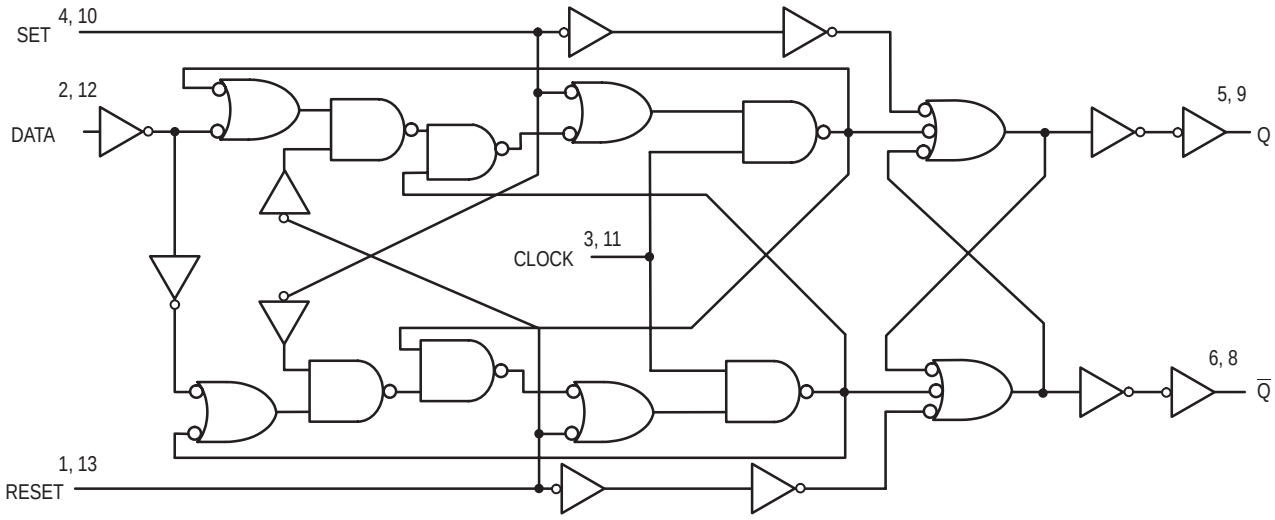
Figure 3.



*Includes all probe and jig capacitance

Figure 4.

EXPANDED LOGIC DIAGRAM



MC74HC86A

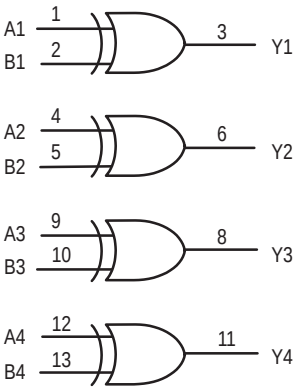
Quad 2-Input Exclusive OR Gate

High–Performance Silicon–Gate CMOS

The MC74HC86A is identical in pinout to the LS86. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 56 FETs or 14 Equivalent Gates

LOGIC DIAGRAM



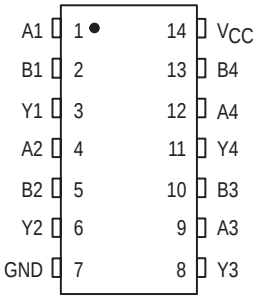
$Y = A \oplus B$

$= \overline{A}B + A\overline{B}$

PIN 14 = V_{CC}

PIN 7 = GND

PIN ASSIGNMENT



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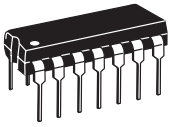
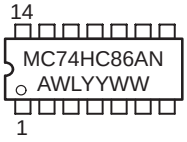
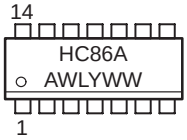
MARKING DIAGRAMS

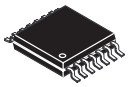


PDIP–14
N SUFFIX
CASE 646

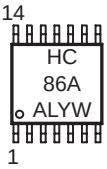


SOIC–14
D SUFFIX
CASE 751A





TSSOP–14
DT SUFFIX
CASE 948G



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

ORDERING INFORMATION

Device	Package	Shipping
MC74HC86AN	PDIP–14	2000 / Box
MC74HC86AD	SOIC–14	55 / Rail
MC74HC86ADR2	SOIC–14	2500 / Reel
MC74HC86ADT	TSSOP–14	96 / Rail
MC74HC86ADTR2	TSSOP–14	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1) V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit – 55 to 25°C	Guaranteed Limit ≤ 85°C	Guaranteed Limit ≤ 125°C	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 4.0 mA $\|I_{out}\|$ ≤ 5.2 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 2.4$ mA $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μA	6.0	1.0	10	40	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input t, = $t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 3.0 4.5 6.0	100 80 20 17	125 90 25 21	150 110 31 26	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, $V_{CC} = 5.0$ V	
C_{PD}	Power Dissipation Capacitance (Per Gate)*	33	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

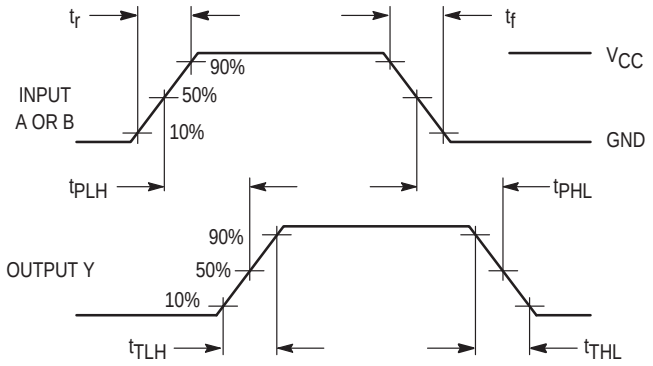
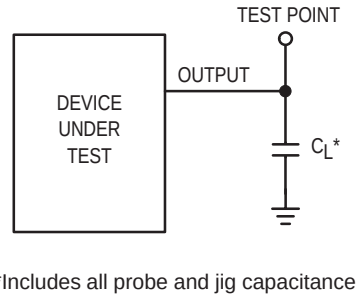


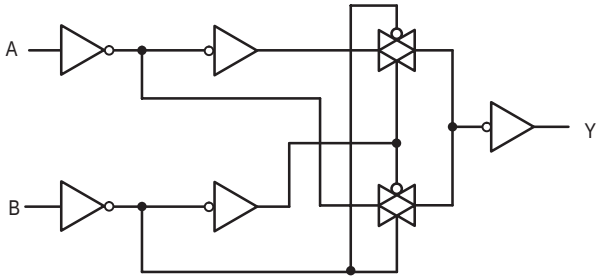
Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM
(1/4 of Device)



MC74HC125A, MC74HC126A

Quad 3-State Noninverting Buffers

High–Performance Silicon–Gate CMOS

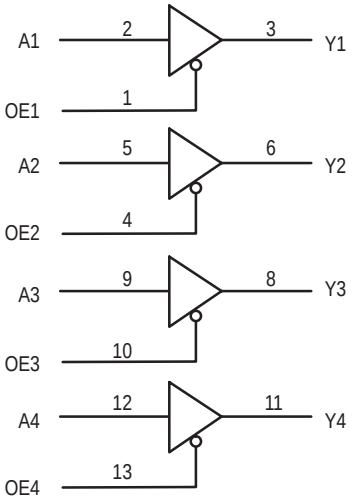
The MC74HC125A and MC74HC126A are identical in pinout to the LS125 and LS126. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC125A and HC126A noninverting buffers are designed to be used with 3–state memory address drivers, clock drivers, and other bus–oriented systems. The devices have four separate output enables that are active–low (HC125A) or active–high (HC126A).

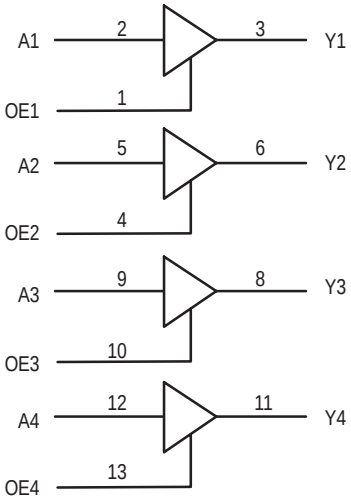
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates

LOGIC DIAGRAM

HC125A
Active–Low Output Enables



HC126A
Active–High Output Enables



PIN 14 = V_{CC}
PIN 7 = GND

FUNCTION TABLE

HC125A		
Inputs		Output
A	OE	Y
H	L	H
L	L	L
X	H	Z

HC126A		
Inputs		Output
A	OE	Y
H	H	H
L	H	L
X	L	Z

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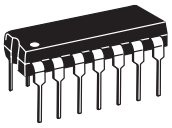
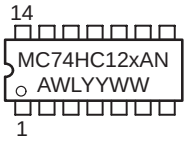
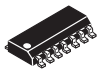
MARKING DIAGRAMS

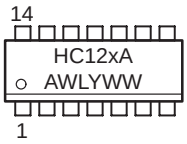


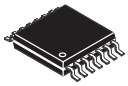
PDIP–14
N SUFFIX
CASE 646



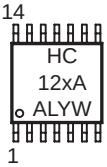


SOIC–14
D SUFFIX
CASE 751A



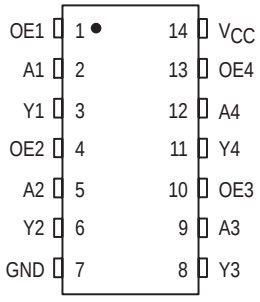


TSSOP–14
DT SUFFIX
CASE 948G



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HC12xAN	PDIP–14	2000 / Box
MC74HC12xAD	SOIC–14	55 / Rail
MC74HC12xADR2	SOIC–14	2500 / Reel
MC74HC12xADT	TSSOP–14	96 / Rail
MC74HC12xADTR2	TSSOP–14	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1) V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} $\|I_{out}\|$ ≤ 3.6 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IL} $\|I_{out}\|$ ≤ 3.6 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0 μA	6.0	4.0	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0 3.0 4.5 6.0	90 36 18 15	115 45 23 20	135 60 27 23	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	2.0 3.0 4.5 6.0	120 45 24 20	150 60 30 26	180 80 36 31	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	2.0 3.0 4.5 6.0	90 36 18 15	115 45 23 20	135 60 27 23	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 3.0 4.5 6.0	60 22 12 10	75 28 15 13	90 34 18 15	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)	—	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Buffer)*	30	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

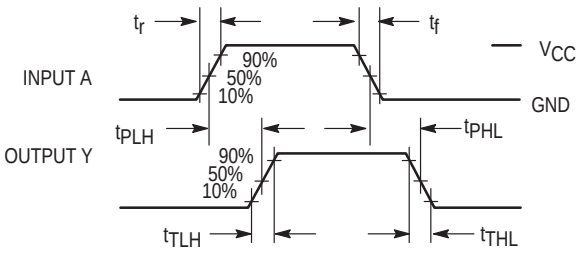


Figure 1.

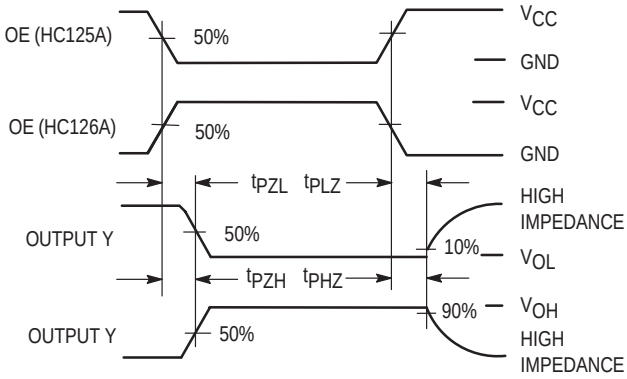
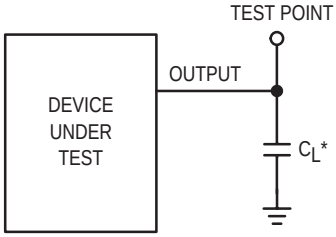
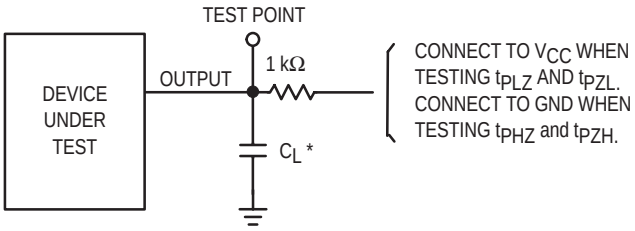


Figure 2.



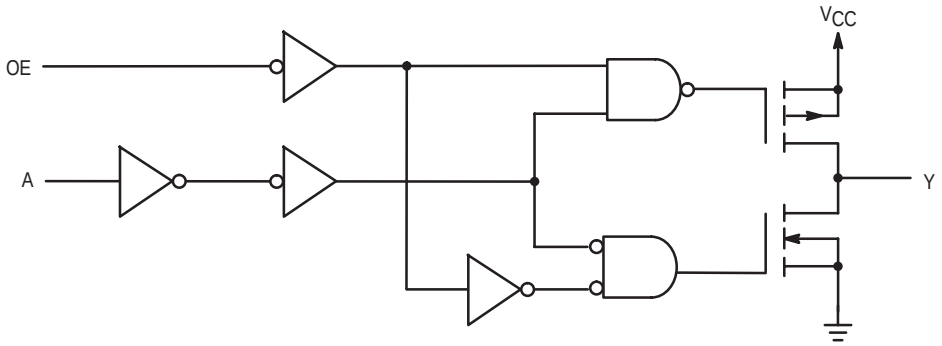
*Includes all probe and jig capacitance

Figure 3. Test Circuit

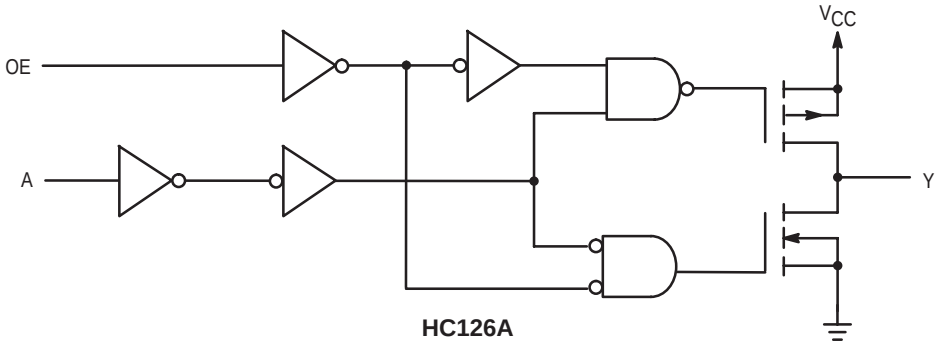


*Includes all probe and jig capacitance

Figure 4. Test Circuit



HC125A
(1/4 OF THE DEVICE)



HC126A
(1/4 OF THE DEVICE)

MC74HC132A

Quad 2-Input NAND Gate with Schmitt-Trigger Inputs

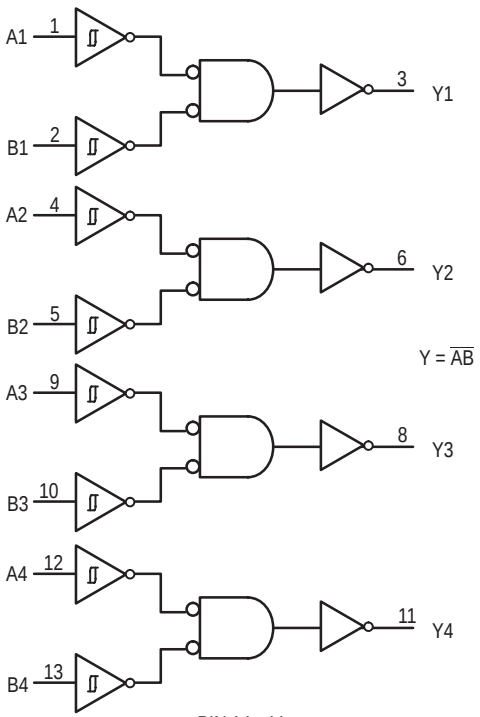
High–Performance Silicon–Gate CMOS

The MC74HC132A is identical in pinout to the LS132. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC132A can be used to enhance noise immunity or to square up slowly changing waveforms.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

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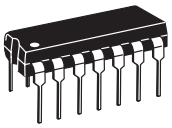
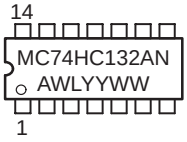
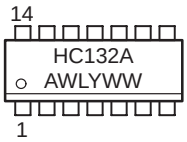
MARKING DIAGRAMS



PDIP–14
N SUFFIX
CASE 646

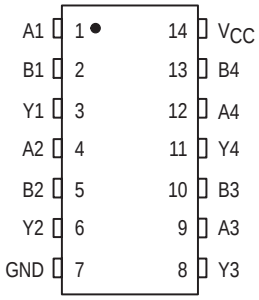


SOIC–14
D SUFFIX
CASE 751A



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HC132AN	PDIP–14	2000 / Box
MC74HC132AD	SOIC–14	55 / Rail
MC74HC132ADR2	SOIC–14	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 1.5 to V_{CC} + 1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	no limit*	ns

*When V_{in} ~ 0.5 V_{CC}, I_{CC} >> quiescent current.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C	– 40°C to + 85°C	– 55°C to + 125°C	
V_{T+} max	Maximum Positive–Going Input Threshold Voltage (Figure 3)	V_{out} = 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{T+} min	Minimum Positive–Going Input Threshold Voltage (Figure 3)	V_{out} = 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.0 2.3 3.0	0.95 2.25 2.95	0.95 2.25 2.95	V
$V_{T–}$ max	Maximum Negative–Going Input Threshold Voltage (Figure 3)	V_{out} = V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.9 2.0 2.6	0.95 2.05 2.65	0.95 2.05 2.65	V
$V_{T–}$ min	Minimum Negative–Going Input Threshold Voltage (Figure 3)	V_{out} = V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
$V_H$max Note 2	Maximum Hysteresis Voltage (Figure 3)	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.2 2.25 3.0	1.2 2.25 3.0	1.2 2.25 3.0	V
$V_H$min Note 2	Minimum Hysteresis Voltage (Figure 3)	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.2 0.4 0.5	0.2 0.4 0.5	0.2 0.4 0.5	V

NOTE: 1. $V_H$min > (V_{T+} min) – ($V_{T–}$ max); $V_H$max = (V_{T+} max) + ($V_{T–}$ min).
NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{OH}	Minimum High–Level Output Voltage	$V_{in} \le V_{T-}$ min or V_{T+} max $\|I_{out}\| \le 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} \le -V_{T-}$ min or V_{T+} max $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	 4.5 6.0	 3.98 5.48	 3.84 5.34	 3.7 5.2	
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} \ge V_{T+}$ max $\|I_{out}\| \le 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} \ge V_{T+}$ max $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.4 0.4	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μA	6.0	1.0	10	40	μA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Gate)*	24	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

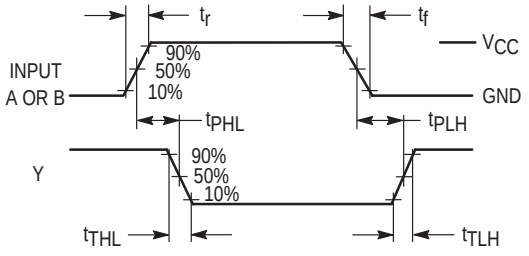
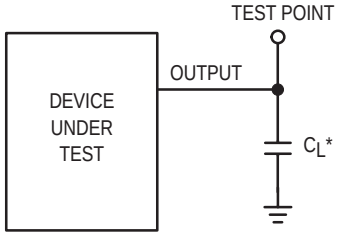


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

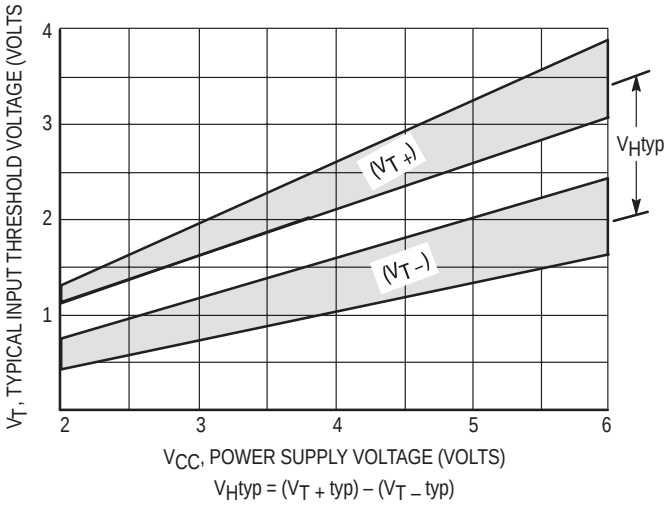


Figure 3. Typical Input Threshold, V_{T+}, V_{T-} Versus Power Supply Voltage

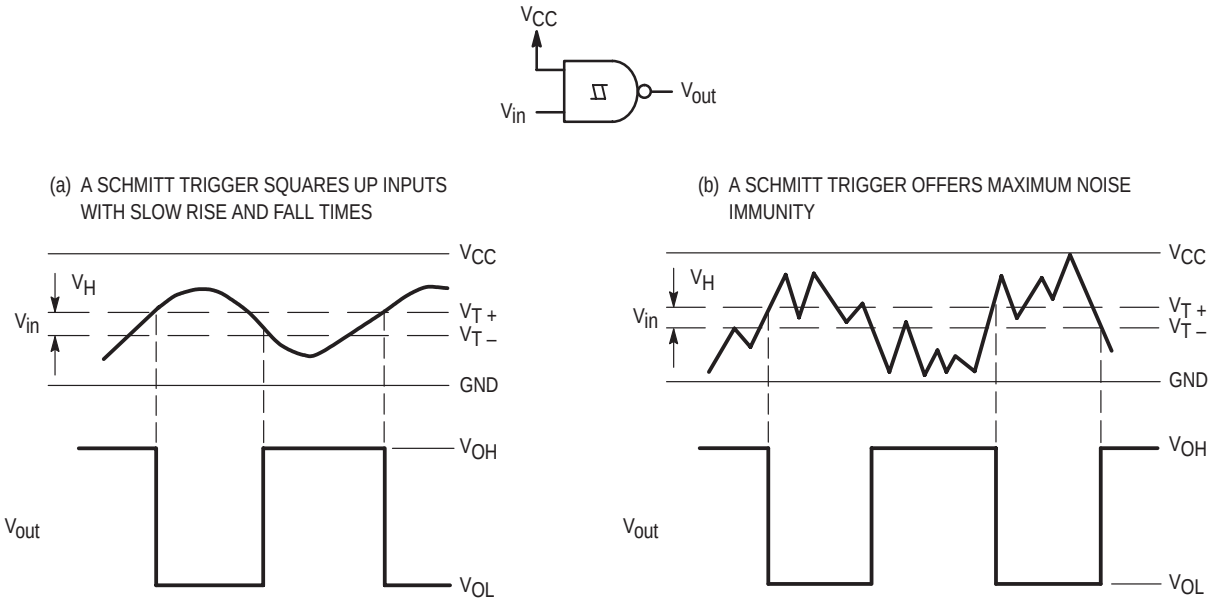


Figure 4. Typical Schmitt–Trigger Applications

MC74HC138A

1-of-8 Decoder/ Demultiplexer

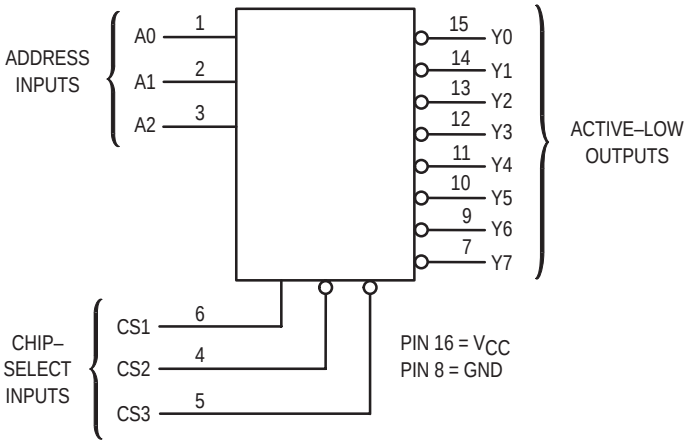
High–Performance Silicon–Gate CMOS

The MC74HC138A is identical in pinout to the LS138. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC138A decodes a three–bit Address to one–of–eight active–low outputs. This device features three Chip Select inputs, two active–low and one active–high to facilitate the demultiplexing, cascading, and chip–selecting functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output; one of the Chip Selects is used as a data input while the other Chip Selects are held in their active states.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 100 FETs or 29 Equivalent Gates

LOGIC DIAGRAM



FUNCTION TABLE

Inputs						Outputs							
CS1	CS2	CS3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = high level (steady state); L = low level (steady state); X = don't care

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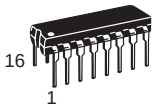
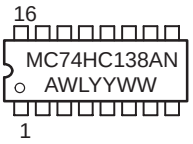
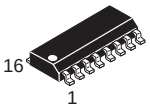
MARKING DIAGRAMS

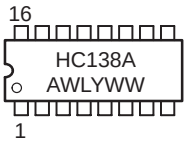


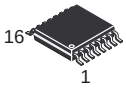
PDIP–16
N SUFFIX
CASE 648



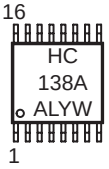


SO–16
D SUFFIX
CASE 751B



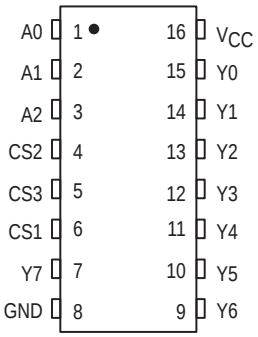


TSSOP–16
DT SUFFIX
CASE 948F



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HC138AN	PDIP–16	2000 / Box
MC74HC138AD	SOIC–16	48 / Rail
MC74HC138ADR2	SOIC–16	2500 / Reel
MC74HC138ADT	TSSOP–16	96 / Rail
MC74HC138ADTR2	TSSOP–16	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 .W/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 2) V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit –55°C to 25°C	Guaranteed Limit ≤ 85°C	Guaranteed Limit ≤ 125°C	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 4.0 mA $\|I_{out}\|$ ≤ 5.2 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				–55°C to 25°C	≤ 85°C	≤ 125°C	
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 2.4$ mA $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55°C to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 4)	2.0 3.0 4.5 6.0	135 90 27 23	170 125 34 29	205 165 41 35	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CS1 to Output Y (Figures 2 and 4)	2.0 3.0 4.5 6.0	110 85 22 19	140 100 28 24	165 125 33 28	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CS2 or CS3 to Output Y (Figures 3 and 4)	2.0 3.0 4.5 6.0	120 90 24 20	150 120 30 26	180 150 36 31	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 4)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, $V_{CC} = 5.0$ V	
C_{PD}	Power Dissipation Capacitance (Per Package)*	55	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

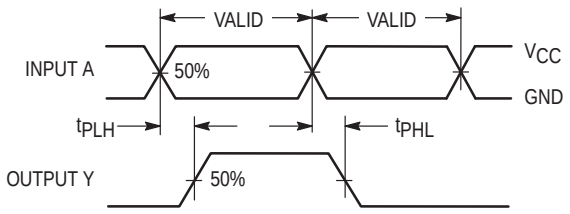


Figure 1.

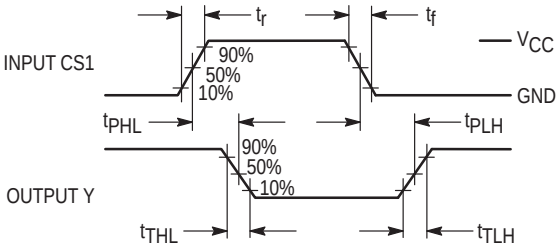


Figure 2.

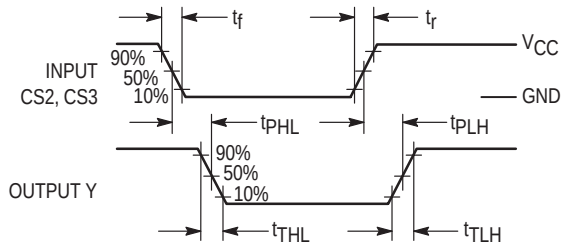
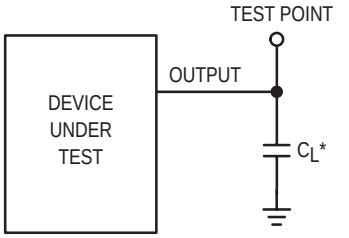


Figure 3.



*Includes all probe and jig capacitance

Figure 4. Test Circuit

PIN DESCRIPTIONS

ADDRESS INPUTS
A0, A1, A2 (Pins 1, 2, 3)

Address inputs. These inputs, when the chip is selected, determine which of the eight outputs is active–low.

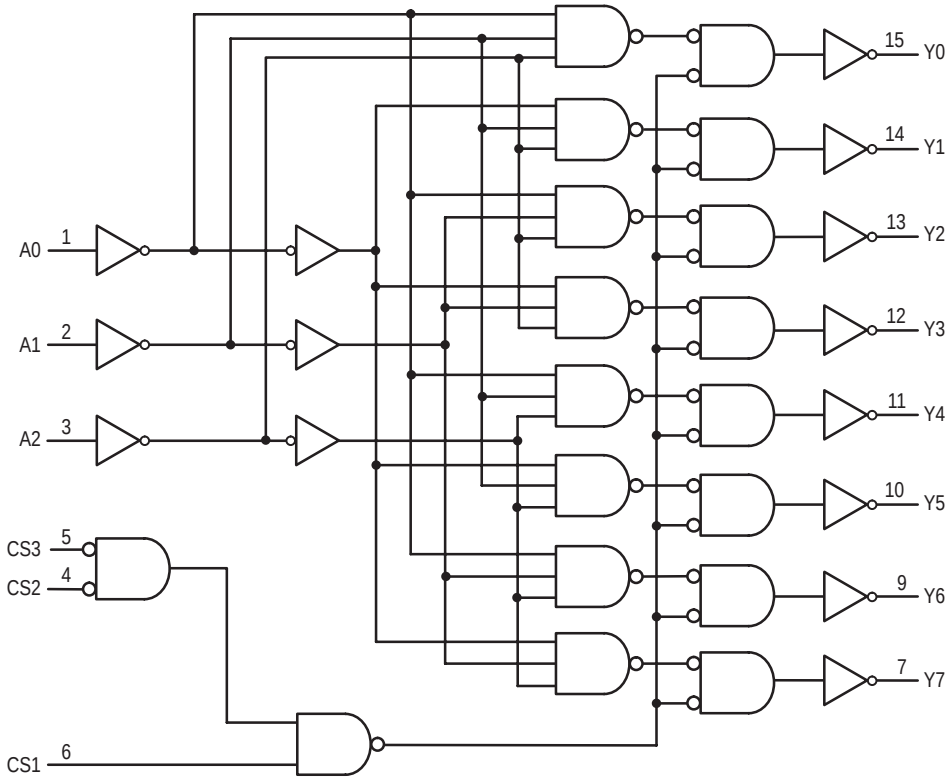
CONTROL INPUTS
CS1, CS2, CS3 (Pins 6, 4, 5)

Chip select inputs. For CS1 at a high level and CS2, CS3 at a low level, the chip is selected and the outputs follow the Address inputs. For any other combination of CS1, CS2, and CS3, the outputs are at a logic high.

OUTPUTS
Y0 – Y7 (Pins 15, 14, 13, 12, 11, 10, 9, 7)

Active–low Decoded outputs. These outputs assume a low level when addressed and the chip is selected. These outputs remain high when not addressed or the chip is not selected.

EXPANDED LOGIC DIAGRAM



MC74HCT138A

1-of-8 Decoder/ Demultiplexer with LSTTL Compatible Inputs

High–Performance Silicon–Gate CMOS

The MC74HCT138A is identical in pinout to the LS138. The HCT138A may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

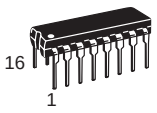
The HCT138A decodes a three–bit Address to one–of–eight active–lot outputs. This device features three Chip Select inputs, two active–low and one active–high to facilitate the demultiplexing, cascading, and chip–selecting functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output; one of the Chip Selects is used as a data input while the other Chip Selects are held in their active states.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 122 FETs or 30.5 Equivalent Gates

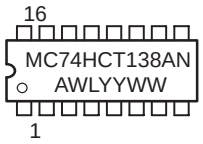
ON Semiconductor

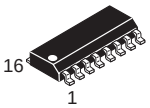
http://onsemi.com

MARKING DIAGRAMS

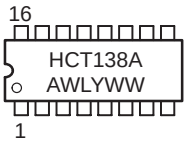


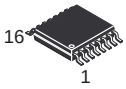
PDIP–16
N SUFFIX
CASE 648



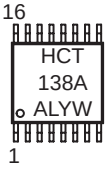


SO–16
D SUFFIX
CASE 751B





TSSOP–16
DT SUFFIX
CASE 948F

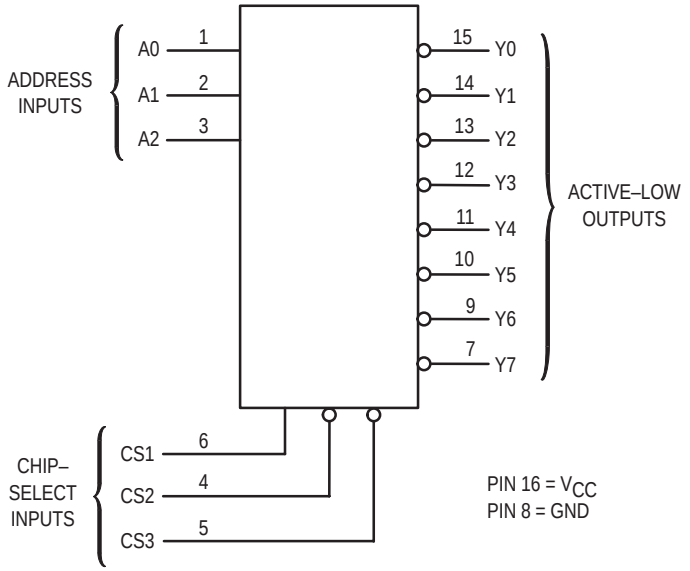


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74HCT138AN	PDIP–16	2000 / Box
MC74HCT138AD	SOIC–16	48 / Rail
MC74HCT138ADR2	SOIC–16	2500 / Reel
MC74HCT138ADT	TSSOP–16	96 / Rail
MC74HCT138ADTR2	TSSOP–16	2500 / Reel

LOGIC DIAGRAM

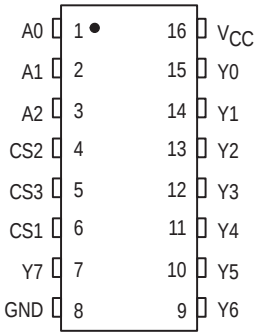


FUNCTION TABLE

Inputs						Outputs							
CS1	CS2	CS3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = high level (steady state)
L = low level (steady state)
X = don't care

PIN ASSIGNMENT



Design Criteria	Value	Units
Internal Gate Count*	30.5	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	.0075	pJ

*Equivalent to a two–input NAND gate.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, TSSOP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 4.0 μA	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 4.0 mA	4.5	0.26	0.33	0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	5.5	4.0	40	160	μA
ΔI_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4 V, Any One Input V_{in} = V_{CC} or GND, Other Inputs I_{out} = 0 μA	5.5	≥ – 55°C 2.9	25°C to 125°C 2.4		mA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

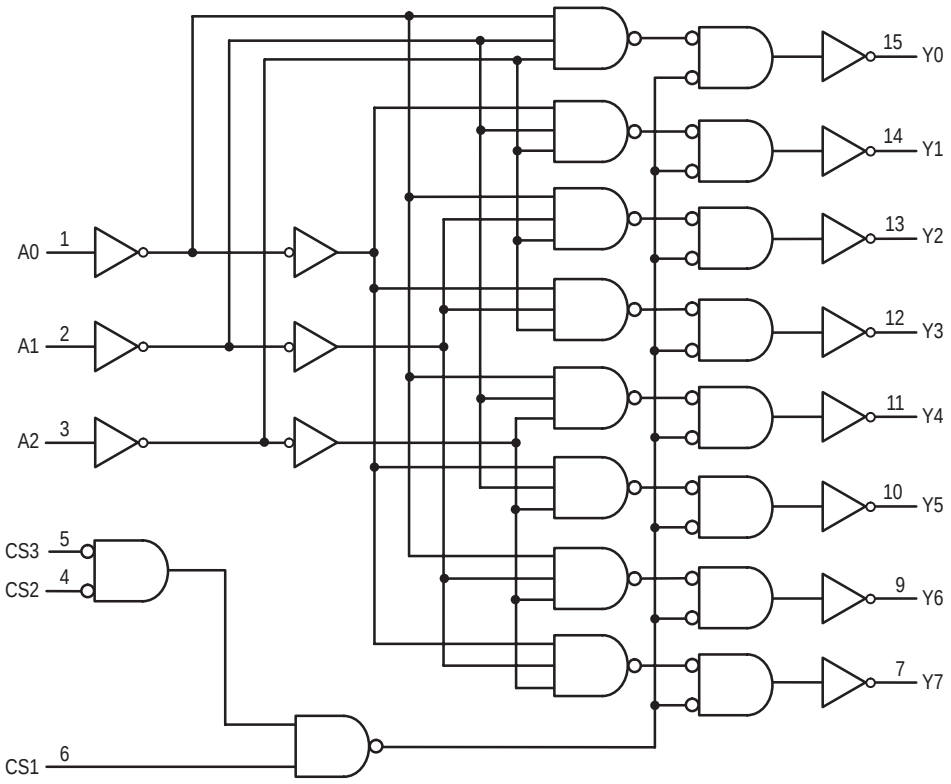
Symbol	Parameter	Guaranteed Limit			Unit
		– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 4)	30	38	45	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CS1 to Output Y (Figures 2 and 4)	27	34	41	ns
t_{PLH}, t_{PHL}	Maximum Output Transition Time, CS2 or CS3 to Output Y (Figures 3 and 4)	30	38	45	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 4)	15	19	22	ns
t_r, t_f	Maximum Input Rise and Fall Time	500	500	500	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	51	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

EXPANDED LOGIC DIAGRAM



SWITCHING WAVEFORMS

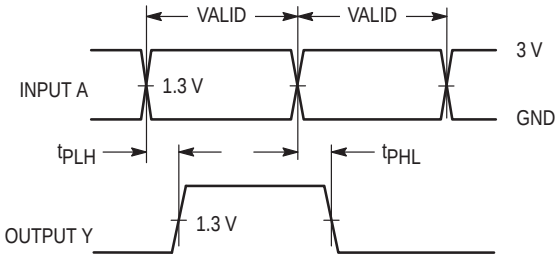


Figure 1.

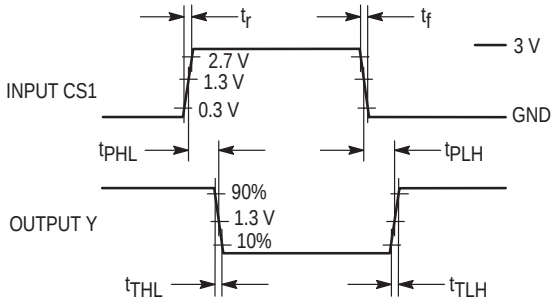


Figure 2.

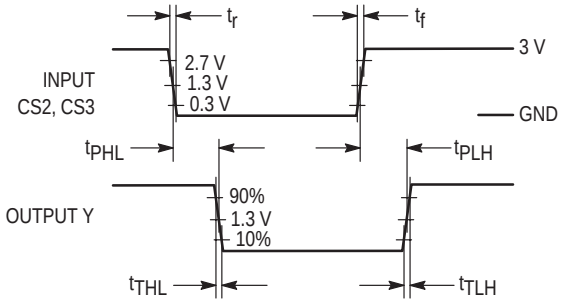
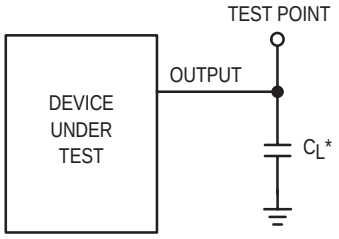


Figure 3.

TEST CIRCUIT



*Includes all probe and jig capacitance

Figure 4.

MC74HC139A

Dual 1-of-4 Decoder/ Demultiplexer

High–Performance Silicon–Gate CMOS

The MC74HC139A is identical in pinout to the LS139. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 1–of–4 decoders, each of which decodes a two–bit Address to one–of–four active–low outputs. Active–low Selects are provided to facilitate the demultiplexing and cascading functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and utilizing the Select as a data input.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 100 FETs or 25 Equivalent Gates

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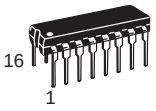
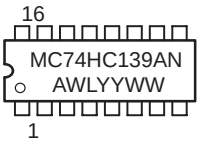
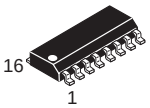
MARKING DIAGRAMS

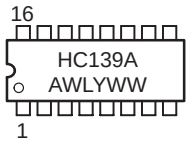


PDIP–16
N SUFFIX
CASE 648



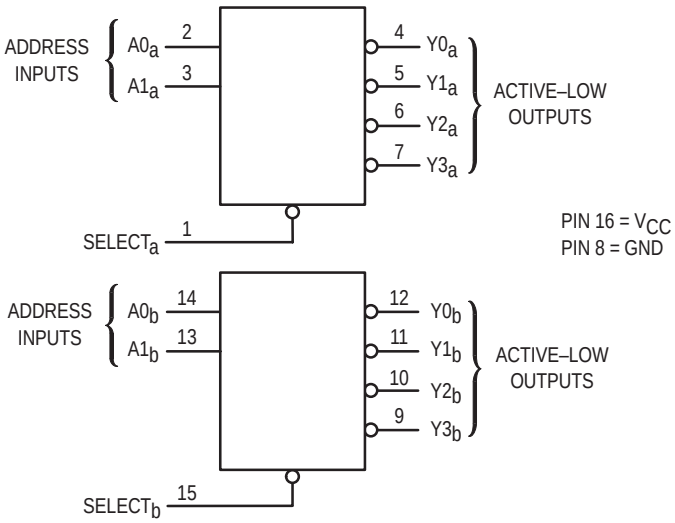


SO–16
D SUFFIX
CASE 751B

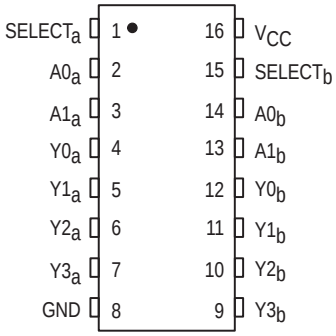


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs			
Select	A1	A0	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

X = don't care

ORDERING INFORMATION

Device	Package	Shipping
MC74HC139AN	PDIP–16	2000 / Box
MC74HC139AD	SOIC–16	48 / Rail
MC74HC139ADR2	SOIC–16	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 1.5 to V_{CC} + 1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 4.0 mA $\|I_{out}\|$ ≤ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 4.0 mA $\|I_{out}\|$ ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Select to Output Y (Figures 1 and 3)	2.0 4.5 6.0	115 23 20	145 29 25	175 35 30	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 2 and 3)	2.0 4.5 6.0	115 23 20	145 29 25	175 35 30	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Decoder)*	55	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

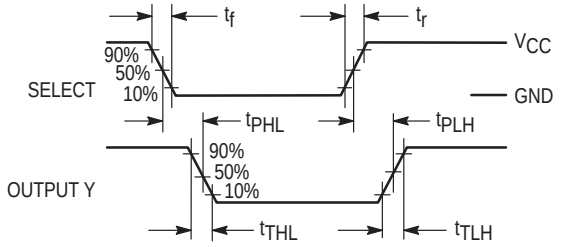


Figure 1.

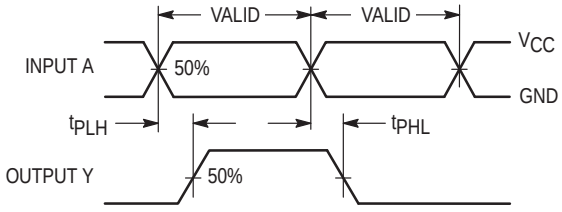
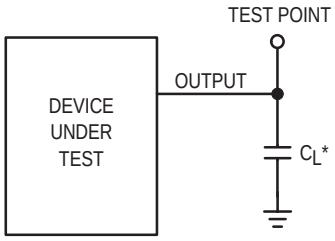


Figure 2.



*Includes all probe and jig capacitance

Figure 3. Test Circuit

PIN DESCRIPTIONS

ADDRESS INPUTS
$A0_a$, $A1_a$, $A0_b$, $A1_b$ (Pins 2, 3, 14, 13)

Address inputs. These inputs, when the respective 1–of–4 decoder is enabled, determine which of its four active–low outputs is selected.

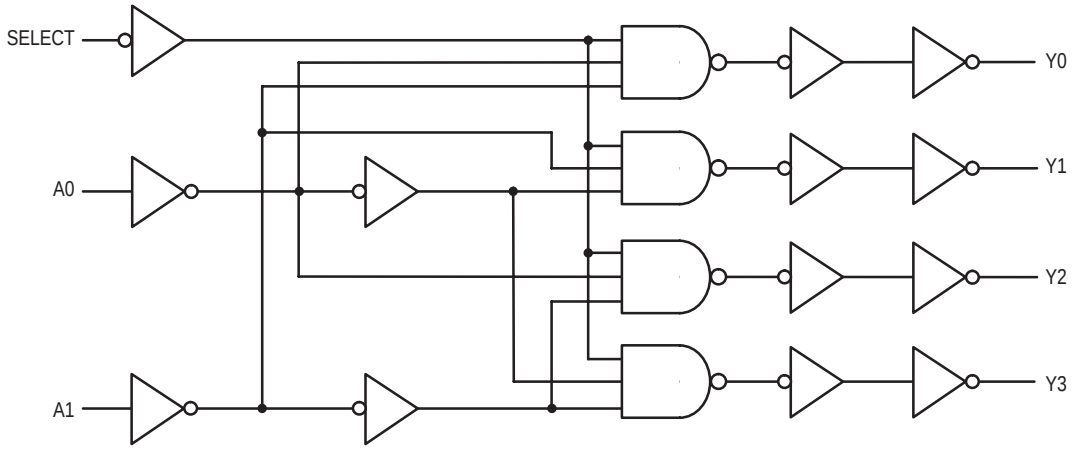
CONTROL INPUTS
$Select_a$, $Select_b$ (Pins 1, 15)

Active–low select inputs. For a low level on this input, the outputs for that particular decoder follow the Address inputs. A high level on this input forces all outputs to a high level.

OUTPUTS
$Y0_a$ – $Y3_a$, $Y0_b$ – $Y3_b$ (Pins 4 – 7, 12, 11, 10, 9)

Active–low outputs. These outputs assume a low level when addressed and the appropriate Select input is active. These outputs remain high when not addressed or the appropriate Select input is inactive.

EXPANDED LOGIC DIAGRAM
(1/2 OF DEVICE)



MC74HC157A

Quad 2-Input Data Selectors / Multiplexers

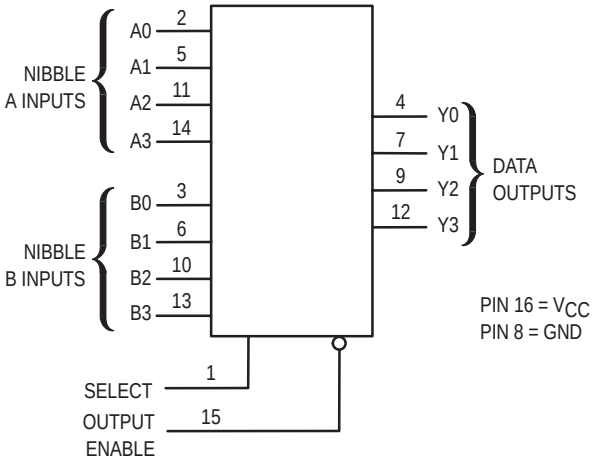
High–Performance Silicon–Gate CMOS

The MC74HC157A is identical in pinout to the LS157. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device routes 2 nibbles (A or B) to a single port (Y) as determined by the Select input. The data is presented at the outputs in noninverted form. A high level on the Output Enable input sets all four Y outputs to a low level.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 82 FETs or 20.5 Equivalent Gates

LOGIC DIAGRAM



FUNCTION TABLE

Inputs		
Output Enable	**Select**	**Outputs Y0 – Y3**
H	X	L
L	L	A0 – A3
L	H	B0 – B3

X = don't care
A0 – A3, B0 – B3 = the levels of the respective Data–Word Inputs.

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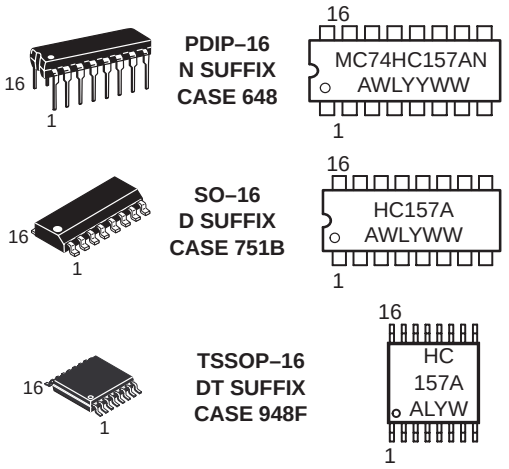
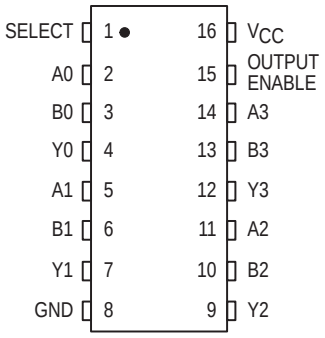
MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HC157AN	PDIP–16	2000 / Box
MC74HC157AD	SOIC–16	48 / Rail
MC74HC157ADR2	SOIC–16	2500 / Reel
MC74HC157ADT	TSSOP–16	96 / Rail
MC74HC157ADTR2	TSSOP–16	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0 μA	6.0	4.0	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 4)	2.0 3.0 4.5 6.0	105 65 21 18	130 85 26 22	160 115 32 27	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Select to Output Y (Figures 2 and 4)	2.0 3.0 4.5 6.0	110 70 22 19	140 90 28 24	165 115 33 28	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 4)	2.0 3.0 4.5 6.0	100 60 20 17	125 80 25 21	150 110 30 26	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package)*	33	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

PIN DESCRIPTIONS

INPUTS

A0, A1, A2, A3 (Pins 2, 5, 11, 14)

Nibble A inputs. The data present on these pins is transferred to the outputs when the Select input is at a low level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form.

B0, B1, B2, B3 (Pins 3, 6, 10, 13)

Nibble B inputs. The data present on these pins is transferred to the outputs when the Select input is at a high level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form.

OUTPUTS

Y0, Y1, Y2, Y3 (Pins 4, 7, 9, 12)

Data outputs. The selected input Nibble is presented at these outputs when the Output Enable input is at a low level. The data present on these pins is in its noninverted form. For the Output Enable input at a high level, the outputs are at a low level.

CONTROL INPUTS

Select (Pin 1)

Nibble select. This input determines the data word to be transferred to the outputs. A low level on this input selects the A inputs and a high level selects the B inputs.

Output Enable (Pin 15)

Output Enable input. A low level on this input allows the selected input data to be presented at the outputs. A high level on this input sets all outputs to a low level.

SWITCHING WAVEFORMS

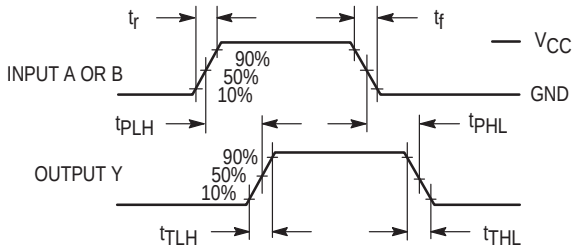


Figure 1. HC157A

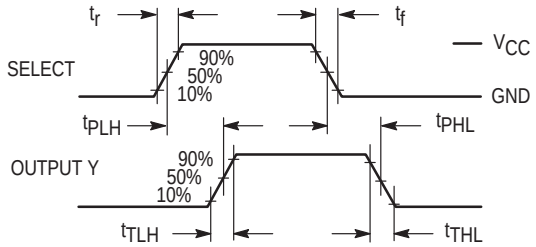


Figure 2. Y versus Select, Noninverted

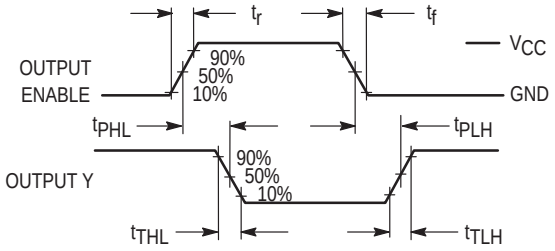
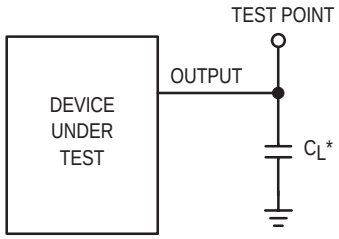


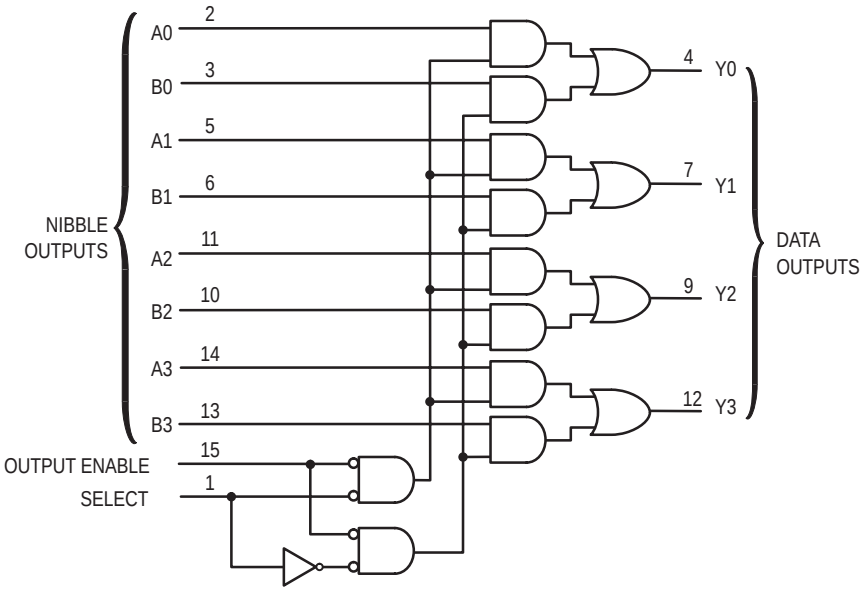
Figure 3. HC157A



*Includes all probe and jig capacitance

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM



MC74HC161A, MC74HC163A

Presettable Counters
High–Performance Silicon–Gate CMOS

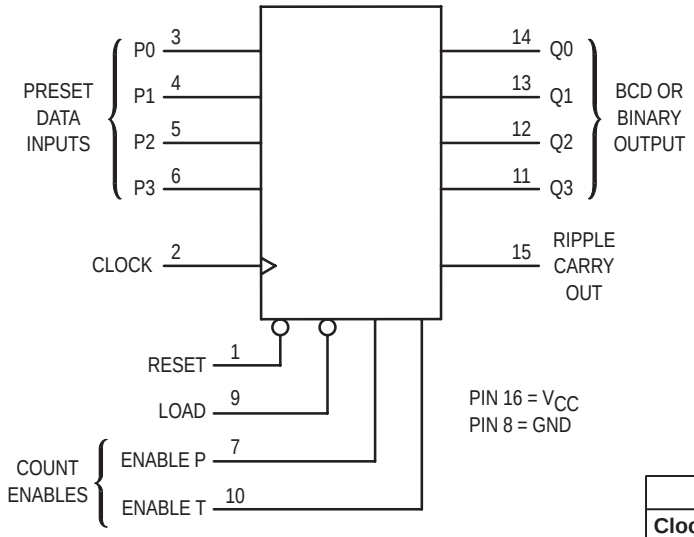
The MC74HC161A and HC163A are identical in pinout to the LS161 and LS163. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC161A and HC163A are programmable 4–bit binary counters with asynchronous and synchronous reset, respectively.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 192 FETs or 48 Equivalent Gates

Device	Count Mode	Reset Mode
HC161A	Binary	Asynchronous
HC163A	Binary	Synchronous

LOGIC DIAGRAM



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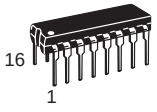
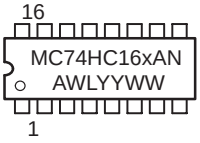
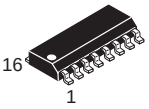
http://onsemi.com

MARKING DIAGRAMS

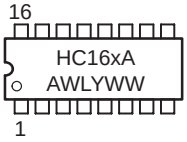


PDIP–16
N SUFFIX
CASE 648





SO–16
D SUFFIX
CASE 751B

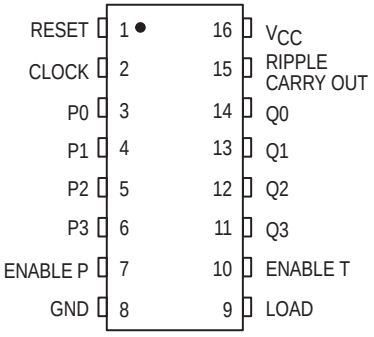


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74HC16xAN	PDIP–16	2000 / Box
MC74HC16xAD	SOIC–16	48 / Rail
MC74HC16xADR2	SOIC–16	2500 / Reel

PIN ASSIGNMENT



FUNCTION TABLE

Inputs					Output
Clock	Reset*	Load	Enable P	Enable T	Q
↗	L	X	X	X	Reset
↗	H	L	X	X	Load Preset Data
↗	H	H	H	H	Count
↗	H	H	L	X	No Count
↗	H	H	X	L	No Count

*HC163A only. HC161A is an Asynchronous Reset Device
H = high level, L = low level, X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \leq 20$ μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \leq 20$ μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 3.6$ mA $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 3.6$ mA $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0 μA	6.0	4.0	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Fig.	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)*	1, 7	2.0 3.0 4.5 6.0	6 15 30 35	5 12 24 28	4 10 20 24	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q	1, 7	2.0 3.0 4.5 6.0	120 75 20 16	160 120 23 20	200 150 28 22	ns
t_{PHL}		1, 7	2.0 3.0 4.5 6.0	145 100 22 18	185 135 25 20	220 150 30 23	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q (HC161A Only)	2, 7	2.0 3.0 4.5 6.0	145 100 20 17	185 135 22 19	220 150 25 21	ns
t_{PLH}	Maximum Propagation Delay, Enable T to Ripple Carry Out	3, 7	2.0 3.0 4.5 6.0	110 60 16 14	150 115 18 15	190 140 20 17	ns
t_{PHL}		3, 7	2.0 3.0 4.5 6.0	135 100 18 15	175 130 20 16	210 160 22 20	ns
t_{PLH}	Maximum Propagation Delay, Clock to Ripple Carry Out	1, 7	2.0 3.0 4.5 6.0	120 75 22 18	160 135 27 22	200 150 30 25	ns
t_{PHL}		1, 7	2.0 3.0 4.5 6.0	145 100 22 20	185 135 28 24	220 150 35 28	ns
t_{PHL}	Maximum Propagation Delay, Reset to Ripple Carry Out (HC161A Only)	2, 7	2.0 3.0 4.5 6.0	155 120 22 18	190 140 26 22	230 155 30 25	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output	2, 7	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
C_{in}	Maximum Input Capacitance	1, 7	—	10	10	10	pF

*Applies to noncascaded/nonsynchronous clocked configurations only with synchronously cascaded counters. (1) Clock to Ripple Carry Out propagation delays. (2) Enable T or Enable P to Clock setup times and (3) Clock to Enable T or Enable P hold times determine f_{max}. However, if Ripple Carry out of each stage is tied to the Clock of the next stage (nonsynchronously clocked) the f_{max} in the table above is applicable. See Applications information in this data sheet.

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Gate)*	45	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Fig.	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Preset Data Inputs to Clock	5	2.0 3.0 4.5 6.0	40 20 15 12	60 30 20 18	80 40 30 20	ns
t_{su}	Minimum Setup Time, Load to Clock	5	2.0 3.0 4.5 6.0	60 25 15 12	75 30 20 18	90 40 30 20	ns
t_{su}	Minimum Setup Time, Reset to Clock (HC163A Only)	4	2.0 3.0 4.5 6.0	60 25 20 17	75 30 25 23	90 40 35 25	ns
t_{su}	Minimum Setup Time, Enable T or Enable P to Clock	6	2.0 3.0 4.5 6.0	80 35 20 17	95 40 25 23	110 50 35 25	ns
t_h	Minimum Hold Time, Clock to Load or Preset Data Inputs	5	2.0 3.0 4.5 6.0	3 3 3 3	3 3 3 3	3 3 3 3	ns
t_h	Minimum Hold Time, Clock to Reset (HC163A Only)	4	2.0 3.0 4.5 6.0	3 3 3 3	3 3 3 3	3 3 3 3	ns
t_h	Minimum Hold Time, Clock to Enable T or Enable P	6	2.0 3.0 4.5 6.0	3 3 3 3	3 3 3 3	3 3 3 3	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (HC161A Only)	2	2.0 3.0 4.5 6.0	80 35 15 12	95 40 20 17	110 50 26 23	ns
t_{rec}	Minimum Recovery Time, Load Inactive to Clock	5	2.0 3.0 4.5 6.0	80 35 15 12	95 40 20 17	110 50 26 23	ns
t_w	Minimum Pulse Width, Clock	1	2.0 3.0 4.5 6.0	60 25 12 10	75 30 15 13	90 40 18 15	ns
t_w	Minimum Pulse Width, Reset (HC161A Only)	2	2.0 3.0 4.5 6.0	60 25 12 10	75 30 15 13	90 40 18 15	ns
t_r, t_f	Maximum Input Rise and Fall Times		2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

FUNCTION DESCRIPTION

The HC161A/163A are programmable 4–bit synchronous counters that feature parallel Load, synchronous or asynchronous Reset, a Carry Output for cascading and count–enable controls.

The HC161A and HC163A are binary counters with asynchronous Reset and synchronous Reset, respectively.

INPUTS

Clock (Pin 2)

The internal flip–flops toggle and the output count advances with the rising edge of the Clock input. In addition, control functions, such as resetting and loading occur with the rising edge of the Clock input.

Preset Data Inputs P0, P1, P2, P3 (Pins 3, 4, 5, 6)

These are the data inputs for programmable counting. Data on these pins may be synchronously loaded into the internal flip–flops and appear at the counter outputs. P0 (Pin 3) is the least–significant bit and P3 (Pin 6) is the most–significant bit.

OUTPUTS

Q0, Q1, Q2, Q3 (Pins 14, 13, 12, 11)

These are the counter outputs. Q0 (Pin 14) is the least–significant bit and Q3 (Pin 11) is the most–significant bit.

Ripple Carry Out (Pin 15)

When the counter is in its maximum state 1111, this output goes high, providing an external look–ahead carry pulse that may be used to enable successive cascaded counters. Ripple Carry Out remains high only during the maximum count state. The logic equation for this output is:

Ripple Carry Out = Enable T • Q0 • Q1 • Q2 • Q3

CONTROL FUNCTIONS

Resetting

A low level on the Reset pin (Pin 1) resets the internal flip–flops and sets the outputs (Q0 through Q3) to a low level. The HC161A resets asynchronously, and the HC163A resets with the rising edge of the Clock input (synchronous reset).

Loading

With the rising edge of the Clock, a low level on Load (Pin 9) loads the data from the Preset Data input pins (P0, P1, P2, P3) into the internal flip–flops and onto the output pins, Q0 through Q3. The count function is disabled as long as Load is low.

Count Enable/Disable

These devices have two count–enable control pins: Enable P (Pin 7) and Enable T (Pin 10). The devices count when these two pins and the Load pin are high. The logic equation is:

Count Enable = Enable P • Enable T • Load

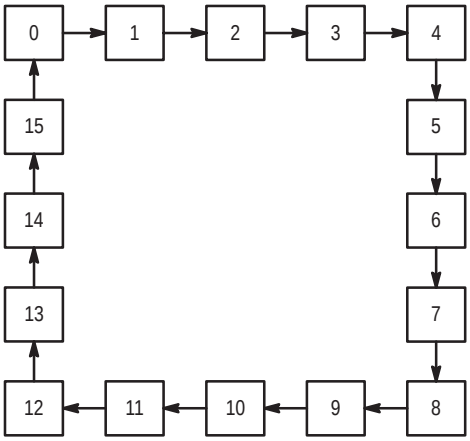
The count is either enabled or disabled by the control inputs according to Table 1. In general, Enable P is a count–enable control: Enable T is both a count–enable and a Ripple–Carry Output control.

Table 1. Count Enable/Disable

Control Inputs			Result at Outputs	
Load	Enable P	Enable T	Q0 – Q3	Ripple Carry Out
H	H	H	Count	High when Q0–Q3 are maximum*
L	H	H	No Count	
X	L	H	No Count	High when Q0–Q3 are maximum*
X	X	L	No Count	L

*Q0 through Q3 are maximum when Q3 Q2 Q1 Q0 = 1111.

OUTPUT STATE DIAGRAMS



Binary Counters

SWITCHING WAVEFORMS

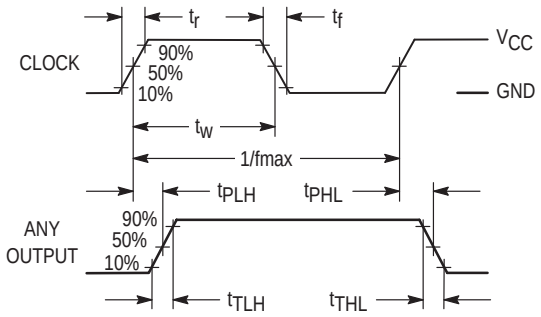


Figure 1.

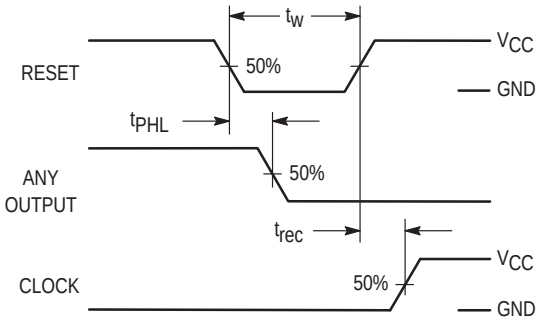


Figure 2.

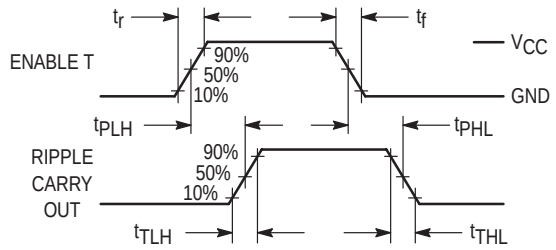


Figure 3.

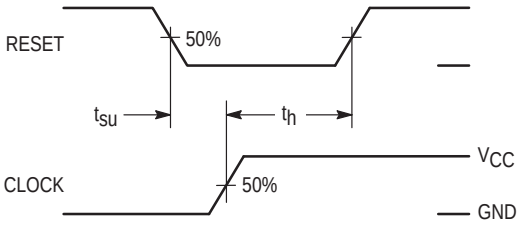


Figure 4. HC163A Only

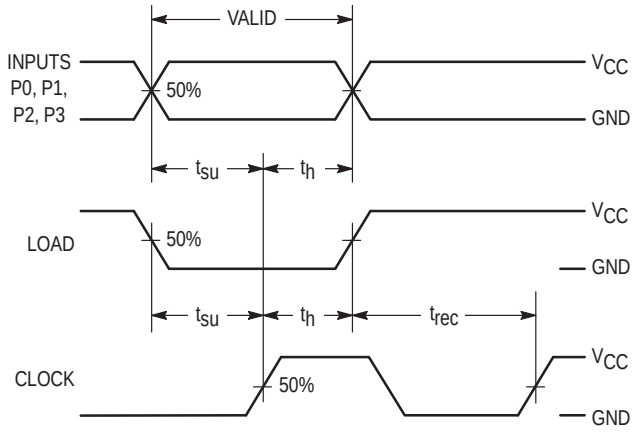


Figure 5.

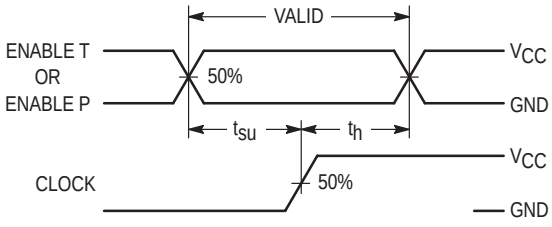
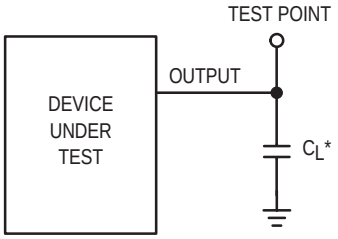


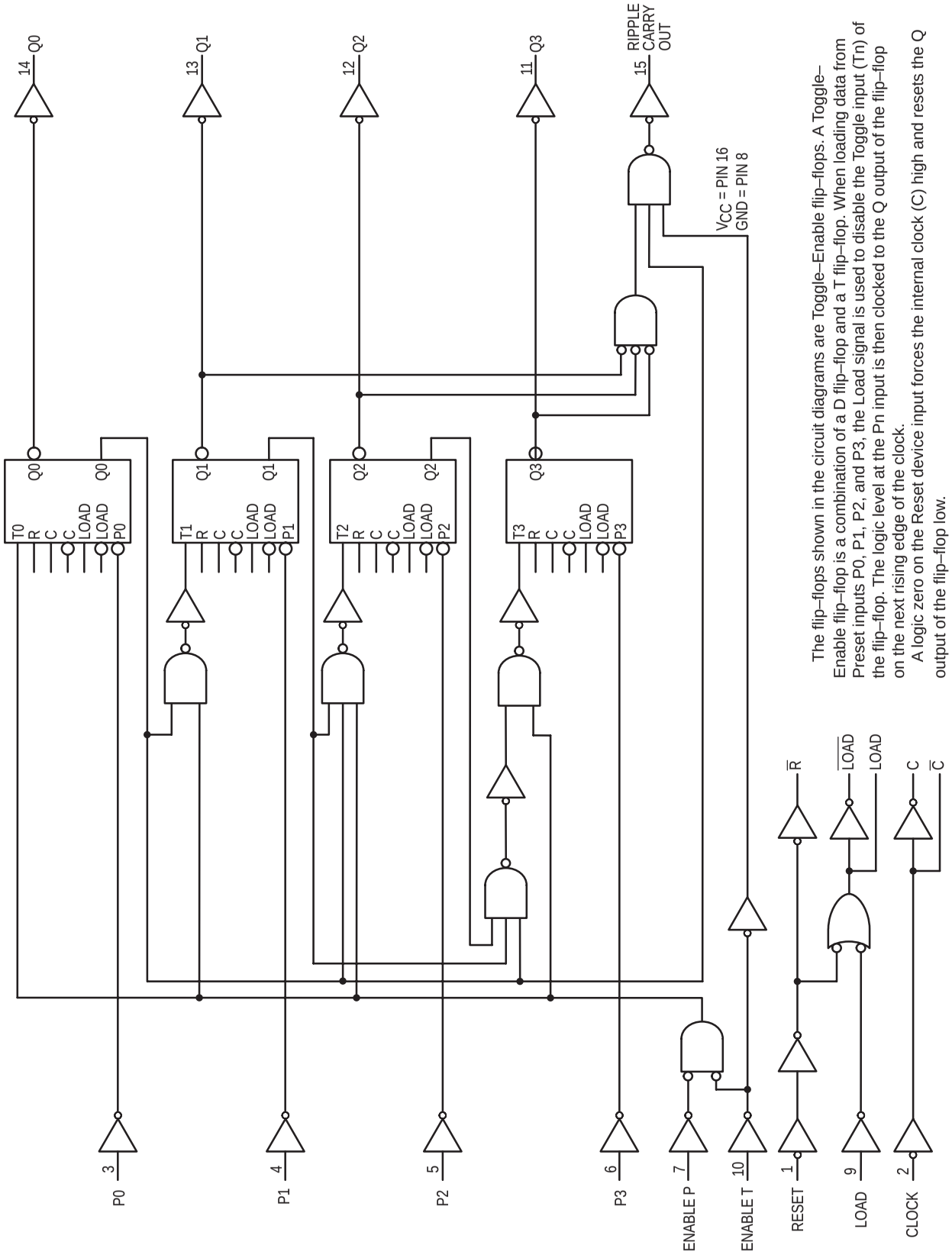
Figure 6.

TEST CIRCUIT



*Includes all probe and jig capacitance

Figure 7.



The flip–flops shown in the circuit diagrams are Toggle–Enable flip–flops. A Toggle–Enable flip–flop is a combination of a D flip–flop and a T flip–flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip–flop. The logic level at the Pn input is then clocked to the Q output of the flip–flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip–flop low.

Figure 8. 4–Bit Binary Counter with Asynchronous Reset (MC74HC161A)

Sequence illustrated in waveforms:
1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one and two.
4. Inhibit.

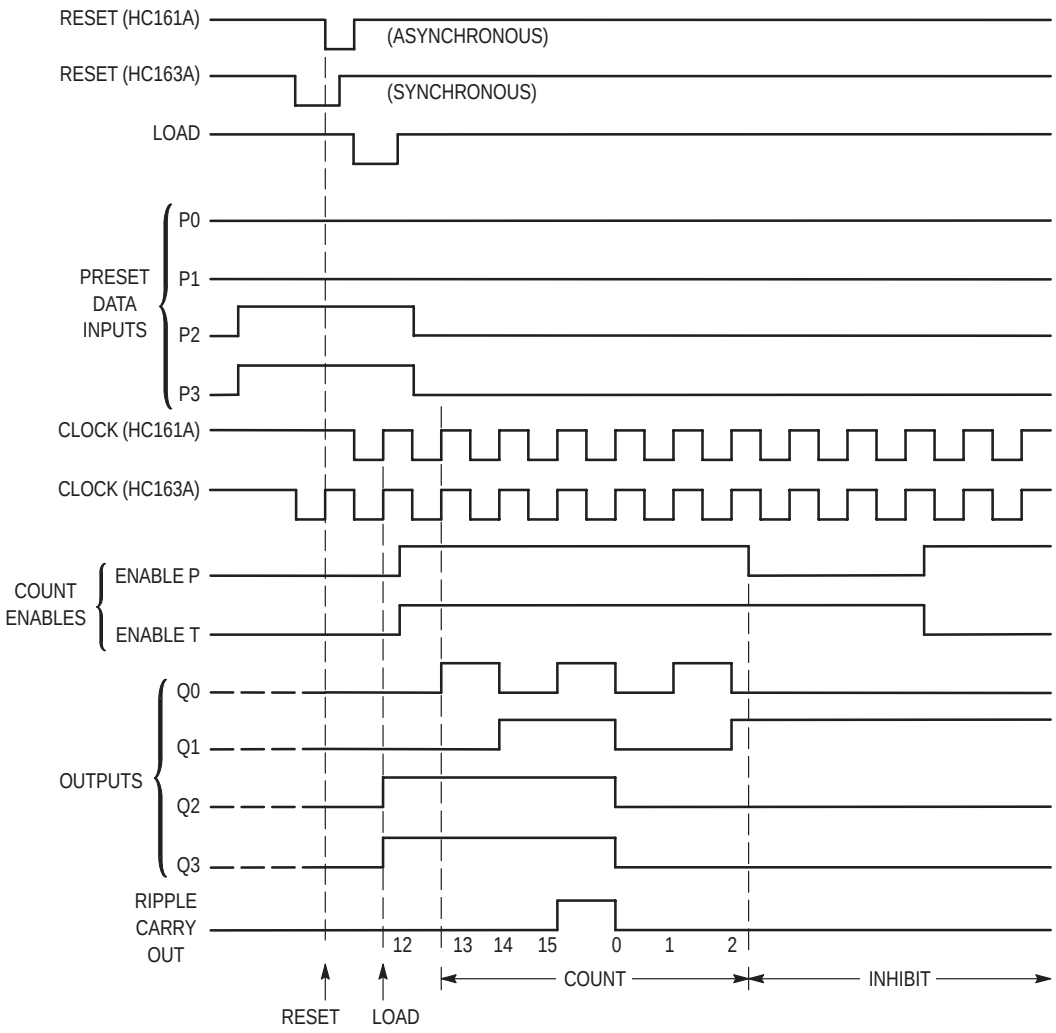
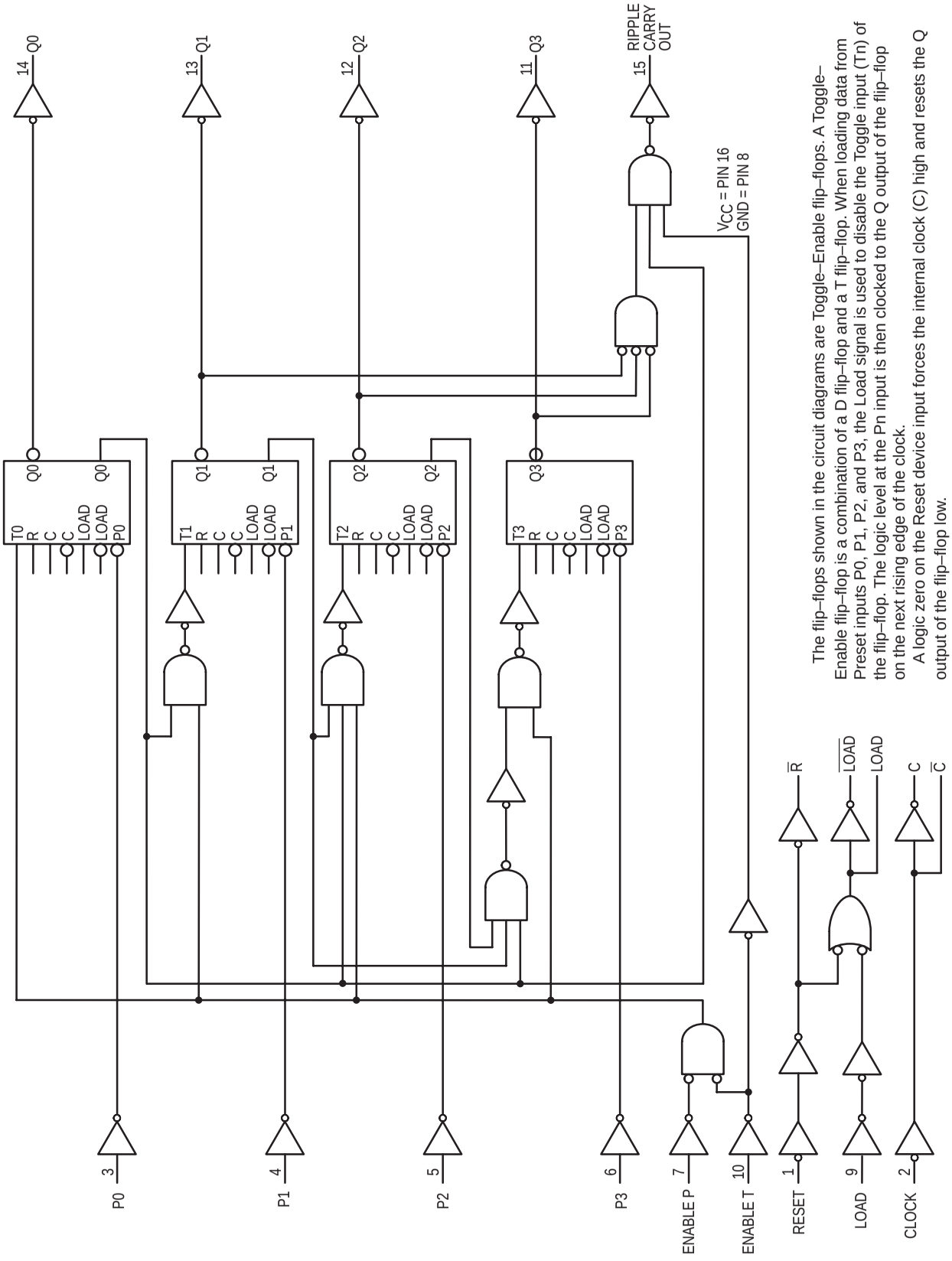


Figure 9. Timing Diagram

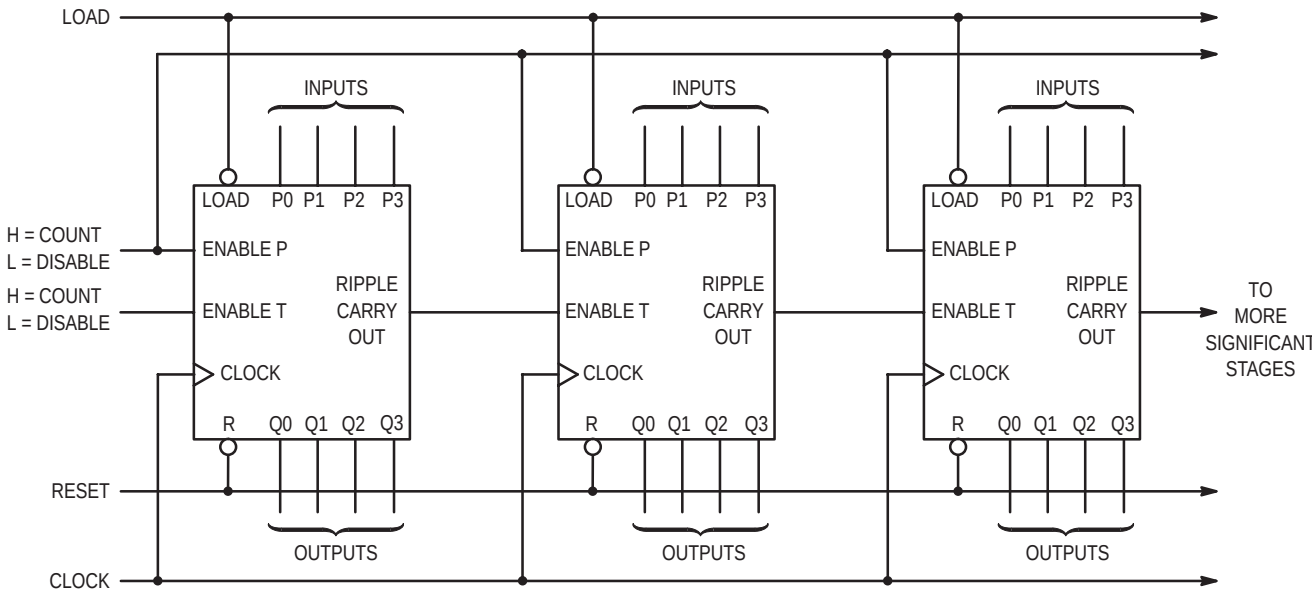


The flip–flops shown in the circuit diagrams are Toggle–Enable flip–flops. A Toggle–Enable flip–flop is a combination of a D flip–flop and a T flip–flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip–flop. The logic level at the Pn input is then clocked to the Q output of the flip–flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip–flop low.

Figure 10. 4–Bit Binary Counter with Synchronous Reset (MC74HC163A)

TYPICAL APPLICATIONS CASCADING



NOTE: When used in these cascaded configurations the clock f_{max} guaranteed limits may not apply. Actual performance will depend on number of stages. This limitation is due to set up times between Enable (Port) and Clock.

Figure 11. N–Bit Synchronous Counters

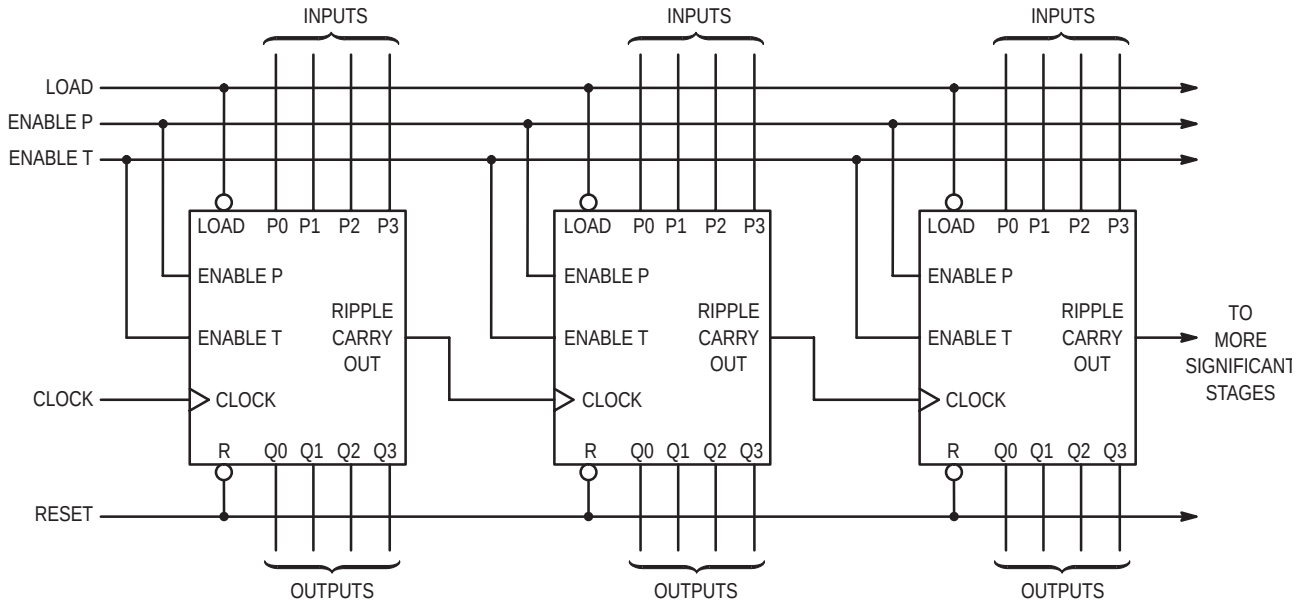


Figure 12. Nibble Ripple Counter

TYPICAL APPLICATIONS VARYING THE MODULUS

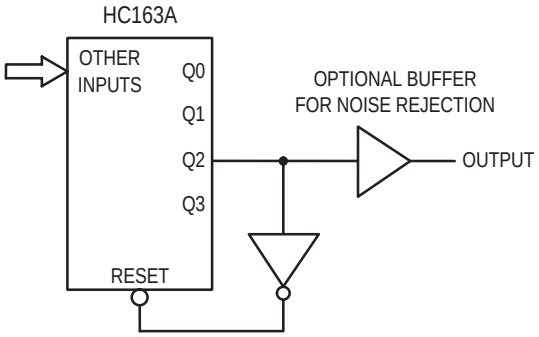


Figure 13. Modulo–5 Counter

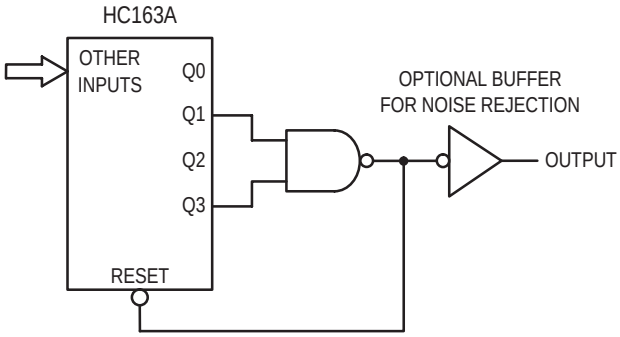


Figure 14. Modulo–11 Counter

The HC163A facilitates designing counters of any modulus with minimal external logic. The output is glitch–free due to the synchronous Reset.

MC74HC164A

8-Bit Serial-Input/ Parallel-Output Shift Register

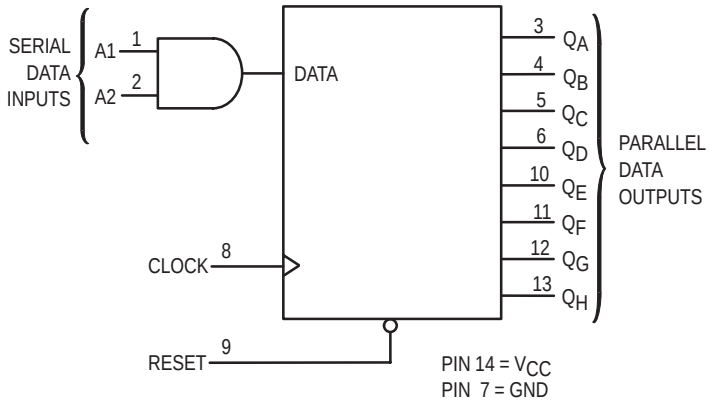
High–Performance Silicon–Gate CMOS

The MC74HC164A is identical in pinout to the LS164. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The MC74HC164A is an 8–bit, serial–input to parallel–output shift register. Two serial data inputs, A1 and A2, are provided so that one input may be used as a data enable. Data is entered on each rising edge of the clock. The active–low asynchronous Reset overrides the Clock and Serial Data inputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 244 FETs or 61 Equivalent Gates

LOGIC DIAGRAM



FUNCTION TABLE

Inputs				Outputs			
Reset	Clock	A1	A2	Q_A	Q_B	…	Q_H
L	X	X	X	L	L	…	L
H	↓	X	X	No Change			
H	↑	H	D	D	Q_{An}	…	Q_{Gn}
H	↑	D	H	D	Q_{An}	…	Q_{Gn}

D = data input

Q_{An} – Q_{Gn} = data shifted from the preceding stage on a rising edge at the clock input.

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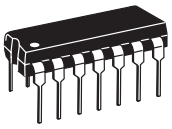
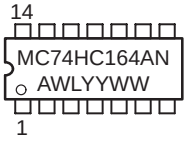
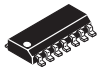
MARKING DIAGRAMS

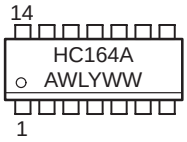


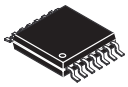
PDIP–14
N SUFFIX
CASE 646



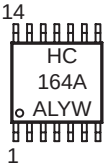


SOIC–14
D SUFFIX
CASE 751A



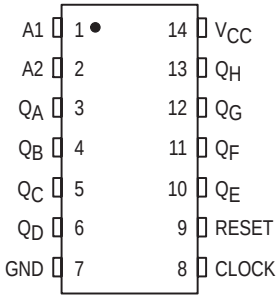


TSSOP–14
DT SUFFIX
CASE 948G



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HC164AN	PDIP–14	2000 / Box
MC74HC164AD	SOIC–14	55 / Rail
MC74HC164ADR2	SOIC–14	2500 / Reel
MC74HC164ADT	TSSOP–14	96 / Rail
MC74HC164ADTR2	TSSOP–14	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1) V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				–55°C to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 4.0 mA $\|I_{out}\|$ ≤ 5.2 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				–55°C to 25°C	≤ 85°C	≤ 125°C	
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 2.4$ mA $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55°C to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 3.0 4.5 6.0	10 20 40 50	10 20 35 45	10 20 30 40	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0 3.0 4.5 6.0	160 100 32 27	200 150 40 34	250 200 48 42	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0 3.0 4.5 6.0	175 100 35 30	220 150 44 37	260 200 53 45	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, $V_{CC} = 5.0$ V	
C_{PD}	Power Dissipation Capacitance (Per Package)*	180	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55°C to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, A1 or A2 to Clock (Figure 3)	2.0 3.0 4.5 6.0	25 15 7 5	35 20 8 6	40 25 9 6	ns
t_h	Minimum Hold Time, Clock to A1 or A2 (Figure 3)	2.0 3.0 4.5 6.0	3 3 3 3	3 3 3 3	3 3 3 3	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 3.0 4.5 6.0	3 3 3 3	3 3 3 3	3 3 3 3	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 3.0 4.5 6.0	50 26 12 10	60 35 15 12	75 45 20 15	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 3.0 4.5 6.0	50 26 12 10	60 35 15 12	75 45 20 15	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

PIN DESCRIPTIONS

INPUTS

A1, A2 (Pins 1, 2)

Serial Data Inputs. Data at these inputs determine the data to be entered into the first stage of the shift register. For a high level to be entered into the shift register, both A1 and A2 inputs must be high, thereby allowing one input to be used as a data–enable input. When only one serial input is used, the other must be connected to V_{CC}.

Clock (Pin 8)

Shift Register Clock. A positive–going transition on this pin shifts the data at each stage to the next stage. The shift register is completely static, allowing clock rates down to DC in a continuous or intermittent mode.

OUTPUTS

Q_A – Q_H (Pins 3, 4, 5, 6, 10, 11, 12, 13)

Parallel Shift Register Outputs. The shifted data is presented at these outputs in true, or noninverted, form.

CONTROL INPUT

Reset (Pin 9)

Active–Low, Asynchronous Reset Input. A low voltage applied to this input resets all internal flip–flops and sets Outputs Q_A – Q_H to the low level state.

SWITCHING WAVEFORMS

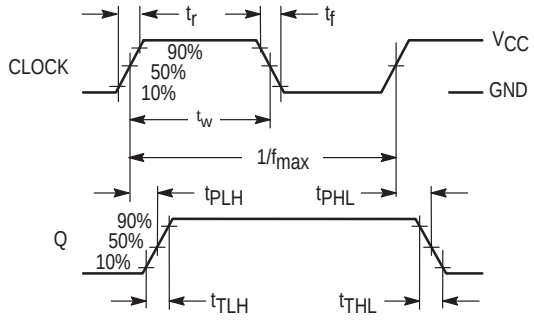


Figure 1.

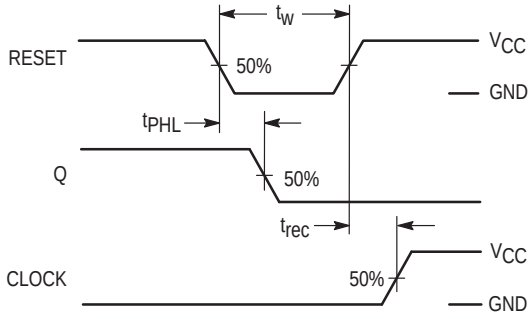


Figure 2.

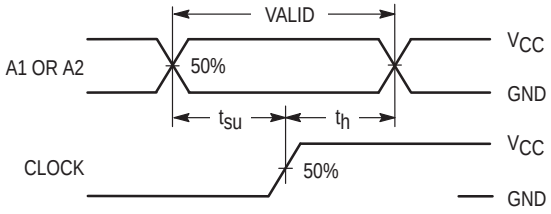
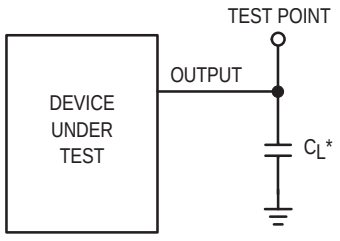


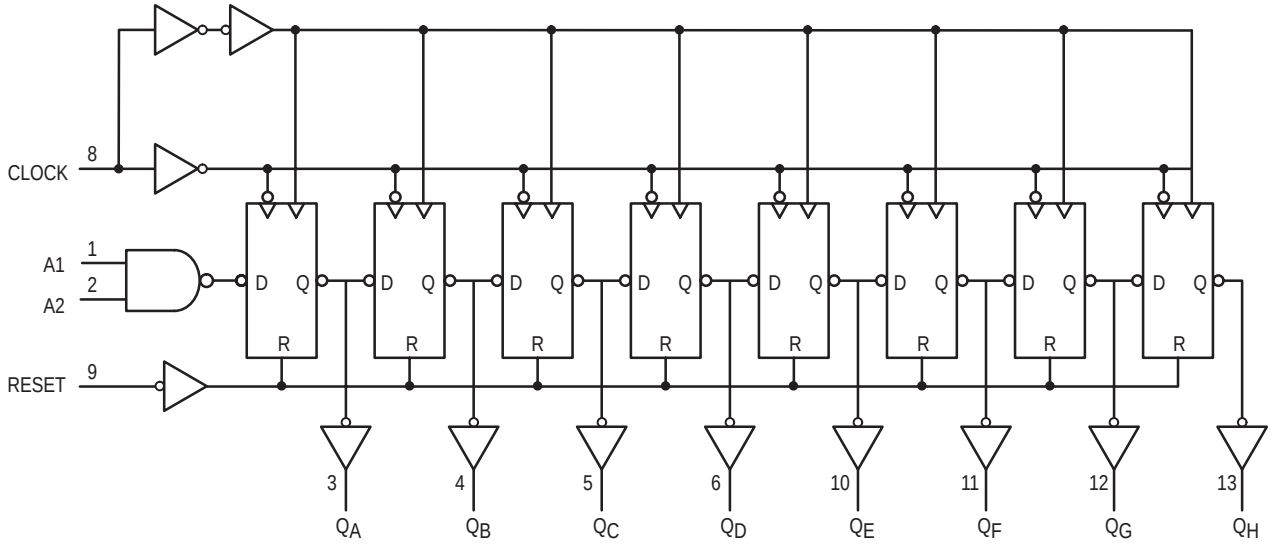
Figure 3.



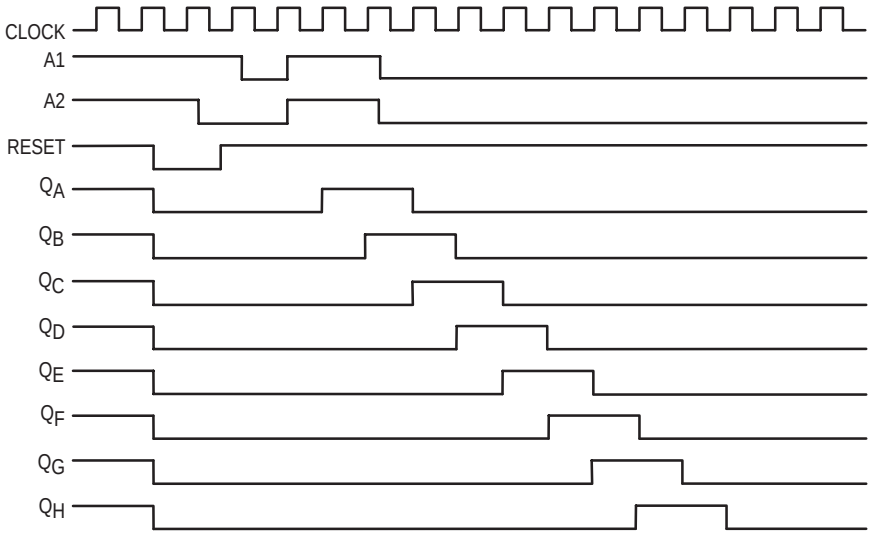
*Includes all probe and jig capacitance

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM



MC74HC165A

8-Bit Serial or Parallel-Input/ Serial-Output Shift Register

High–Performance Silicon–Gate CMOS

The MC74HC165A is identical in pinout to the LS165. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is an 8–bit shift register with complementary outputs from the last stage. Data may be loaded into the register either in parallel or in serial form. When the Serial Shift/Parallel Load input is low, the data is loaded asynchronously in parallel. When the Serial Shift/Parallel Load input is high, the data is loaded serially on the rising edge of either Clock or Clock Inhibit (see the Function Table).

The 2–input NOR clock may be used either by combining two independent clock sources or by designating one of the clock inputs to act as a clock inhibit.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 286 FETs or 71.5 Equivalent Gates

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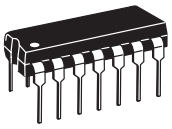
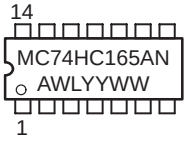
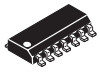
MARKING DIAGRAMS

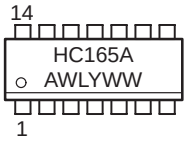


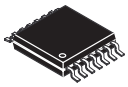
PDIP–14
N SUFFIX
CASE 646



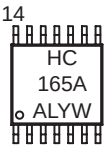


SOIC–14
D SUFFIX
CASE 751A





TSSOP–14
DT SUFFIX
CASE 948G



A = Assembly Location
WL or L = Wafer Lot
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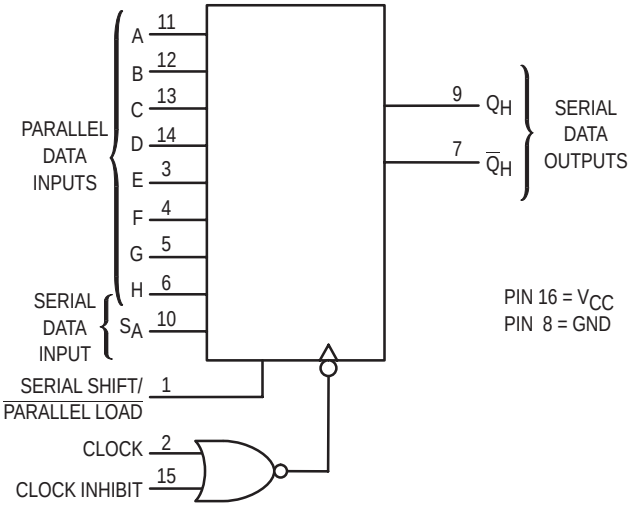
WW or W = Work Week

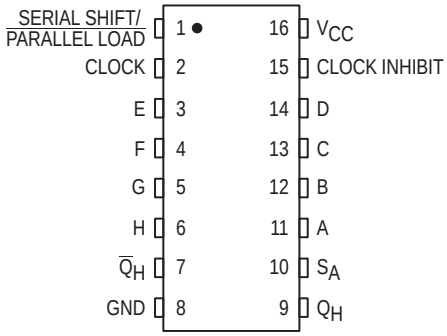
ORDERING INFORMATION

Device	Package	Shipping
MC74HC165AN	PDIP–14	2000 / Box
MC74HC165AD	SOIC–14	55 / Rail
MC74HC165ADR2	SOIC–14	2500 / Reel
MC74HC165ADT	TSSOP–14	96 / Rail
MC74HC165ADTR2	TSSOP–14	2500 / Reel

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs					Internal Stages		Output	
Serial Shift/ $\overline{\text{Parallel Load}}$	Clock	Clock Inhibit	S_A	A – H	Q_A	Q_B	Q_H	Operation
L	X	X	X	a … h	a	b	h	Asynchronous Parallel Load
H H	↗ ↗	L L	L H	X X	L H	Q_{An} Q_{An}	Q_{Gn} Q_{Gn}	Serial Shift via Clock
H H	L L	↗ ↗	L H	X X	L H	Q_{An} Q_{An}	Q_{Gn} Q_{Gn}	Serial Shift via Clock Inhibit
H H	X H	H X	X X	X X	No Change			Inhibited Clock
H	L	L	X	X	No Change			No Clock

X = don't care Q_{An} – Q_{Gn} = Data shifted from the preceding stage

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
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This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 600 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit – 55 to 25°C	Guaranteed Limit ≤ 85°C	Guaranteed Limit ≤ 125°C	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.80	0.5 0.9 1.35 1.80	0.5 0.9 1.35 1.80	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 4.0 mA $\|I_{out}\|$ ≤ 5.2 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	V

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 2.4$ mA $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 8)	2.0 3.0 4.5 6.0	6 18 30 35	4.8 17 24 28	4 15 20 24	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock (or Clock Inhibit) to Q_H or $\overline{Q}_H$ (Figures 1 and 8)	2.0 3.0 4.5 6.0	150 52 30 26	190 63 38 33	225 65 45 38	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Serial Shift/$\overline{\text{Parallel Load}}$ to Q_H or $\overline{Q}_H$ (Figures 2 and 8)	2.0 3.0 4.5 6.0	175 58 35 30	220 70 44 37	265 72 53 45	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input H to Q_H or $\overline{Q}_H$ (Figures 3 and 8)	2.0 3.0 4.5 6.0	150 52 30 26	190 63 38 33	225 65 45 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 8)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package)*	40	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Parallel Data Inputs to Serial Shift/$\overline{\text{Parallel Load}}$ (Figure 4)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t_{su}	Minimum Setup Time, Input SA to Clock (or Clock Inhibit) (Figure 5)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t_{su}	Minimum Setup Time, Serial Shift/$\overline{\text{Parallel Load}}$ to Clock (or Clock Inhibit) (Figure 6)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t_{su}	Minimum Setup Time, Clock to Clock Inhibit (Figure 7)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t_h	Minimum Hold Time, Serial Shift/$\overline{\text{Parallel Load}}$ to Parallel Data Inputs (Figure 4)	2.0 3.0 4.5 6.0	5 5 5 5	5 5 5 5	5 5 5 5	ns
t_h	Minimum Hold Time, Clock (or Clock Inhibit) to Input SA (Figure 5)	2.0 3.0 4.5 6.0	5 5 5 5	5 5 5 5	5 5 5 5	ns
t_h	Minimum Hold Time, Clock (or Clock Inhibit) to Serial Shift/$\overline{\text{Parallel Load}}$ (Figure 6)	2.0 3.0 4.5 6.0	5 5 5 5	5 5 5 5	5 5 5 5	ns
t_{rec}	Minimum Recovery Time, Clock to Clock Inhibit (Figure 7)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t_w	Minimum Pulse Width, Clock (or Clock Inhibit) (Figure 1)	2.0 3.0 4.5 6.0	70 27 15 13	90 32 19 16	100 36 22 19	ns
t_w	Minimum Pulse width, Serial Shift/$\overline{\text{Parallel Load}}$ (Figure 2)	2.0 3.0 4.5 6.0	70 27 15 13	90 32 19 16	100 36 22 19	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

PIN DESCRIPTIONS

INPUTS

A, B, C, D, E, F, G, H (Pins 11, 12, 13, 14, 3, 4, 5, 6)

Parallel Data inputs. Data on these inputs are asynchronously entered in parallel into the internal flip–flops when the Serial Shift/Parallel Load input is low.

SA (Pin 10)

Serial Data input. When the Serial Shift/Parallel Load input is high, data on this pin is serially entered into the first stage of the shift register with the rising edge of the Clock.

CONTROL INPUTS

Serial Shift/Parallel Load (Pin 1)

Data–entry control input. When a high level is applied to this pin, data at the Serial Data input (SA) are shifted into the register with the rising edge of the Clock. When a low level is applied to this pin, data at the Parallel Data inputs are asynchronously loaded into each of the eight internal stages.

Clock, Clock Inhibit (Pins 2, 15)

Clock inputs. These two clock inputs function identically. Either may be used as an active–high clock inhibit. However, to avoid double clocking, the inhibit input should go high only while the clock input is high.

The shift register is completely static, allowing Clock rates down to DC in a continuous or intermittent mode.

OUTPUTS

Q_H, $\overline{Q}_H$ (Pins 9, 7)

Complementary Shift Register outputs. These pins are the noninverted and inverted outputs of the eighth stage of the shift register.

SWITCHING WAVEFORMS

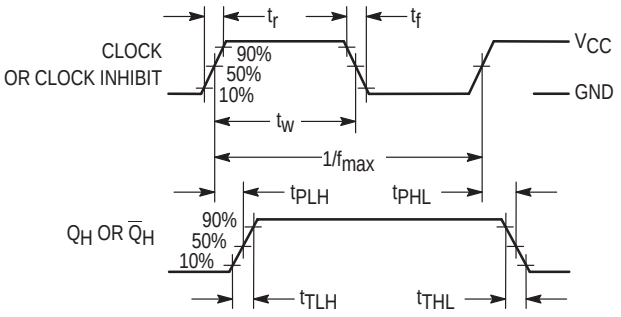


Figure 1. Serial–Shift Mode

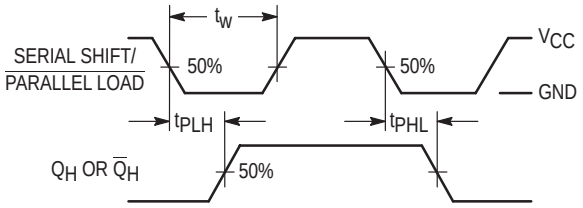


Figure 2. Parallel–Load Mode

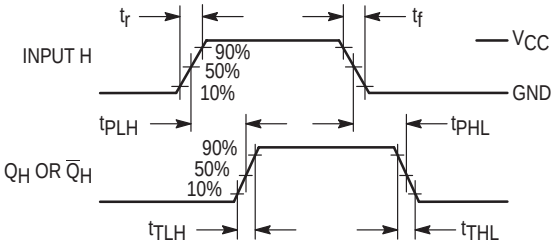


Figure 3. Parallel–Load Mode

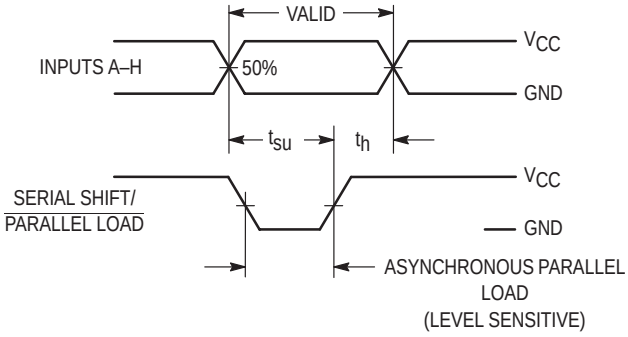


Figure 4. Parallel–Load Mode

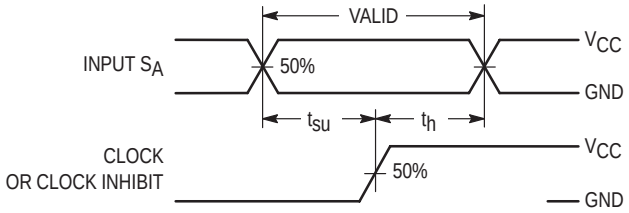


Figure 5. Serial–Shift Mode

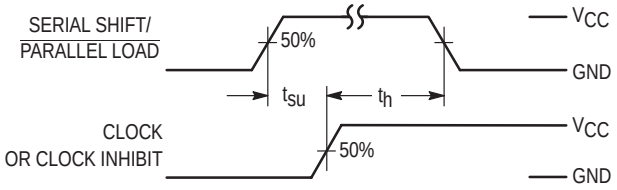


Figure 6. Serial–Shift Mode

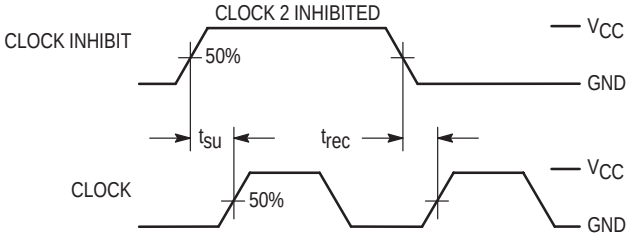
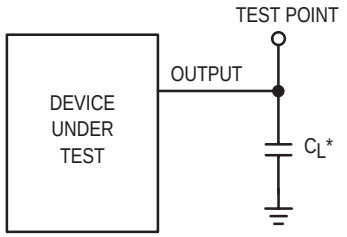


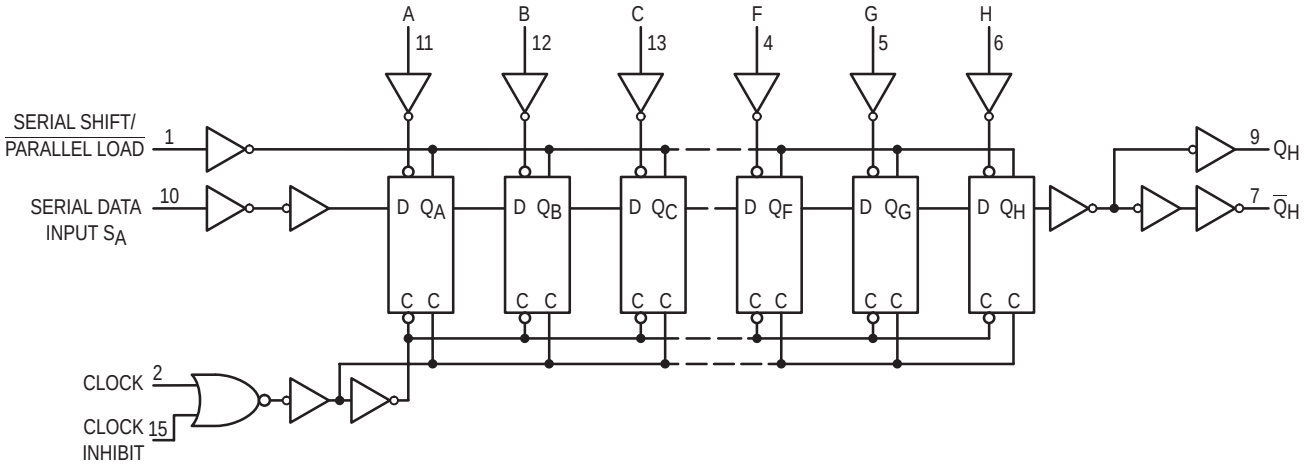
Figure 7. Serial–Shift, Clock–Inhibit Mode



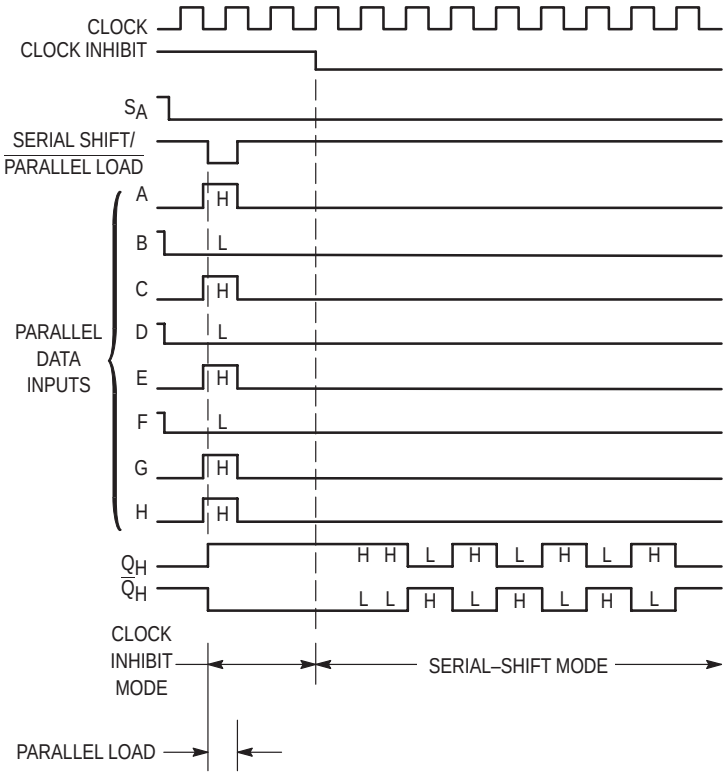
*Includes all probe and jig capacitance

Figure 8. Test Circuit

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM



MC74HC174A

Hex D Flip-Flop with Common Clock and Reset

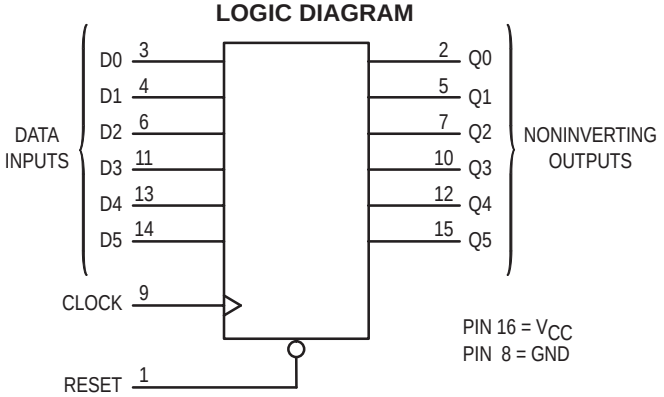
High–Performance Silicon–Gate CMOS

The MC74HC174A is identical in pinout to the LS174. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six D flip–flops with common Clock and Reset inputs. Each flip–flop is loaded with a low–to–high transition of the Clock input. Reset is asynchronous and active–low.

- Output Drive Capability: 10 LSTTL Loads
- TTL NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 162 FETs or 40.5 Equivalent Gates

LOGIC DIAGRAM



FUNCTION TABLE

Inputs			Output
Reset	Clock	D	Q
L	X	X	L
H	↗	H	H
H	↗	L	L
H	L	X	No Change
H	↘	X	No Change

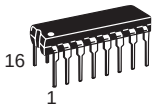
Design Criteria	Value	Units
Internal Gate Count*	40.5	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	.0075	pJ

*Equivalent to a two–input NAND gate.

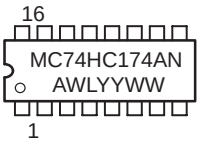
ON Semiconductor

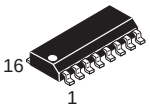
http://onsemi.com

MARKING DIAGRAMS

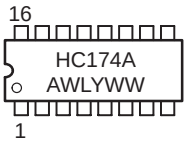


PDIP–16
N SUFFIX
CASE 648



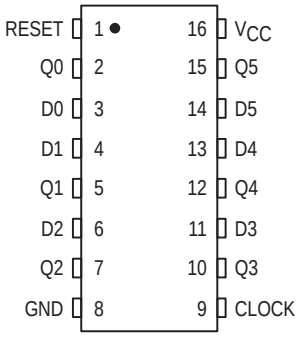


SO–16
D SUFFIX
CASE 751B



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HC174AN	PDIP–16	2000 / Box
MC74HC174AD	SOIC–16	48 / Rail
MC74HC174ADR2	SOIC–16	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 1.5 to V_{CC} + 1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 4.0 mA $\|I_{out}\|$ ≤ 5.2 mA	 4.5 6.0	 3.98 5.48	 3.84 5.34	 3.7 5.2	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 4.0 mA $\|I_{out}\|$ ≤ 5.2 mA	 4.5 6.0	 0.26 0.26	 0.33 0.33	 0.4 0.4	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0 μA	6.0	4.0	40	160	μA

NOTES:
1. Information on typical parametric values along with high frequency or heavy load considerations, can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).
2. Total Supply Current = $I_{CC} + S\Delta I_{CC}$.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t_{PLH} t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
t_{PLH} t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0 4.5 6.0	110 21 19	140 28 24	160 32 27	ns
t_{TLH} t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

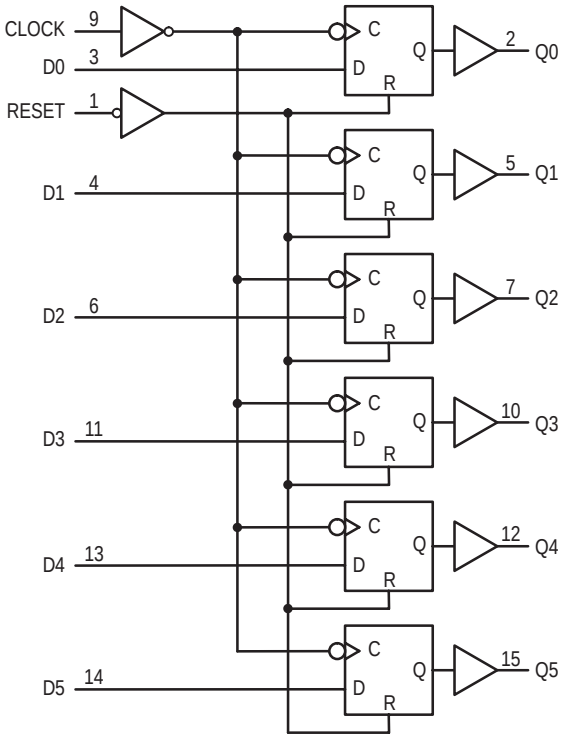
		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	62	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Fig.	V_{CC} V	Guaranteed Limit						Unit
				– 55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
t_{su}	Minimum Setup Time, Data to Clock	3	2.0 4.5 6.0	50 10 9.0		65 13 11		75 15 13		ns
t_h	Minimum Hold Time, Clock to Data	3	2.0 4.5 6.0	5.0 5.0 5.0		5.0 5.0 5.0		5.0 5.0 5.0		ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock	2	2.0 4.5 6.0	5.0 5.0 5.0		5.0 5.0 5.0		5.0 5.0 5.0		ns
t_w	Minimum Pulse Width, Clock	1	2.0 4.5 6.0	75 15 13		95 19 16		110 22 19		ns
t_w	Minimum Pulse Width, Reset	2	2.0 4.5 6.0	75 15 13		95 19 16		110 22 19		ns
t_r, t_f	Maximum Input Rise and Fall Times	1	2.0 4.5 6.0		1000 500 400		1000 500 400		1000 500 400	ns

EXPANDED LOGIC DIAGRAM



SWITCHING WAVEFORMS

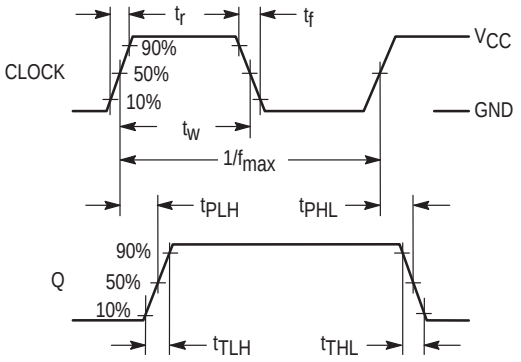


Figure 1.

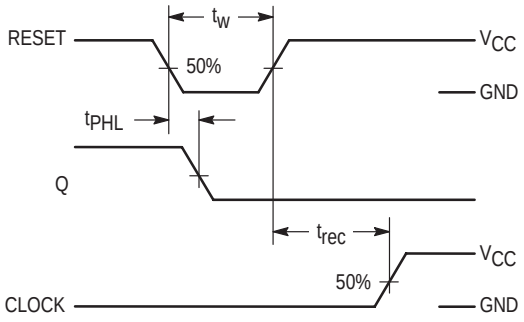


Figure 2.

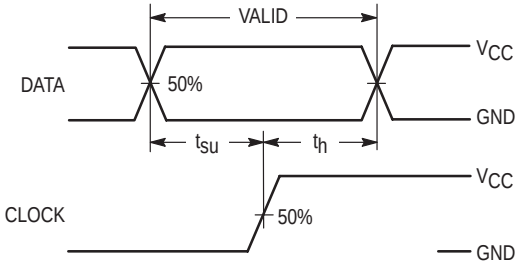
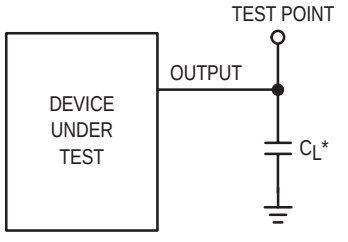


Figure 3.



*Includes all probe and jig capacitance

Figure 4. Test Circuit

MC74HC175A

Quad D Flip-Flop with Common Clock and Reset

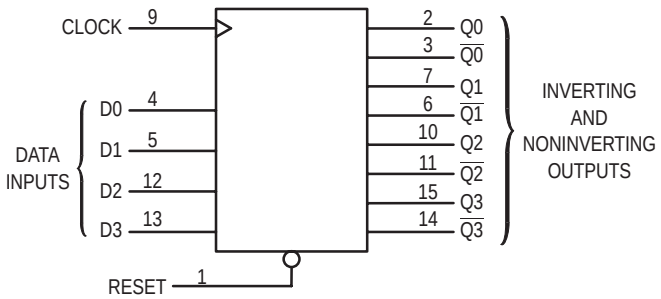
High–Performance Silicon–Gate CMOS

The MC74HC175A is identical in pinout to the LS175. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of four D flip–flops with common Reset and Clock inputs, and separate D inputs. Reset (active–low) is asynchronous and occurs when a low level is applied to the Reset input. Information at a D input is transferred to the corresponding Q output on the next positive going edge of the Clock input.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity 166 FETs or 41.5 Equivalent Gates

LOGIC DIAGRAM



PIN 16 = V_{CC}
PIN 8 = GND

FUNCTION TABLE

Inputs			Outputs	
Reset	Clock	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	No Change	

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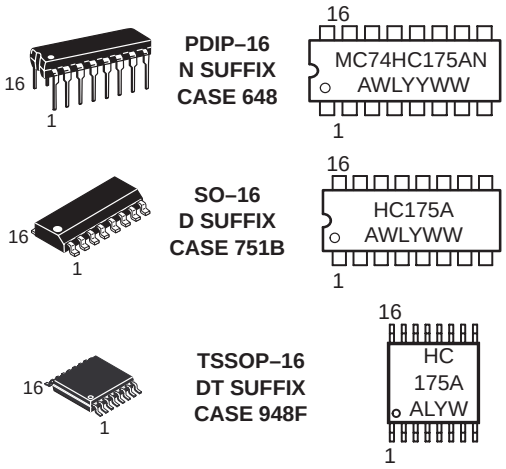
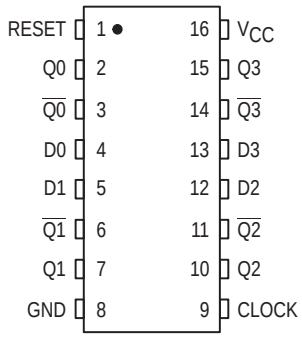
MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HC175AN	PDIP–16	2000 / Box
MC74HC175AD	SOIC–16	48 / Rail
MC74HC175ADR2	SOIC–16	2500 / Reel
MC74HC175ADT	TSSOP–16	96 / Rail
MC74HC175ADTR2	TSSOP–16	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 600 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4 2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.80	0.5 0.9 1.35 1.80	0.5 0.9 1.35 1.80	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 4.0 mA $\|I_{out}\|$ ≤ 5.2 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 2.4$ mA $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 3.0 4.5 6.0	6 10 30 35	4.8 8.0 24 28	4 6 20 24	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figures 1 and 4)	2.0 3.0 4.5 6.0	150 75 26 22	190 90 32 28	225 110 38 33	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q or $\overline{Q}$ (Figures 2 and 4)	2.0 3.0 4.5 6.0	125 70 22 19	155 85 27 24	190 110 34 30	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, $V_{CC} = 5.0$ V	
C_{PD}	Power Dissipation Capacitance (Per Flip–Flop)*	35	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Data to Clock (Figure 3)	2.0 3.0 4.5 6.0	100 45 20 17	125 65 25 21	150 85 30 26	ns
t_h	Minimum Hold Time, Clock to Data (Figure 3)	2.0 3.0 4.5 6.0	5 3 3 3	5 3 3 3	5 3 3 3	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 3.0 4.5 6.0	100 45 20 17	125 65 25 21	150 85 30 26	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 3.0 4.5 6.0	80 45 16 14	100 65 20 17	120 85 24 20	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 3.0 4.5 6.0	80 45 16 14	100 65 20 17	120 85 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

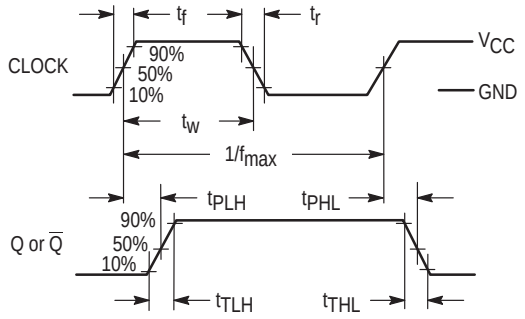


Figure 1.

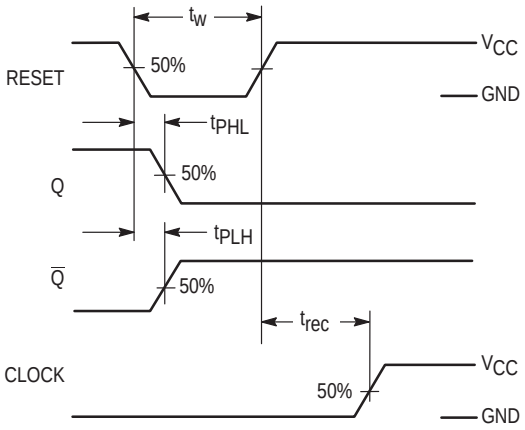


Figure 2.

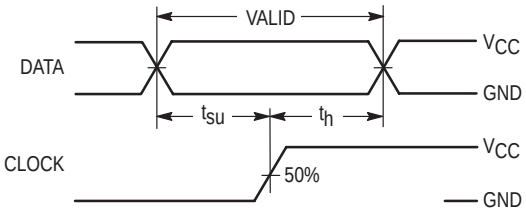
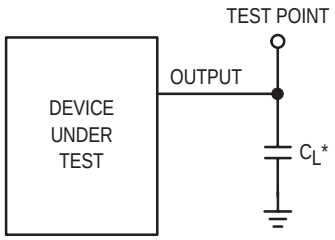


Figure 3.

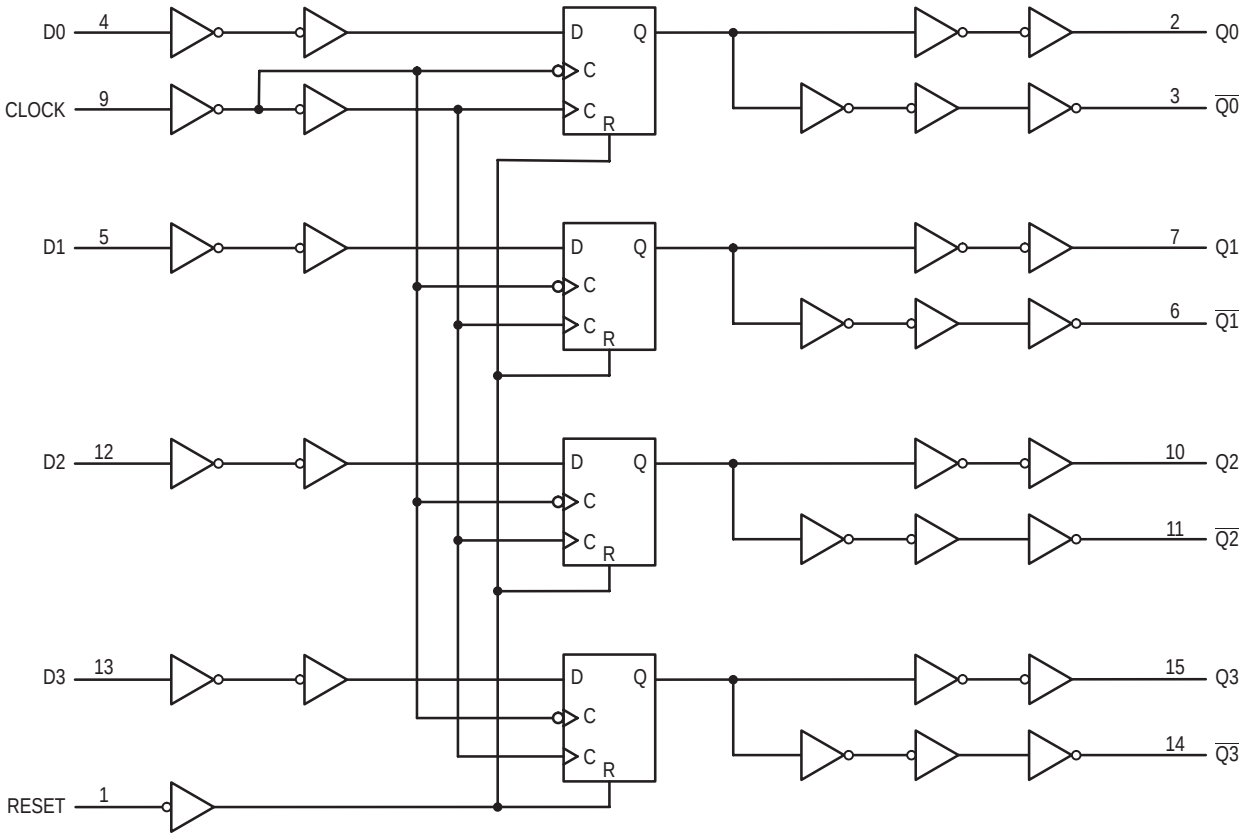
TEST CIRCUIT



*Includes all probe and jig capacitance

Figure 4.

EXPANDED LOGIC DIAGRAM



MC74HC240A

Octal 3-State Inverting Buffer/Line Driver/Line Receiver

High–Performance Silicon–Gate CMOS

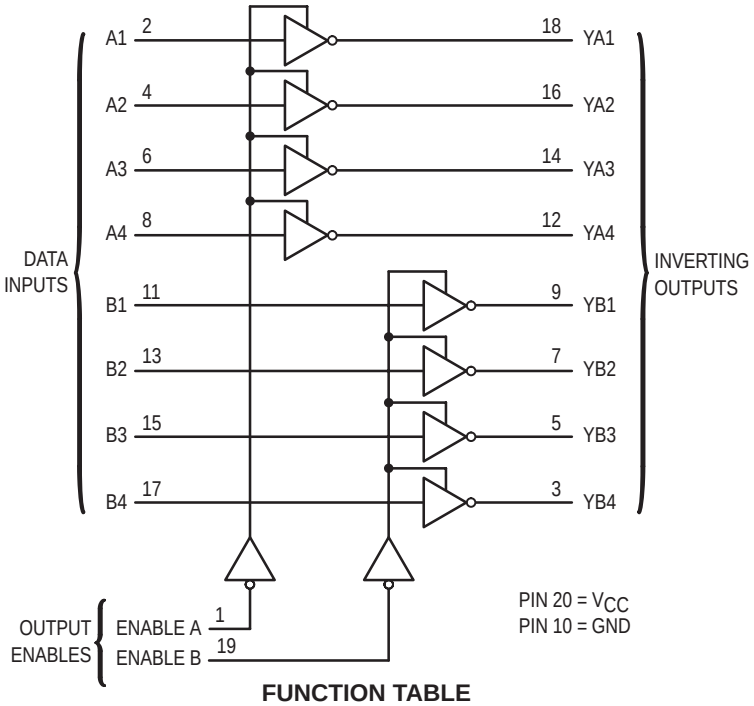
The MC74HC240A is identical in pinout to the LS240. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This octal noninverting buffer/line driver/line receiver is designed to be used with 3–state memory address drivers, clock drivers, and other sub–oriented systems. The device has inverting outputs and two active–low output enables.

The HC240A is similar in function to the HC244A.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 120 FETs or 30 Equivalent Gates

LOGIC DIAGRAM



FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A, B	YA, YB
L	L	H
L	H	L
H	X	Z

Z = high impedance

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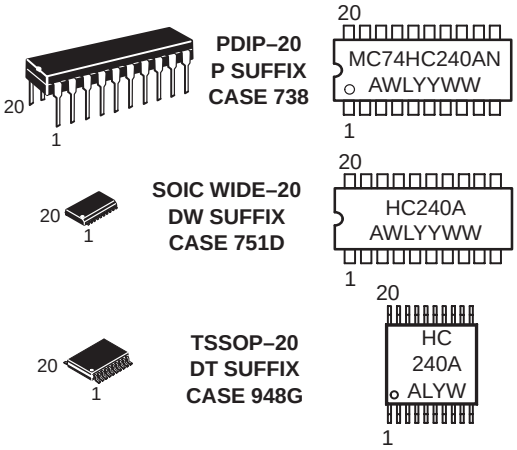
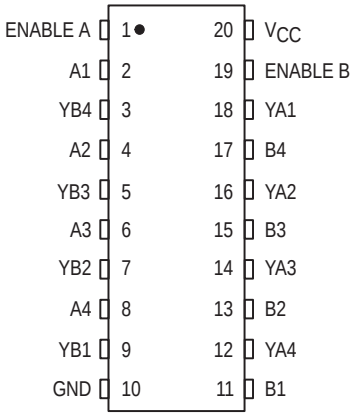
MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HC240AN	PDIP–20	1440 / Box
MC74HC240ADW	SOIC–WIDE	38 / Rail
MC74HC240ADWR2	SOIC–WIDE	1000 / Reel
MC74HC240ADT	TSSOP–20	75 / Rail
MC74HC240ADTR2	TSSOP–20	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0 μA	6.0	4.0	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	2.0 3.0 4.5 6.0	80 40 16 14	100 50 20 17	120 60 24 20	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0 3.0 4.5 6.0	110 60 22 19	140 70 28 24	165 80 33 28	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0 3.0 4.5 6.0	110 60 22 19	140 70 28 24	165 80 33 28	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 3.0 4.5 6.0	60 23 12 10	75 27 15 13	90 32 18 15	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)	—	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Transceiver Channel)*	32	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

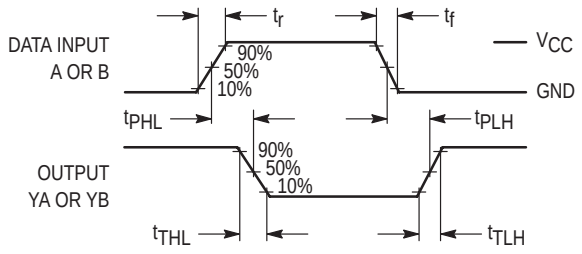


Figure 1.

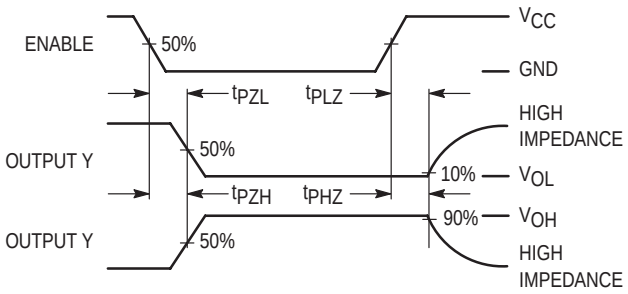
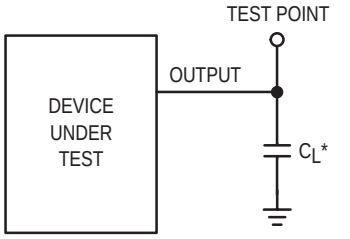
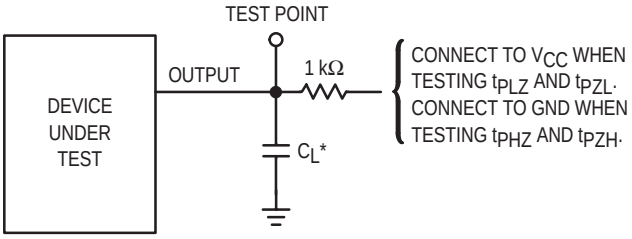


Figure 2.



*Includes all probe and jig capacitance

Figure 3. Test Circuit



*Includes all probe and jig capacitance

Figure 4. Test Circuit

PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, B1, B2, B3, B4
(Pins 2, 4, 6, 8, 11, 13, 15, 17)

Data input pins. Data on these pins appear in inverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROLS

Enable A, Enable B (Pins 1, 19)

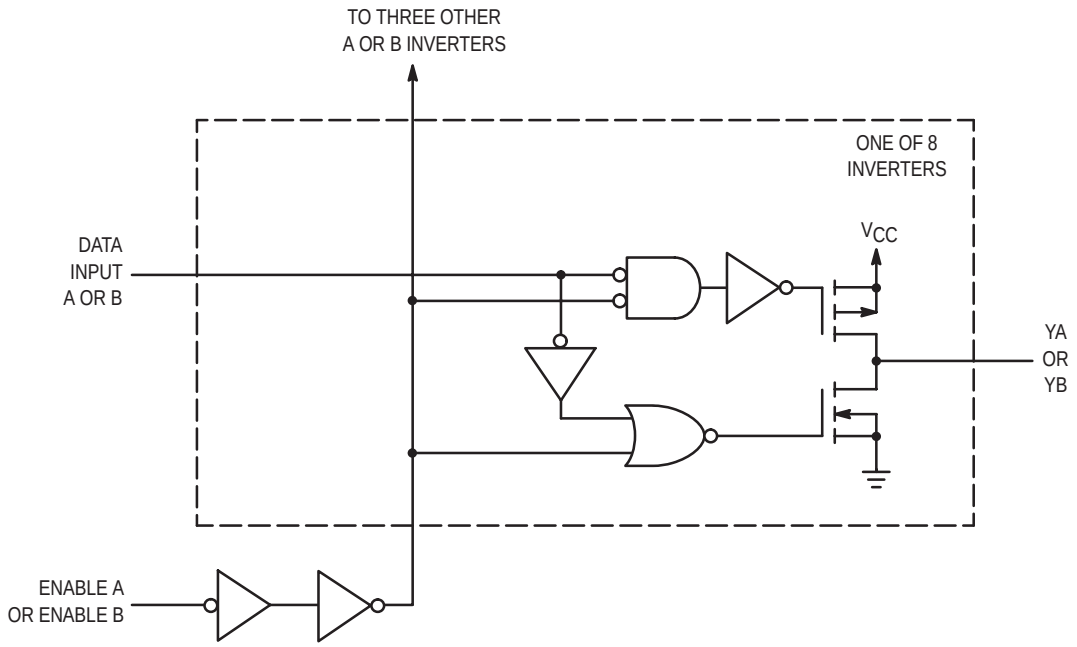
Output enables (active–low). When a low level is applied to these pins, the outputs are enabled and the devices function as inverters. When a high level is applied, the outputs assume the high–impedance state.

OUTPUTS

YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4
(Pins 18, 16, 14, 12, 9, 7, 5, 3)

Device outputs. Depending upon the state of the output–enable pins, these outputs are either inverting outputs or high–impedance outputs.

LOGIC DETAIL



MC74HC244A

Octal 3-State Noninverting Buffer/Line Driver/ Line Receiver

High–Performance Silicon–Gate CMOS

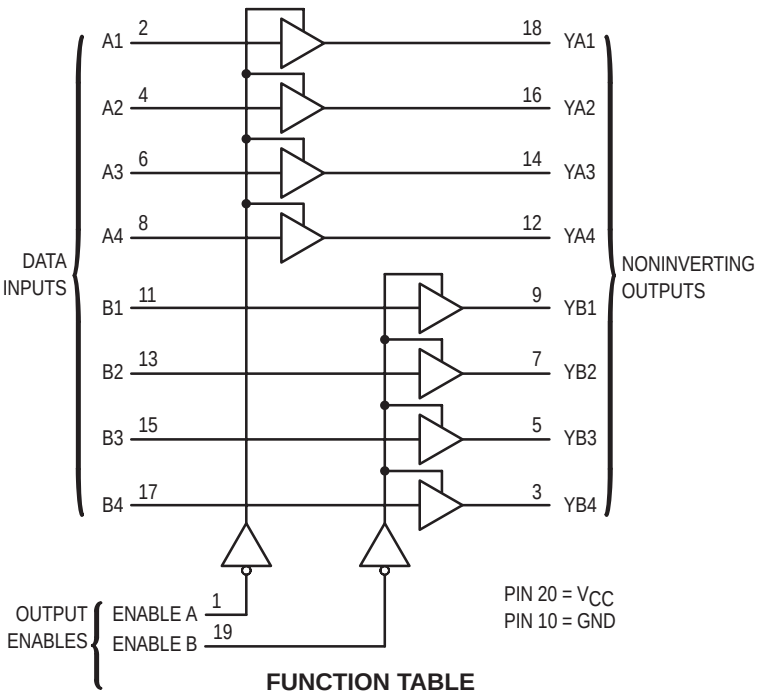
The MC74HC244A is identical in pinout to the LS244. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This octal noninverting buffer/line driver/line receiver is designed to be used with 3–state memory address drivers, clock drivers, and other bus–oriented systems. The device has noninverting outputs and two active–low output enables.

The HC244A is similar in function to the HC240A.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 136 FETs or 34 Equivalent Gates

LOGIC DIAGRAM



FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A, B	YA, YB
L	L	L
L	H	H
H	X	Z

Z = high impedance

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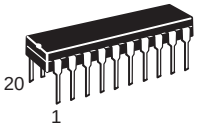
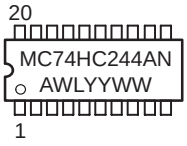
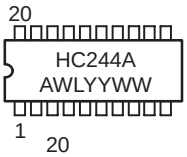
MARKING DIAGRAMS

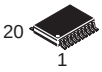


PDIP–20
P SUFFIX
CASE 738



SOIC WIDE–20
DW SUFFIX
CASE 751D

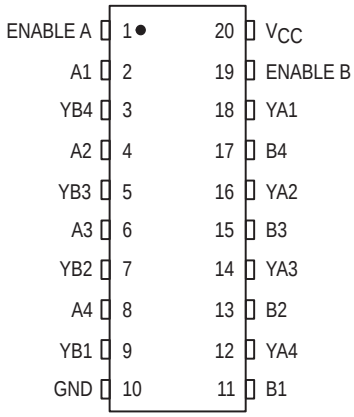




TSSOP–20
DT SUFFIX
CASE 948G

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HC244AN	PDIP–20	1440 / Box
MC74HC244ADW	SOIC–WIDE	38 / Rail
MC74HC244ADWR2	SOIC–WIDE	1000 / Reel
MC74HC244ADT	TSSOP–20	75 / Rail
MC74HC244ADTR2	TSSOP–20	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC, SSOP or TSSOP Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0 μA	6.0	4.0	40	160	μA

NOTE: Information on typical parametric values and high frequency or heavy load considerations can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	2.0 3.0 4.5 6.0	96 50 18 15	115 60 23 20	135 70 27 23	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0 3.0 4.5 6.0	110 60 22 19	140 70 28 24	165 80 33 28	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0 3.0 4.5 6.0	110 60 22 19	140 70 28 24	165 80 33 28	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 3.0 4.5 6.0	60 23 12 10	75 27 15 13	90 32 18 15	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)	—	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Buffer)*	34	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

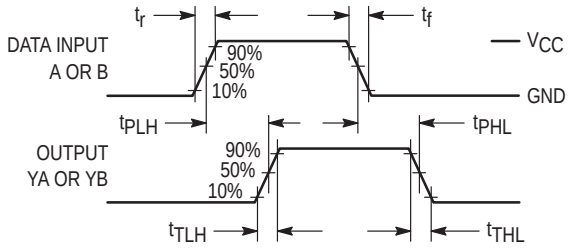


Figure 1.

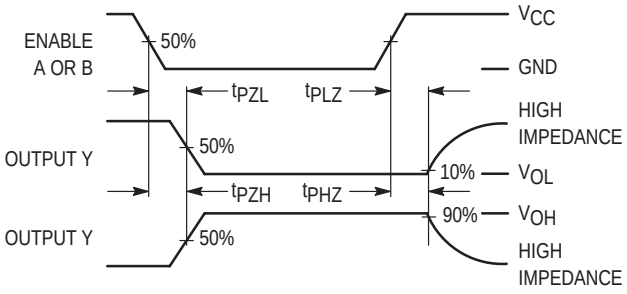
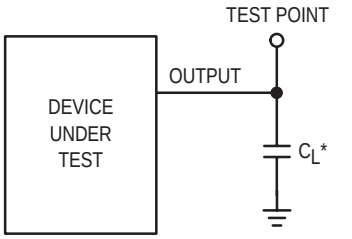


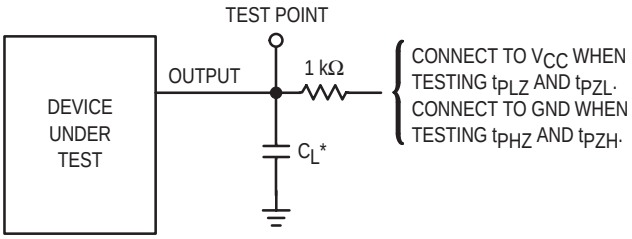
Figure 2.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 3. Test Circuit



*Includes all probe and jig capacitance

Figure 4. Test Circuit

PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, B1, B2, B3, B4
(Pins 2, 4, 6, 8, 11, 13, 15, 17)

Data input pins. Data on these pins appear in noninverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROLS

Enable A, Enable B (Pins 1, 19)

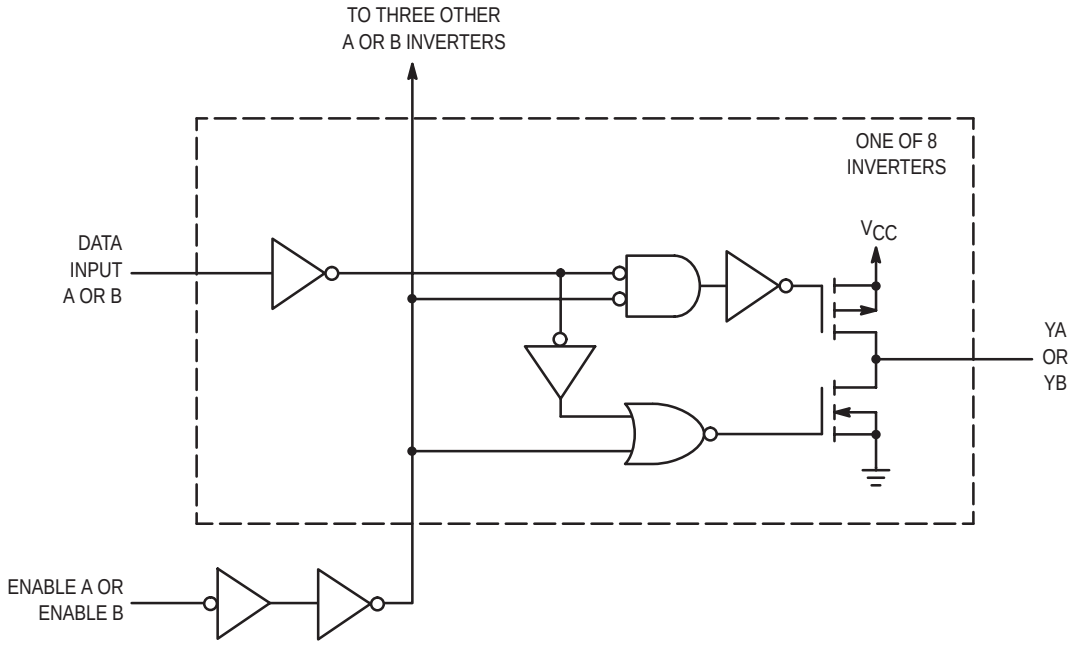
Output enables (active–low). When a low level is applied to these pins, the outputs are enabled and the devices function as noninverting buffers. When a high level is applied, the outputs assume the high impedance state.

OUTPUTS

YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4
(Pins 18, 16, 14, 12, 9, 7, 5, 3)

Device outputs. Depending upon the state of the output–enable pins, these outputs are either noninverting outputs or high–impedance outputs.

LOGIC DETAIL



MC74HCT244A

Octal 3-State Noninverting Buffer/Line Driver/ Line Receiver with LSTTL-Compatible Inputs

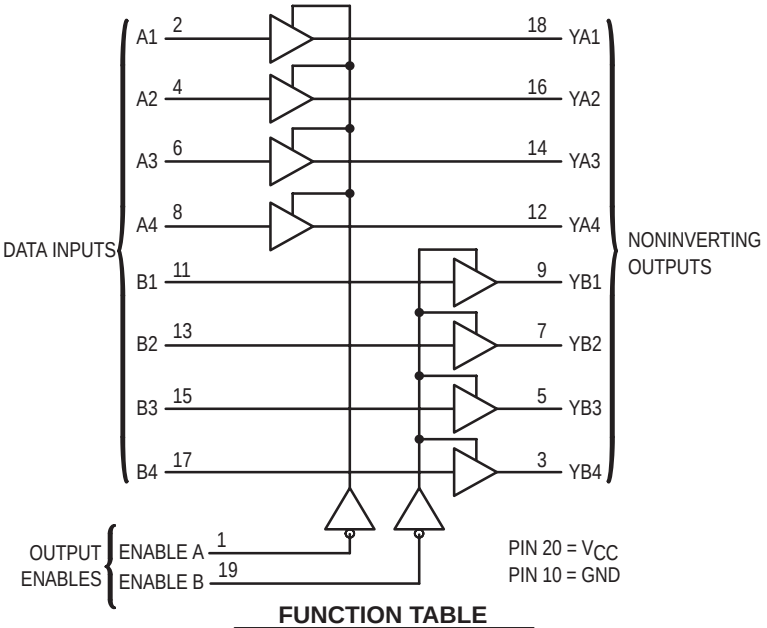
High–Performance Silicon–Gate CMOS

The MC74HCT244A is identical in pinout to the LS244. This device may be used as a level converter for interfacing TTL or NMOS outputs to High–Speed CMOS inputs. The HCT244A is an octal noninverting buffer line driver line receiver designed to be used with 3–state memory address drivers, clock drivers, and other bus–oriented systems. The device has non–inverted outputs and two active–low output enables.

The HCT244A is the noninverting version of the HCT240. See also HCT241.

- Output Drive Capability: 15 LSTTL Loads
- TTL NMOS–Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 112 FETs or 28 Equivalent Gates

LOGIC DIAGRAM



FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A, B	YA, YB
L	L	L
L	H	H
H	X	Z

Z = high impedance, X = don't care

ON Semiconductor

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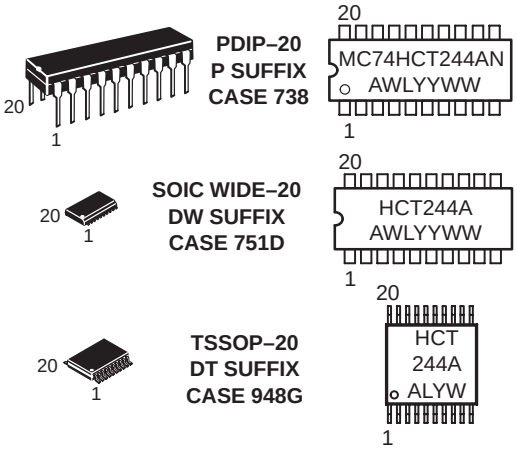
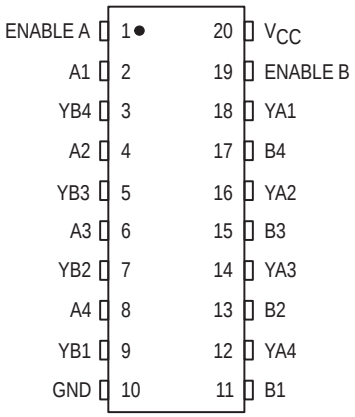
MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HCT244AN	PDIP–20	1440 / Box
MC74HCT244ADW	SOIC–WIDE	38 / Rail
MC74HCT244ADWR2	SOIC–WIDE	1000 / Reel
MC74HCT244ADT	TSSOP–20	75 / Rail
MC74HCT244ADTR2	TSSOP–20	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC, SSOP or TSSOP Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	2 2	2 2	2 2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6 mA	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6 mA	4.5	0.26	0.33	0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	5.5	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	5.5	4	40	160	μA

ΔI_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4 V, Any One Input V_{in} = V_{CC} or GND, Other Inputs I_{out} = 0 μA	5.5	≥ **–55°C** 2.9	**25°C to 125°C** 2.4	mA

NOTES:
1. Information on typical parametric values along with frequency or heavy load considerations can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).
2. Total Supply Current = $I_{CC} + \Sigma\Delta I_{CC}$.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		– 55 to 25°C	≤ **85°C**	≤ **125°C**	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	20	25	30	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	26	33	39	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	22	28	33	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	55	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

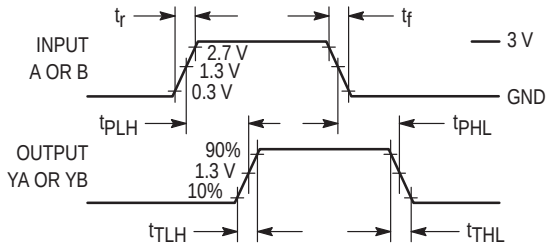


Figure 1.

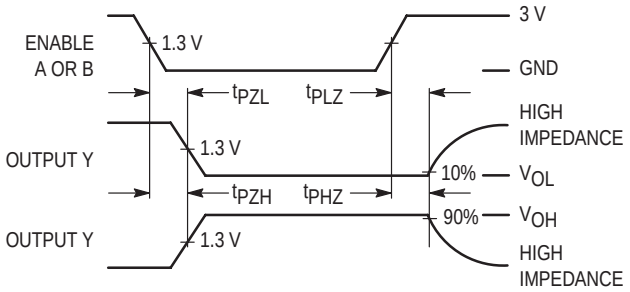
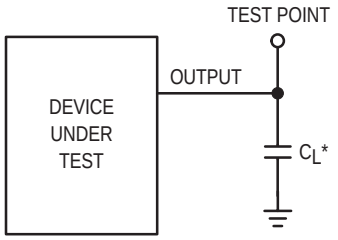


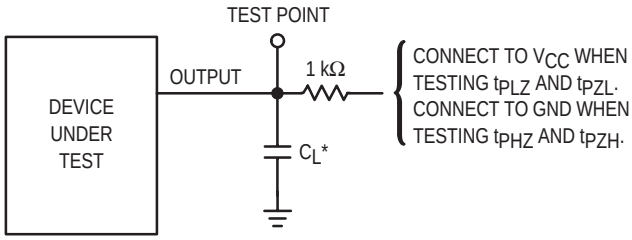
Figure 2.

TEST CIRCUITS



*Includes all probe and jig capacitance

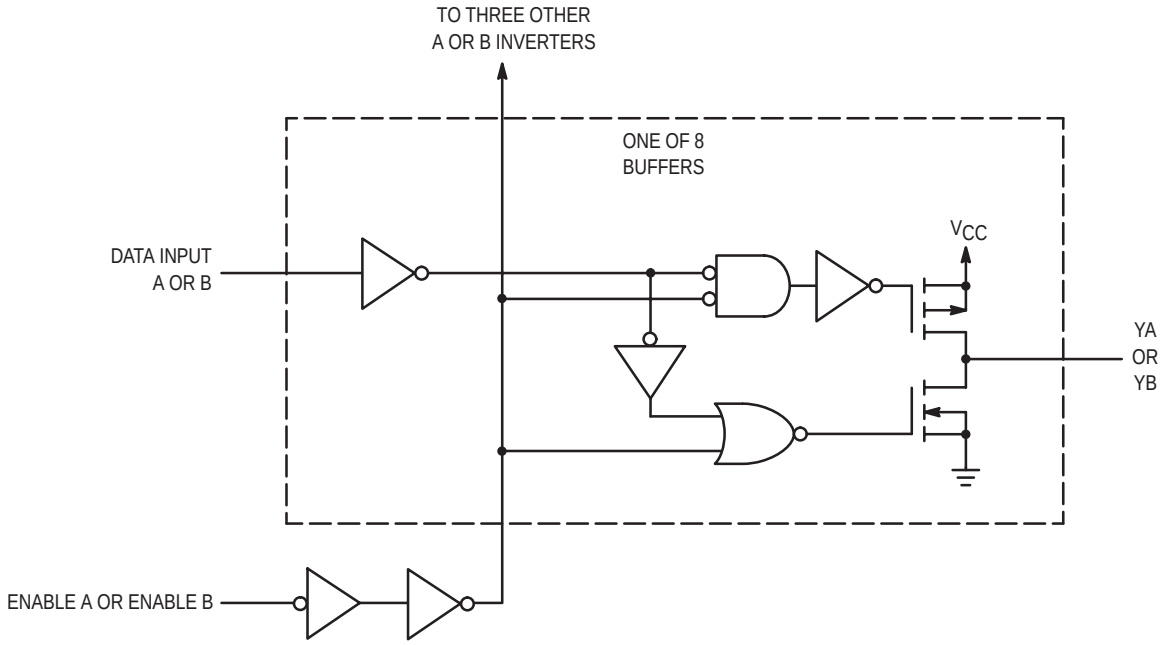
Figure 3.



*Includes all probe and jig capacitance

Figure 4.

LOGIC DETAIL



MC74HC245A

Octal 3-State Noninverting Bus Transceiver

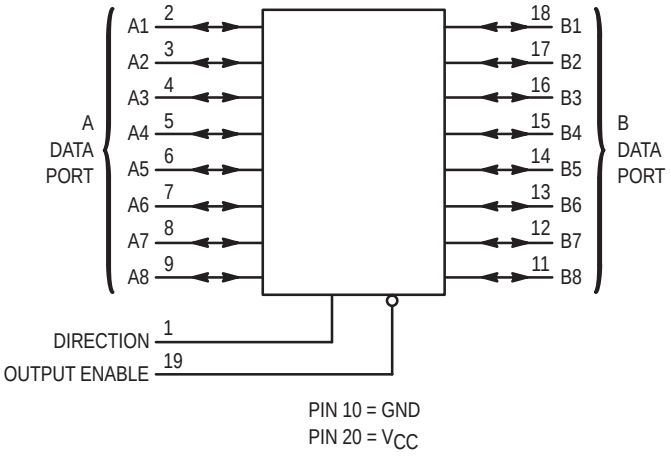
High–Performance Silicon–Gate CMOS

The MC74HC245A is identical in pinout to the LS245. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC245A is a 3–state noninverting transceiver that is used for 2–way asynchronous communication between data buses. The device has an active–low Output Enable pin, which is used to place the I/O ports into high–impedance states. The Direction control determines whether data flows from A to B or from B to A.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 308 FETs or 77 Equivalent Gates

LOGIC DIAGRAM



FUNCTION TABLE

Control Inputs		Operation
Output Enable	Direction	
L	L	Data Transmitted from Bus B to Bus A
L	H	Data Transmitted from Bus A to Bus B
H	X	Buses Isolated (High–Impedance State)

X = don't care

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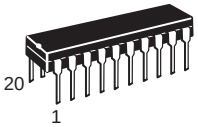
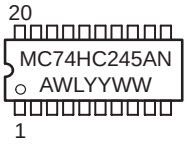
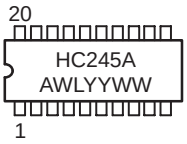
MARKING DIAGRAMS



PDIP–20
P SUFFIX
CASE 738

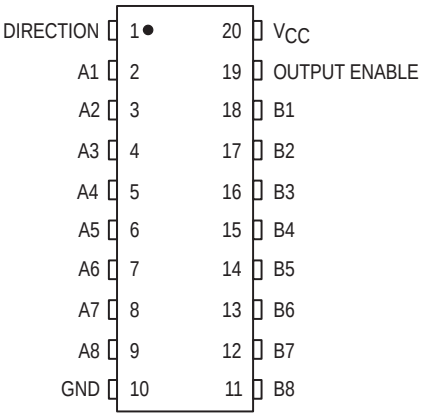


SOIC WIDE–20
DW SUFFIX
CASE 751D



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HC245AN	PDIP–20	1440 / Box
MC74HC245ADW	SOIC–WIDE	38 / Rail
MC74HC245ADWR2	SOIC–WIDE	1000 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
$V_{I/O}$	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
$I_{I/O}$	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1) V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0 μA	6.0	4.0	40	160	μA

NOTE: Information on typical parametric values and high frequency or heavy load considerations can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to B, B to A (Figures 1 and 3)	2.0 3.0 4.5 6.0	75 55 15 13	95 70 19 16	110 80 22 19	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	2.0 3.0 4.5 6.0	110 90 22 19	140 110 28 24	165 130 33 28	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to A or B (Figures 2 and 4)	2.0 3.0 4.5 6.0	110 90 22 19	140 110 28 24	165 130 33 28	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 3.0 4.5 6.0	60 23 12 10	75 27 15 13	90 32 18 15	ns
C_{in}	Maximum Input Capacitance (Pin 1 or Pin 19)	—	10	10	10	pF
C_{out}	Maximum Three–State I/O Capacitance (I/O in High–Impedance State)	—	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Transceiver Channel)*	40	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

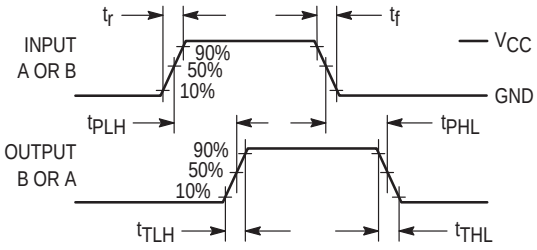


Figure 1.

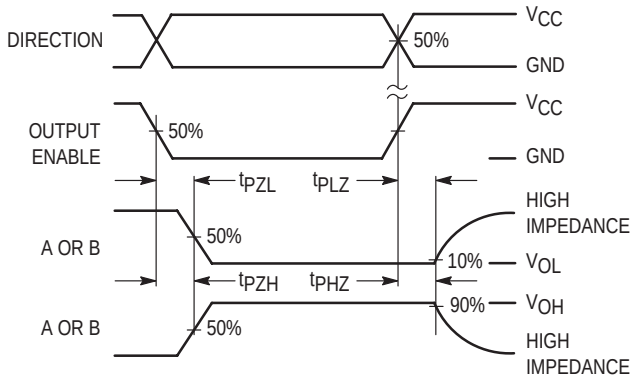
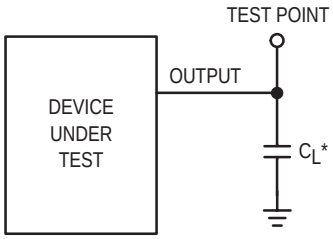


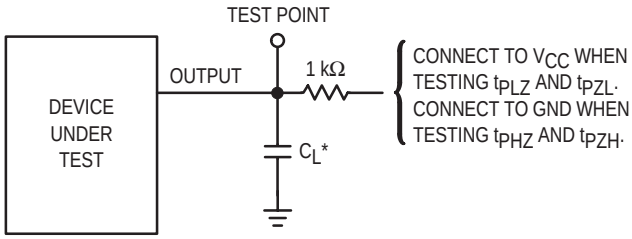
Figure 2.

TEST CIRCUITS



*Includes all probe and jig capacitance

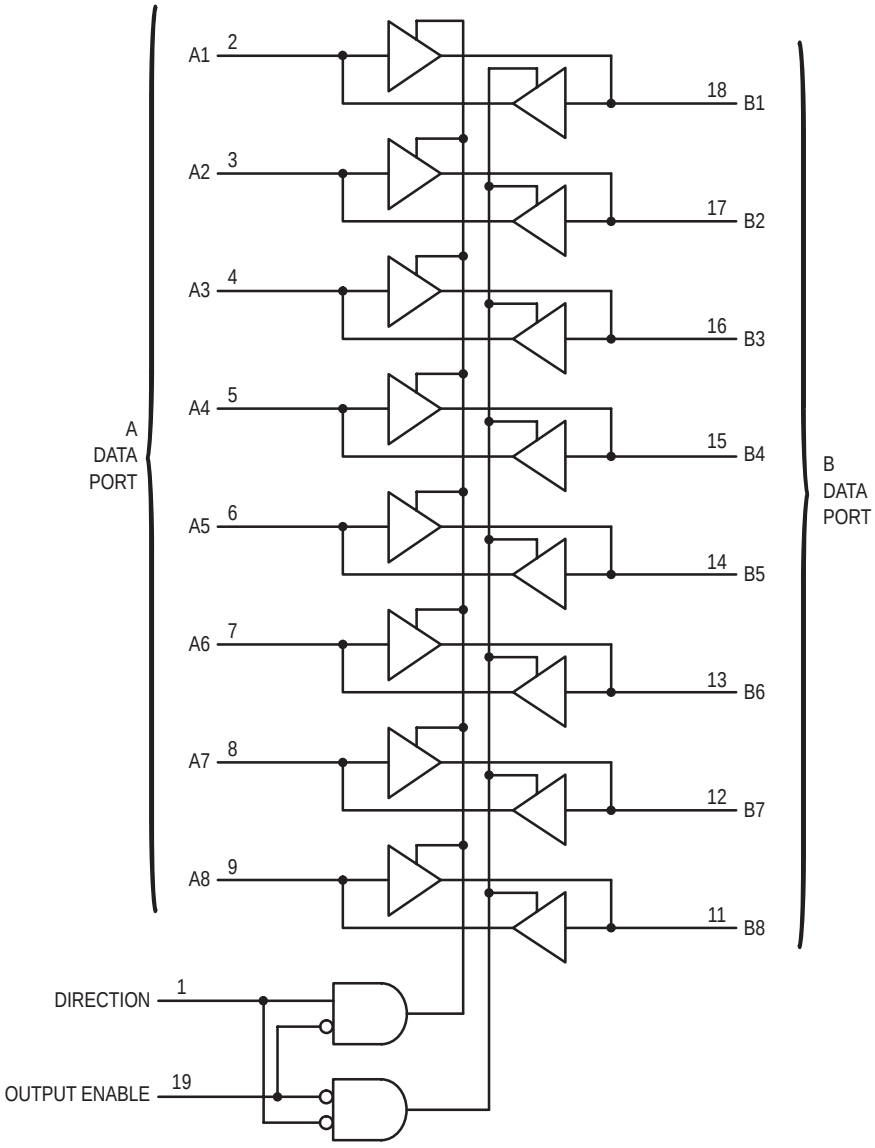
Figure 3.



*Includes all probe and jig capacitance

Figure 4.

EXPANDED LOGIC DIAGRAM



MC74HCT245A

Octal 3-State Noninverting Bus Transceiver with LSTTL Compatible Inputs

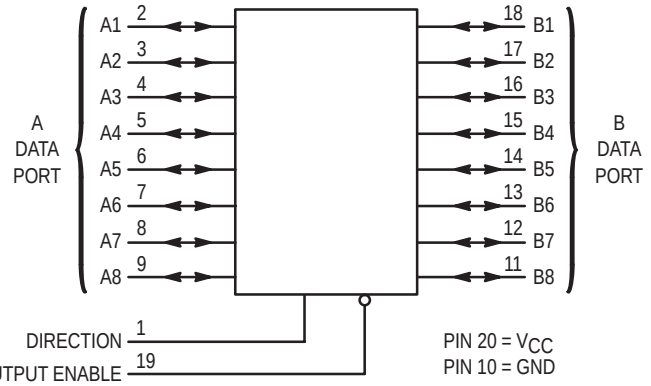
High–Performance Silicon–Gate CMOS

The MC74HCT245A is identical in pinout to the LS245. This device may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

The MC74HCT245A is a 3–state noninverting transceiver that is used for 2–way asynchronous communication between data buses. The device has an active–low Output Enable pin, which is used to place the I/O ports into high–impedance states. The Direction control determines whether data flows from A to B or from B to A.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 304 FETs or 76 Equivalent Gates

LOGIC DIAGRAM



Design Criteria	Value	Units
Internal Gate Count*	76	ea
Internal Gate Propagation Delay	1.0	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	0.005	pJ

*Equivalent to a two–input NAND gate.

FUNCTION TABLE

Control Inputs		
Output Enable	Direction	Operation
L	L	Data Transmitted from Bus B to Bus A
L	H	Data Transmitted from Bus A to Bus B
H	X	Buses Isolated (High–Impedance State)

X = Don't Care

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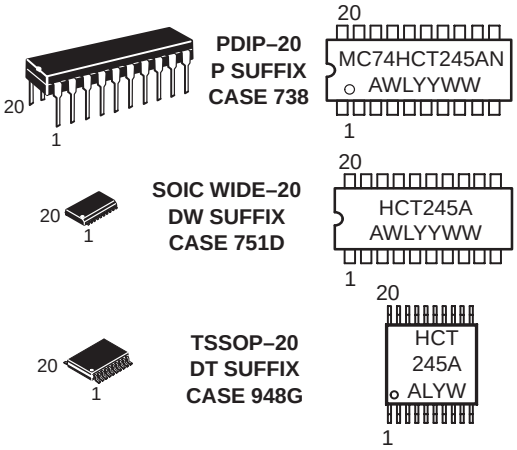
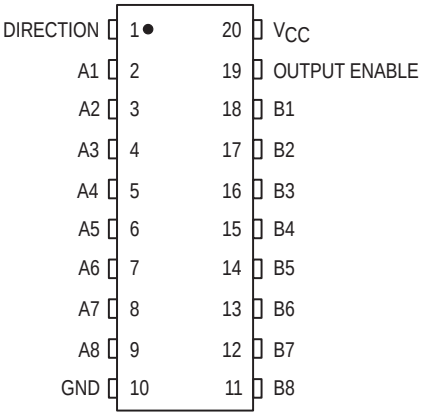
MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HCT245AN	PDIP–20	1440 / Box
MC74HCT245ADW	SOIC–WIDE	38 / Rail
MC74HCT245ADWR2	SOIC–WIDE	1000 / Reel
MC74HCT245ADT	TSSOP–20	75 / Rail
MC74HCT245ADTR2	TSSOP–20	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC, SSOP or TSSOP Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6.0 mA	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6.0 mA	4.5	0.26	0.33	0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND, Pins 1 or 19	5.5	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	5.5	4.0	40	160	μA
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND, I/O Pins	5.5	± 0.5	± 5.0	± 10	μA
ΔI_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4 V, Any One Input V_{in} = V_{CC} or GND, Other Inputs I_{out} = 0 μA	5.5	≥ –55°C 2.9		25°C to 125°C 2.4	mA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to B or B to A (Figures 1 and 3)	22	28	33	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	30	36	42	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to A or 8 (Figures 2 and 4)	30	36	42	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time. any Output (Figures 1 and 3)	12	15	18	ns
C_{in}	Maximum Input Capacitance (Pin 1 or 19)	10	10	10	pF
C_{out}	Maximum Three–State I/O Capacitance, (I/O in High–Impedance State)	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	97	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

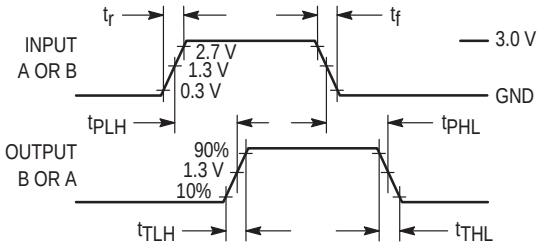


Figure 1.

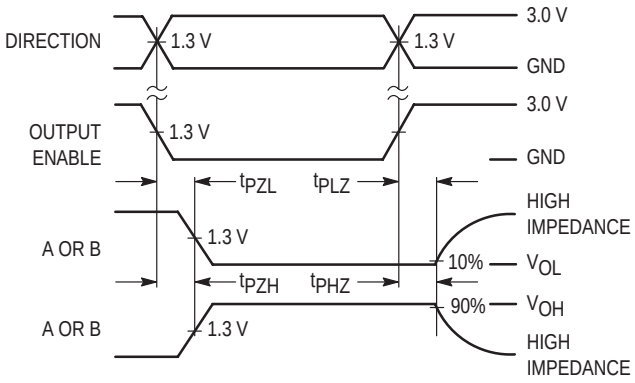
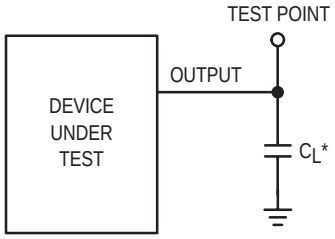
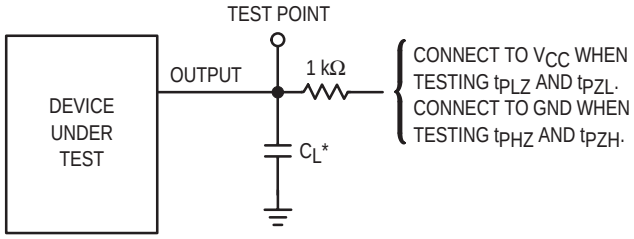


Figure 2.



*Includes all probe and jig capacitance

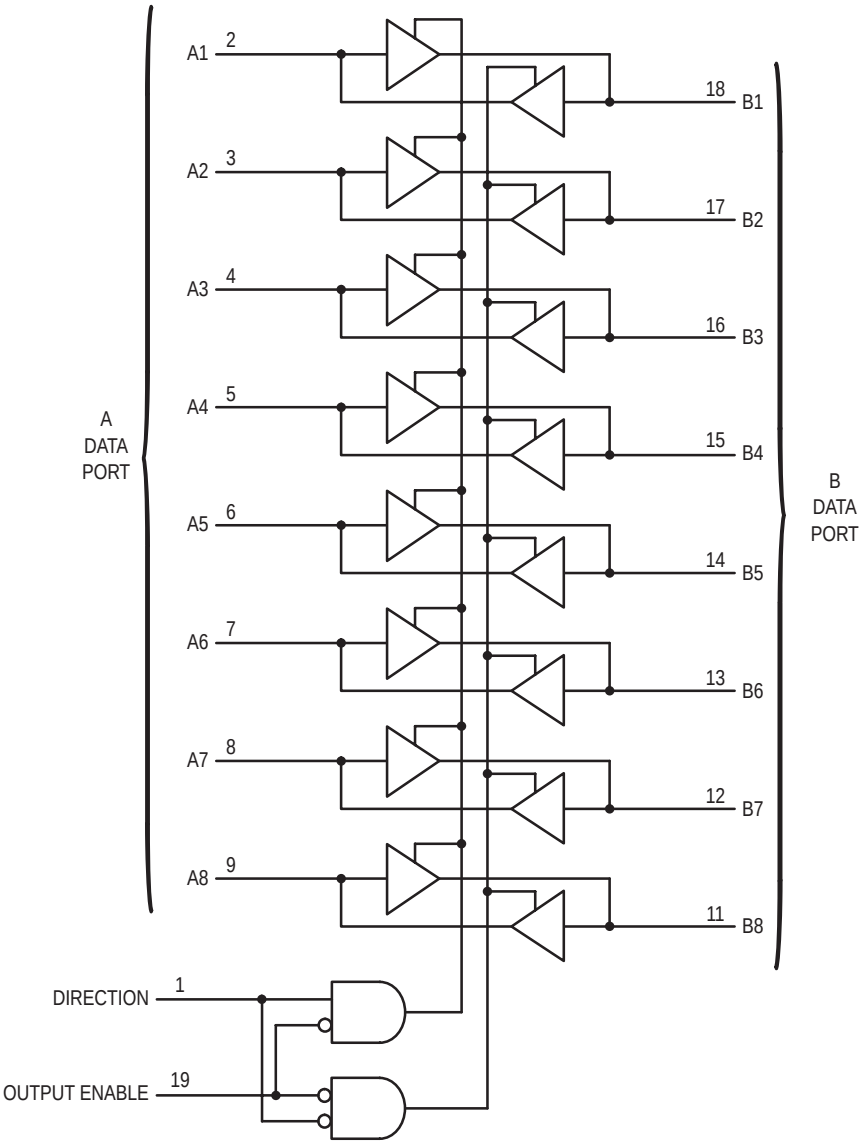
Figure 3.



*Includes all probe and jig capacitance

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM



MC74HC273A

Octal D Flip-Flop with Common Clock and Reset

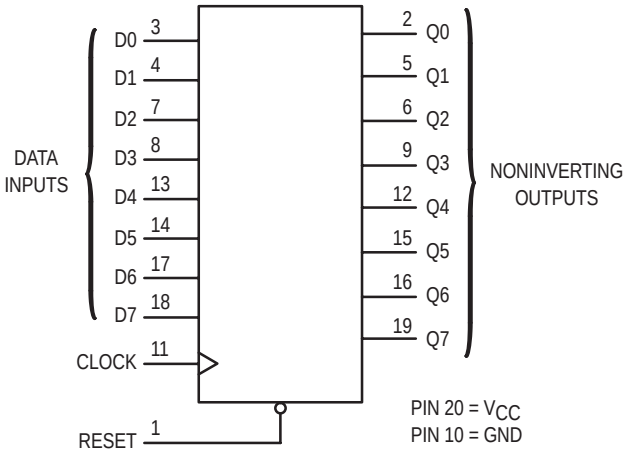
High–Performance Silicon–Gate CMOS

The MC74HC273A is identical in pinout to the LS273. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of eight D flip–flops with common Clock and Reset inputs. Each flip–flop is loaded with a low–to–high transition of the Clock input. Reset is asynchronous and active low.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 264 FETs or 66 Equivalent Gates

LOGIC DIAGRAM



FUNCTION TABLE

Inputs			Output
Reset	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	No Change
H	↓	X	No Change

Design Criteria	Value	Units
Internal Gate Count*	66	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	.0075	pJ

*Equivalent to a two–input NAND gate.

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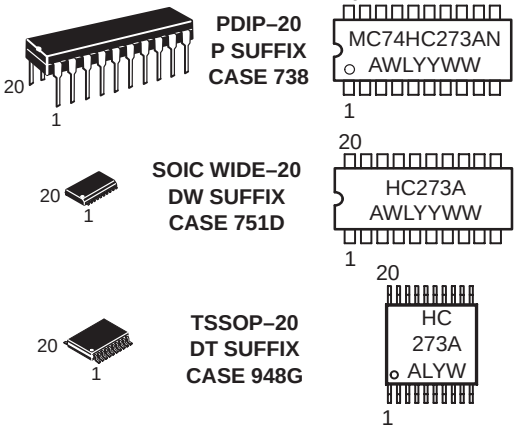
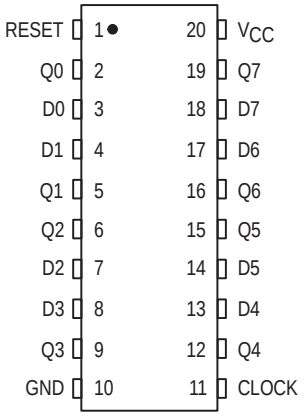
MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HC273AN	PDIP–20	1440 / Box
MC74HC273ADW	SOIC–WIDE	38 / Rail
MC74HC273ADWR2	SOIC–WIDE	1000 / Reel
MC74HC273ADT	TSSOP–20	75 / Rail
MC74HC273ADTR2	TSSOP–20	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0 μA	6.0	4.0	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 3.0 4.5 6.0	6.0 15 30 35	5.0 10 24 28	4.0 8.0 20 24	MHz
t_{PLH} t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0 3.0 4.5 6.0	145 90 29 25	180 120 36 31	220 140 44 38	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0 3.0 4.5 6.0	145 90 29 25	180 120 36 31	220 140 44 38	ns
t_{TLH} t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	48	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Fig.	V_{CC} Volts	Guaranteed Limit						Unit
				– 55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
t_{su}	Minimum Setup Time, Data to Clock	3	2.0 3.0 4.5 6.0	60 23 12 10		75 27 15 13		90 32 18 15		ns
t_h	Minimum Hold Time, Clock to Data	3	2.0 3.0 4.5 6.0	3.0 3.0 3.0 3.0		3.0 3.0 3.0 3.0		3.0 3.0 3.0 3.0		ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock	2	2.0 3.0 4.5 6.0	5.0 5.0 5.0 5.0		5.0 5.0 5.0 5.0		5.0 5.0 5.0 5.0		ns
t_w	Minimum Pulse Width, Clock	1	2.0 3.0 4.5 6.0	60 23 12 10		75 27 15 13		90 32 18 15		ns
t_w	Minimum Pulse Width, Reset	2	2.0 3.0 4.5 6.0	60 23 12 10		75 27 15 13		90 32 18 15		ns
t_r, t_f	Maximum Input Rise and Fall Times	1	2.0 3.0 4.5 6.0		1000 800 500 400		1000 800 500 400		1000 800 500 400	ns

SWITCHING WAVEFORMS

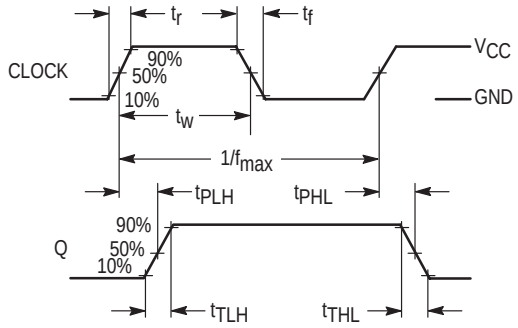


Figure 1.

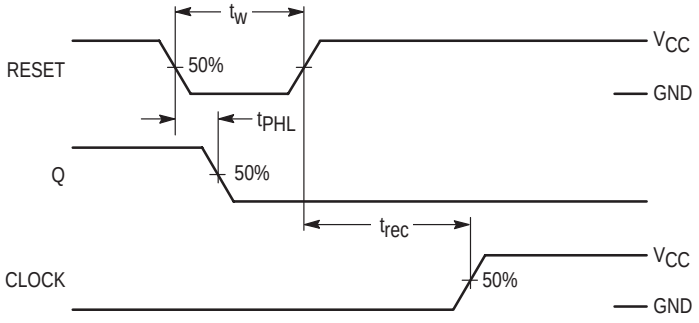


Figure 2.

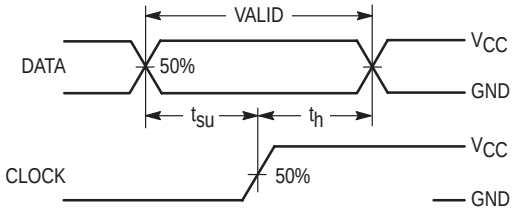
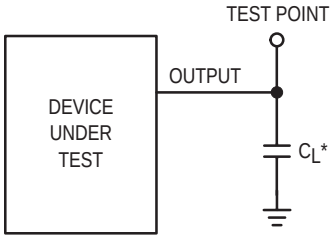


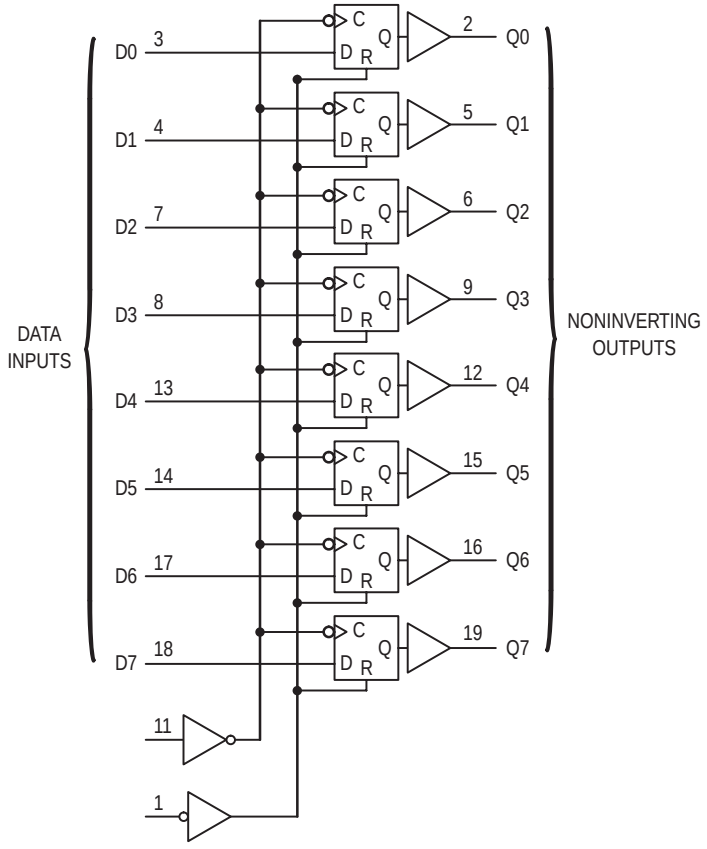
Figure 3.



*Includes all probe and jig capacitance

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM



MC74HCT273A

Octal D Flip-Flop with Common Clock and Reset with LSTTL-Compatible Inputs

High–Performance Silicon–Gate CMOS

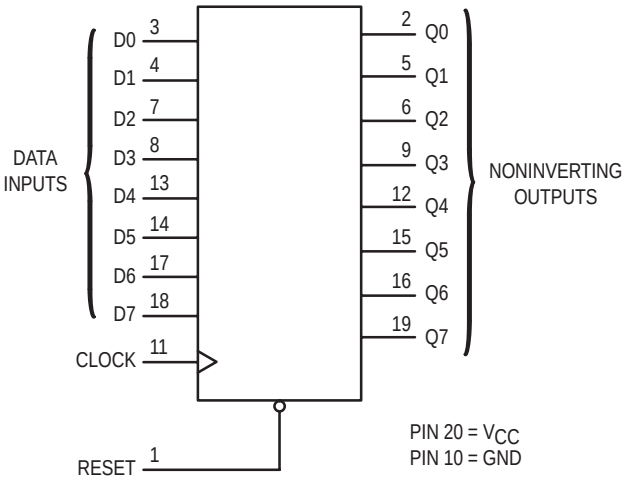
The MC74HCT273A may be used as a level converter for interfacing TTL or NMOS outputs to High–Speed CMOS inputs.

The HCT273A is identical in pinout to the LS273.

This device consists of eight D flip–flops with common Clock and Reset inputs. Each flip–flop is loaded with a low–to–high transition of the Clock input. Reset is asynchronous and active low.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 284 FETs or 71 Equivalent Gates

LOGIC DIAGRAM



FUNCTION TABLE

Inputs			Output
Reset	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	No Change
H	↓	X	No Change

X = Don't Care
Z = High Impedance

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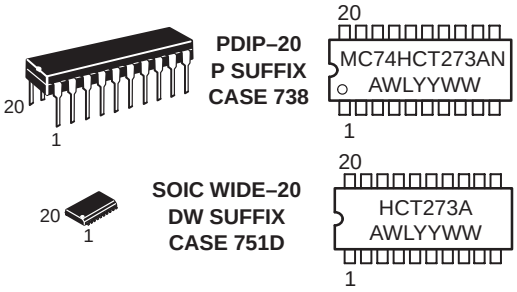
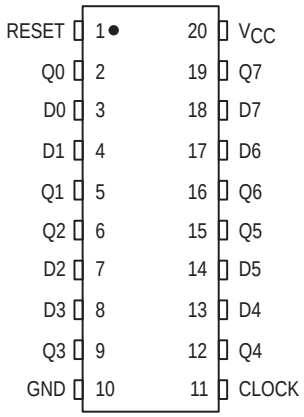
MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HCT273AN	PDIP–20	1440 / Box
MC74HCT273ADW	SOIC–WIDE	38 / Rail
MC74HCT273ADWR2	SOIC–WIDE	1000 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air Plastic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (SOIC or Plastic DIP)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 4.0 mA	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 4.0 mA	4.5	0.26	0.33	0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	5.5	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	5.5	4.0	40	160	μA

ΔI_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4 V, Any One Input V_{in} = V_{CC} or GND, Other Inputs I_{out} = 0 μA	5.5	≥ –55°C 2.9	25°C to 125°C 2.4		mA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Fig.	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	1, 4	30	24	20	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q	1, 4	25	28	35	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q	2, 4	25	28	35	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output	1, 5	18	20	22	ns

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Gate)*	30	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (V_{CC} = 5.0 V ± 10%, C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Fig.	Guaranteed Limit						Unit
			– 55 to 25°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
t_{su}	Minimum Setup Time, Data to Clock	3	10		12		15		ns
t_h	Minimum Hold Time, Clock to Data	3	3.0		3.0		3.0		ns
t_{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock	2	5.0		5.0		5.0		ns
t_w	Minimum Pulse Width, Clock	1	12		15		18		ns
t_w	Minimum Pulse Width, Set or Reset	2	12		15		18		ns
t_r, t_f	Maximum Input Rise and Fall Times	1		500		500		500	ns

SWITCHING WAVEFORMS

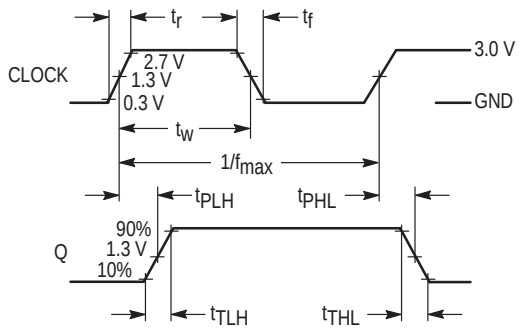


Figure 1.

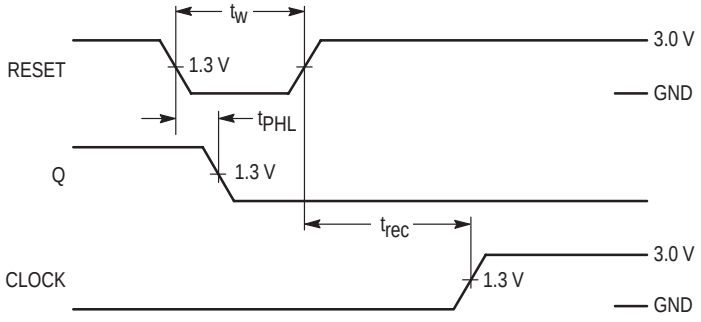


Figure 2.

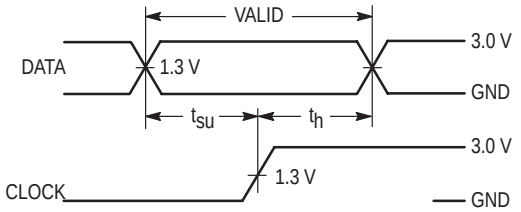
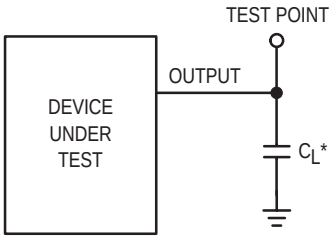


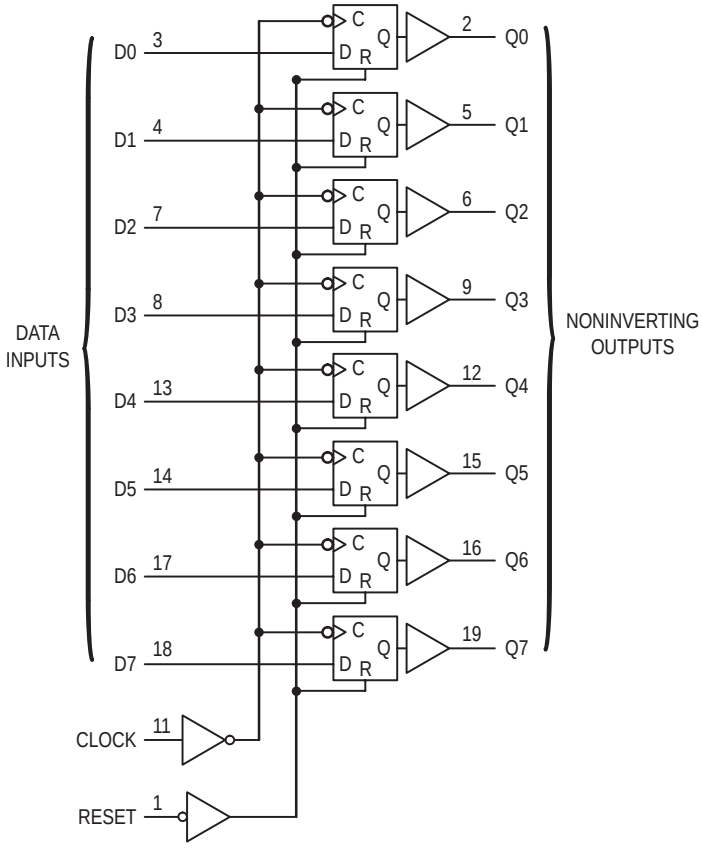
Figure 3.



*Includes all probe and jig capacitance

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM



MC74HC373A

Octal 3-State Non-Inverting Transparent Latch

High–Performance Silicon–Gate CMOS

The MC74HC373A is identical in pinout to the LS373. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high–impedance state. Thus, data may be latched even when the outputs are not enabled.

The HC373A is identical in function to the HC573A which has the data inputs on the opposite side of the package from the outputs to facilitate PC board layout.

The HC373A is the non–inverting version of the HC533A.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 186 FETs or 46.5 Equivalent Gates

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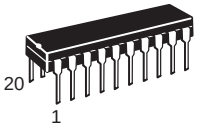
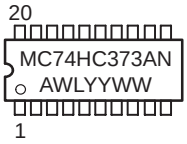
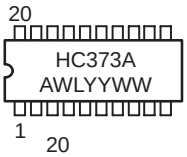
MARKING DIAGRAMS

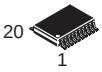


PDIP–20
P SUFFIX
CASE 738

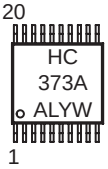


SOIC WIDE–20
DW SUFFIX
CASE 751D





TSSOP–20
DT SUFFIX
CASE 948G

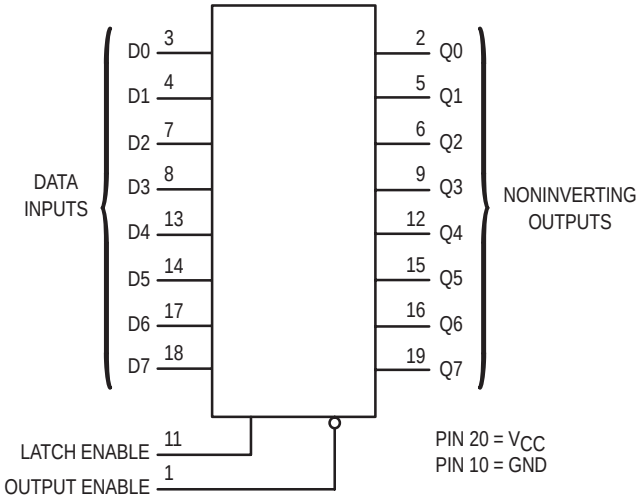


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

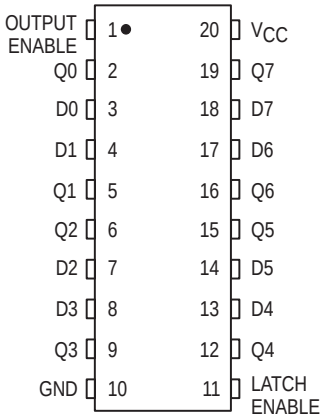
ORDERING INFORMATION

Device	Package	Shipping
MC74HC373AN	PDIP–20	1440 / Box
MC74HC373ADW	SOIC–WIDE	38 / Rail
MC74HC373ADWR2	SOIC–WIDE	1000 / Reel
MC74HC373ADT	TSSOP–20	75 / Rail
MC74HC373ADTR2	TSSOP–20	2500 / Reel

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
Output Enable	**Latch Enable**	**D**	**Q**
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

X = Don't Care
Z = High Impedance

Design Criteria	Value	Units
Internal Gate Count*	46.5	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	0.0075	pJ

*Equivalent to a two–input NAND gate.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC, SSOP or TSSOP Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0 μA	6.0	4.0	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH} t_{PHL}	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	2.0 3.0 4.5 6.0	125 80 25 21	155 110 31 26	190 130 38 32	ns
t_{PLH} t_{PHL}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	2.0 3.0 4.5 6.0	140 90 28 24	175 120 35 30	210 140 42 36	ns
t_{PLZ} t_{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 3.0 4.5 6.0	150 100 30 26	190 125 38 33	225 150 45 38	ns
t_{PZL} t_{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 3.0 4.5 6.0	150 100 30 26	190 125 38 33	225 150 45 38	ns
t_{TLH} t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0 3.0 4.5 6.0	60 23 12 10	75 27 15 13	90 32 18 15	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)		15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	36	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Fig.	V_{CC} Volts	Guaranteed Limit						Unit
				– 55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
t_{su}	Minimum Setup Time, Input D to Latch Enable	4	2.0 3.0 4.5 6.0	25 20 5.0 5.0		30 25 6.0 6.0		40 30 8.0 7.0		ns
t_h	Minimum Hold Time, Latch Enable to Input D	4	2.0 3.0 4.5 6.0	5.0 5.0 5.0 5.0		5.0 5.0 5 0 5.0		5.0 5.0 5.0 5.0		ns
t_w	Minimum Pulse Width, Latch Enable	2	2.0 3.0 4.5 6.0	60 23 12 10		75 27 15 13		90 32 18 15		ns
t_r, t_f	Maximum Input Rise and Fall Times	1	2.0 3.0 4.5 6.0		1000 800 500 400		1000 800 500 400		1000 800 500 400	ns

SWITCHING WAVEFORMS

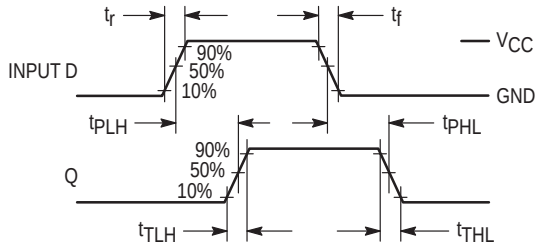


Figure 1.

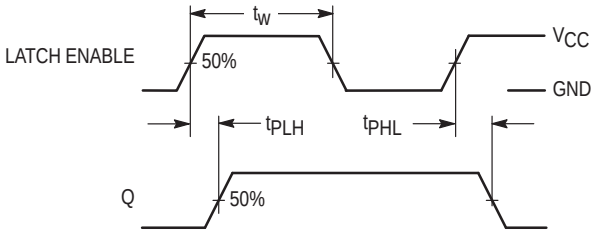


Figure 2.

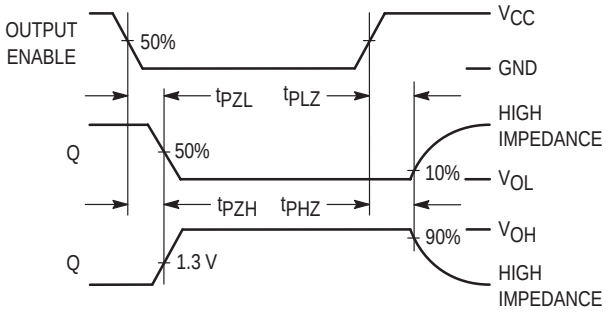


Figure 3.

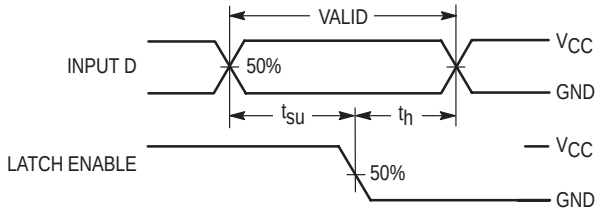
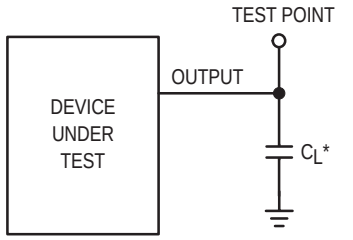


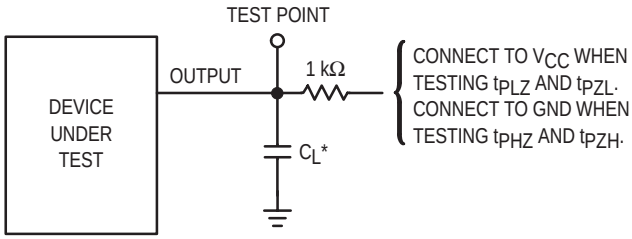
Figure 4.

TEST CIRCUITS



*Includes all probe and jig capacitance

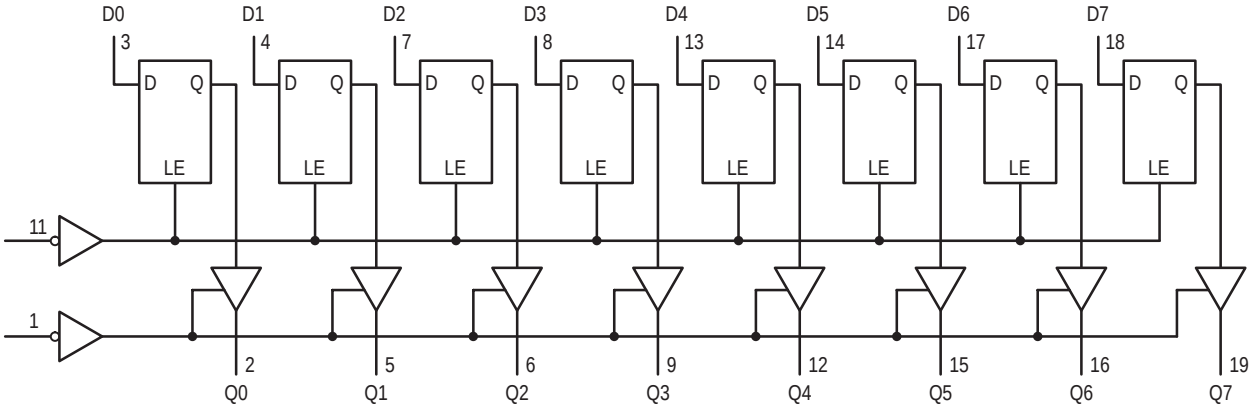
Figure 5.



*Includes all probe and jig capacitance

Figure 6.

EXPANDED LOGIC DIAGRAM



MC74HCT373A

Octal 3-State Noninverting Transparent Latch with LSTTL-Compatible Inputs

High–Performance Silicon–Gate CMOS

The MC74HCT373A may be used as a level converter for interfacing TTL or NMOS outputs to High–Speed CMOS inputs.

The HCT373A is identical in pinout to the LS373.

The eight latches of the HCT373A are transparent D–type latches. While the Latch Enable is high the Q outputs follow the Data Inputs. When Latch Enable is taken low, data meeting the setup and hold times becomes latched.

The Output Enable does not affect the state of the latch, but when Output Enable is high, all outputs are forced to the high–impedance state. Thus, data may be latched even when the outputs are not enabled.

The HCT373A is identical in function to the HCT573A, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HCT533A, which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS–Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 196 FETs or 49 Equivalent Gates

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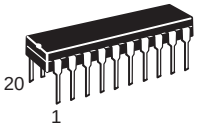
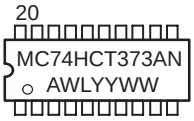
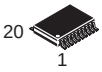
MARKING DIAGRAMS



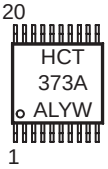
PDIP–20
P SUFFIX
CASE 738



SOIC WIDE–20
DW SUFFIX
CASE 751D

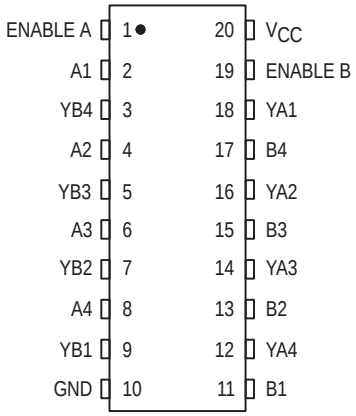


TSSOP–20
DT SUFFIX
CASE 948G



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

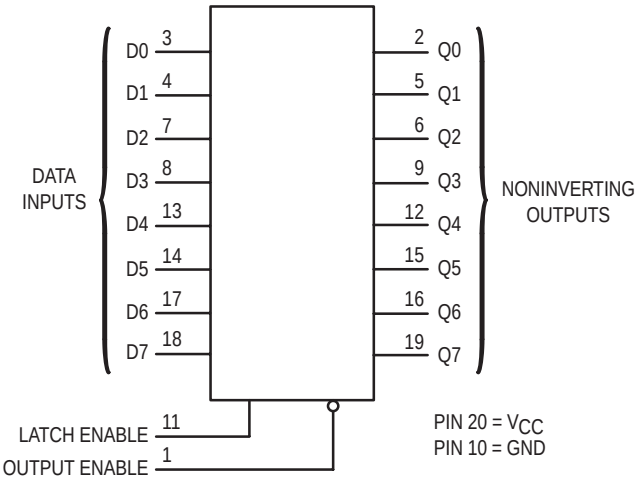
PIN ASSIGNMENT



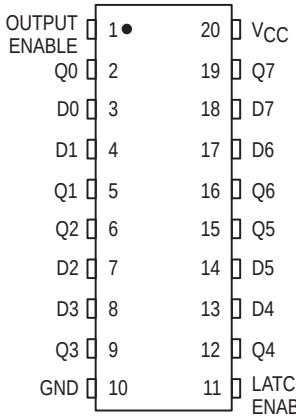
ORDERING INFORMATION

Device	Package	Shipping
MC74HCT373AN	PDIP–20	1440 / Box
MC74HCT373ADW	SOIC–WIDE	38 / Rail
MC74HCT373ADWR2	SOIC–WIDE	1000 / Reel
MC74HCT373ADT	TSSOP–20	75 / Rail
MC74HCT373ADTR2	TSSOP–20	2500 / Reel

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
Output Enable	**Latch Enable**	**D**	**Q**
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

X = don't care
Z = high impedance

Design Criteria	Value	Units
Internal Gate Count*	49	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	.0075	pJ

*Equivalent to a two–input NAND gate.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC, SSOP or TSSOP Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6.0 mA	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6.0 mA	4.5	0.26	0.33	0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	5.5	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	5.5	4.0	40	160	μA

ΔI_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4 V, Any One Input V_{in} = V_{CC} or GND, Other Inputs I_{out} = 0 μA	5.5	≥ **–55°C**	**25°C to 125°C**	mA
				2.9	2.4	

NOTE: 1. Total Supply Current = $I_{CC} + \Sigma\Delta I_{CC}$.
NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

		Guaranteed Limit			
Symbol	**Parameter**	**– 55 to 25°C**	**≤ 85°C**	**≤ 125°C**	**Unit**
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	28	35	42	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	32	40	48	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	30	38	45	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	35	44	53	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	12	15	18	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

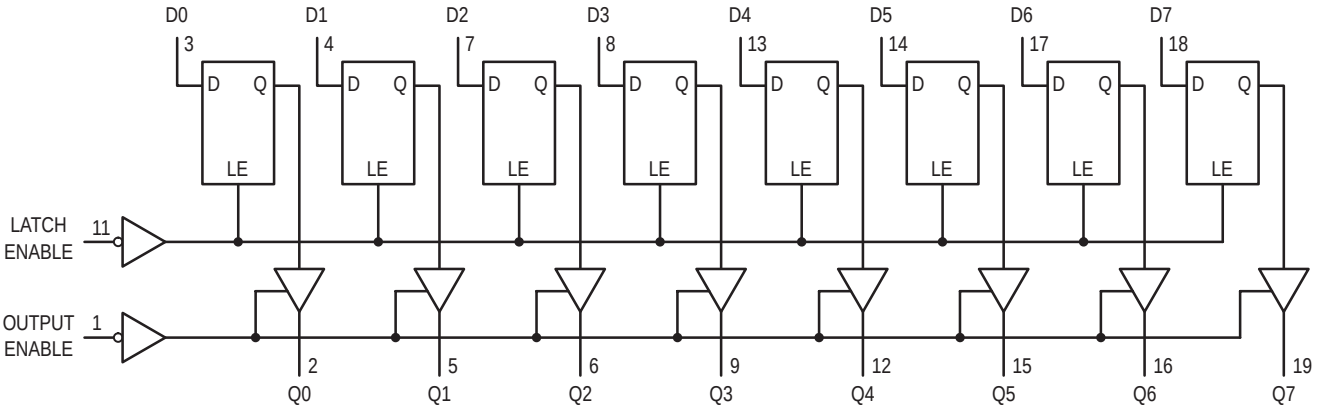
		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Latch)*	65	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (V_{CC} = 5.0 V ± 10%, Input $t_r = t_f$ = 6.0 ns)

		Guaranteed Limit			
Symbol	**Parameter**	**– 55 to 25°C**	**≤ 85°C**	**≤ 125°C**	**Unit**
t_{su}	Minimum Setup Time, Input D to Latch Enable (Figure 4)	10	13	15	ns
t_h	Minimum Hold Time, Latch Enable to Input D (Figure 4)	10	13	15	ns
t_w	Minimum Pulse Width, Latch Enable (Figure 2)	12	15	18	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	500	500	500	ns

EXPANDED LOGIC DIAGRAM



SWITCHING WAVEFORMS

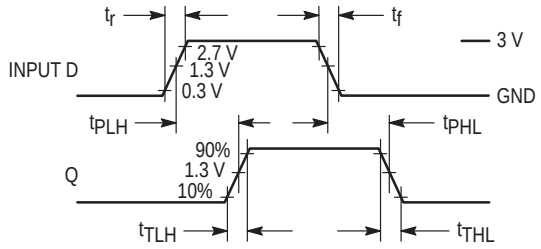


Figure 1.

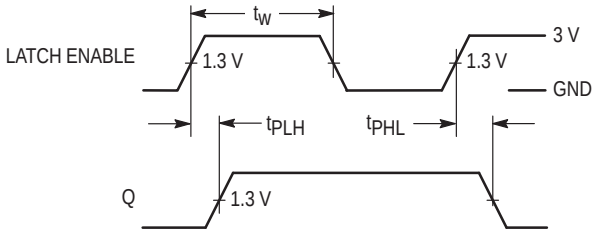


Figure 2.

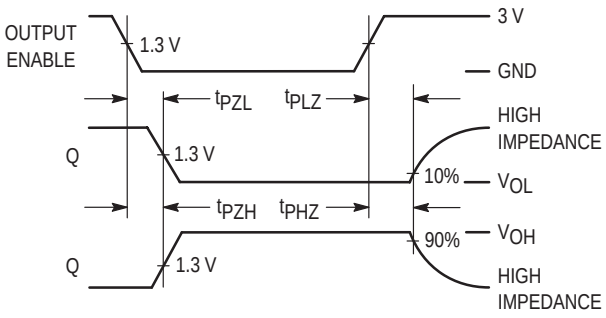


Figure 3.

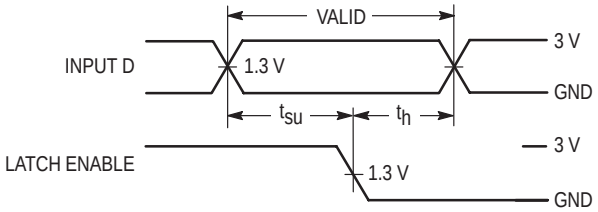
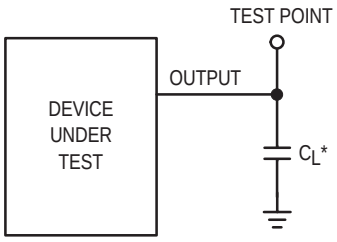


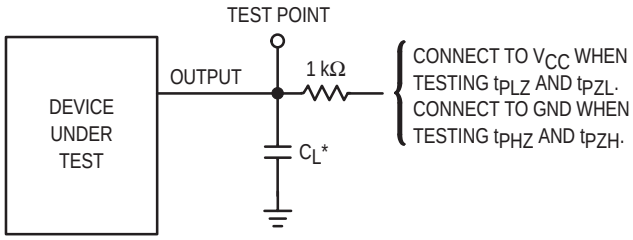
Figure 4.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 5.



*Includes all probe and jig capacitance

Figure 6.

MC74HC374A

Octal 3-State Non-Inverting D Flip-Flop

High–Performance Silicon–Gate CMOS

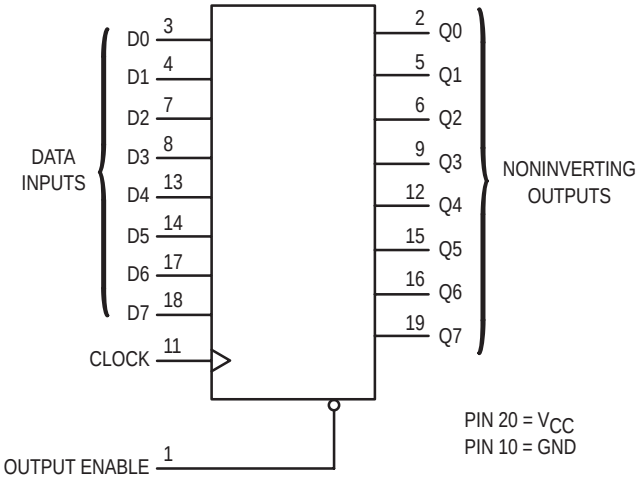
The MC74HC374A is identical in pinout to the LS374. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Data meeting the setup time is clocked to the outputs with the rising edge of the clock. The Output Enable input does not affect the states of the flip–flops, but when Output Enable is high, the outputs are forced to the high–impedance state; thus, data may be stored even when the outputs are not enabled.

The HC374A is identical in function to the HC574A which has the input pins on the opposite side of the package from the output. This device is similar in function to the HC534A which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 266 FETs or 66.5 Equivalent Gates

LOGIC DIAGRAM



FUNCTION TABLE

Inputs			Output
Output Enable	Clock	D	Q
L	↑	H	H
L	↑	L	L
L	L,H,↓	X	No Change
H	X	X	Z

X = don't care
Z = high impedance

ON Semiconductor

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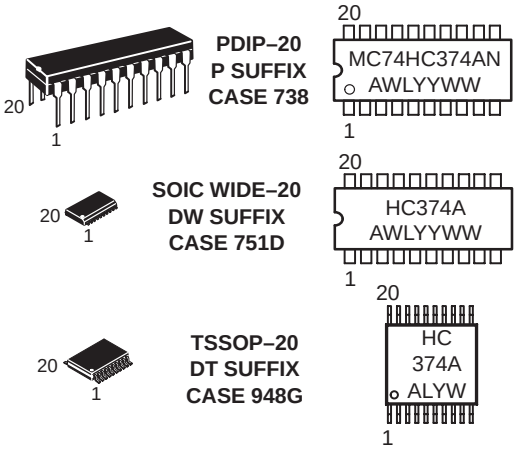
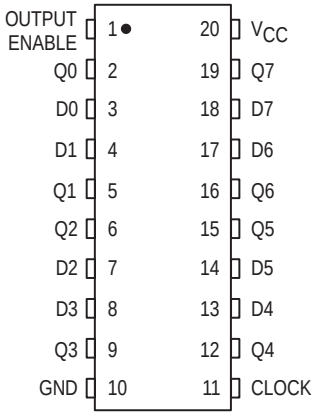
MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HC374AN	PDIP–20	1440 / Box
MC74HC374ADW	SOIC–WIDE	38 / Rail
MC74HC374ADWR2	SOIC–WIDE	1000 / Reel
MC74HC374ADT	TSSOP–20	75 / Rail
MC74HC374ADTR2	TSSOP–20	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC, SSOP or TSSOP Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1) V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit – 55 to 25°C	Guaranteed Limit ≤ 85°C	Guaranteed Limit ≤ 125°C	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.90 4.40 5.90	1.90 4.40 5.90	1.90 4.40 5.90	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	2.48 2.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	V

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	0.10 0.10 0.10	0.10 0.10 0.10	0.10 0.10 0.10	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 2.4$ mA $\|I_{out}\| \leq 6.0$ mA $\|I_{out}\| \leq 7.8$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	V
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	2.0 3.0 4.5 6.0	6 15 30 35	5 10 24 28	4 8 20 24	MHz
t_{PLH} t_{PHL}	Maximum Propagation Delay, Input Clock to Q (Figures 1 and 5)	2.0 3.0 4.5 6.0	125 80 25 21	155 110 31 26	190 130 38 32	ns
t_{PLZ} t_{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 3.0 4.5 6.0	150 100 30 26	190 125 38 33	225 150 45 38	ns
t_{PLZ} t_{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 3.0 4.5 6.0	150 100 30 26	190 125 38 33	225 150 45 38	ns
t_{TLH} t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)		15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	34	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Fig.	V_{CC} Volts	Guaranteed Limit						Unit
				– 55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
t_{su}	Minimum Setup Time, Data to Clock	3	2.0 3.0 4.5 6.0	50 40 10 9		65 50 13 11		75 60 15 13		ns
t_h	Minimum Hold Time, Clock to Data	3	2.0 3.0 4.5 6.0	5.0 5.0 5.0 5.0		5.0 5 0 5.0 5.0		5.0 5.0 5.0 5.0		ns
t_w	Minimum Pulse Width, Clock	1	2.0 3.0 4.5 6.0	60 23 12 10		75 27 15 13		90 32 18 15		ns
t_r, t_f	Maximum Input Rise and Fall Times	1	2.0 3.0 4.5 6.0		1000 800 500 400		1000 800 500 400		1000 800 500 400	ns

SWITCHING WAVEFORMS

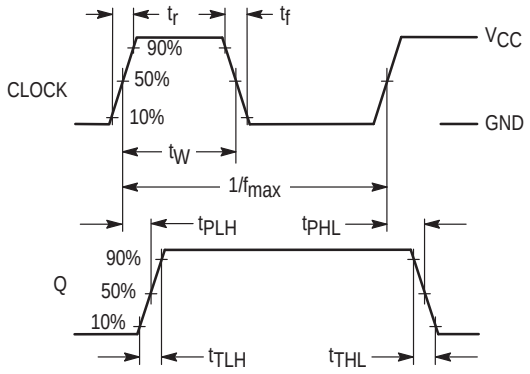


Figure 1.

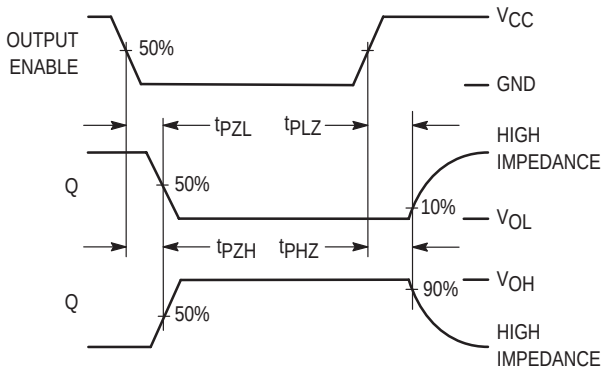


Figure 2.

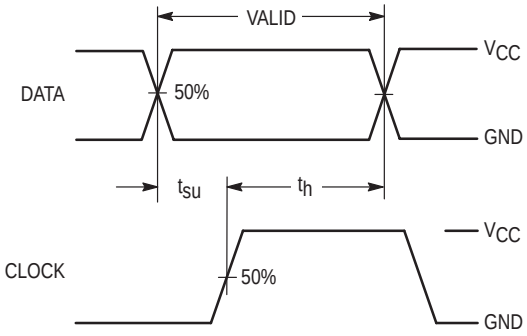
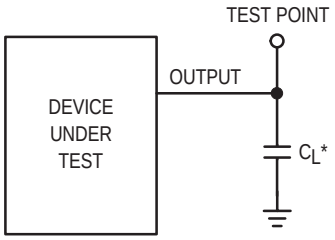


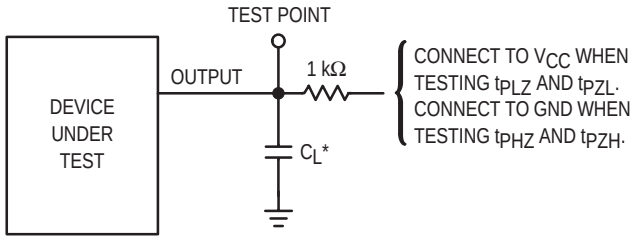
Figure 3.

TEST CIRCUITS



*Includes all probe and jig capacitance

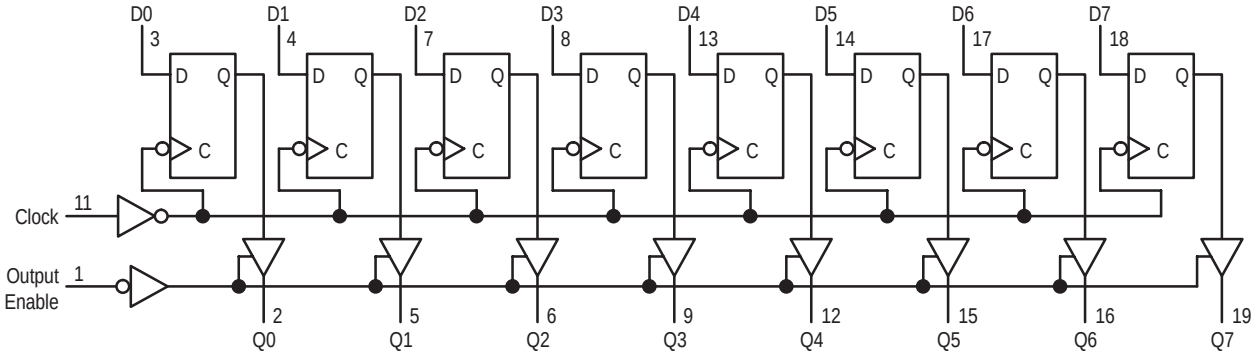
Figure 4.



*Includes all probe and jig capacitance

Figure 5.

EXPANDED LOGIC DIAGRAM



MC74HCT374A

Octal 3-State Noninverting D Flip-Flop with LSTTL-Compatible Inputs

High–Performance Silicon–Gate CMOS

The MC74HCT374A may be used as a level converter for interfacing TTL or NMOS outputs to High–Speed CMOS inputs.

The HCT374A is identical in pinout to the LS374.

Data meeting the setup and hold time is clocked to the outputs with the rising edge of Clock. The Output Enable does not affect the state of the flip–flops, but when Output Enable is high, the outputs are forced to the high–impedance state. Thus, data may be stored even when the outputs are not enabled.

The HCT374A is identical in function to the HCT574A, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HCT534A, which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS–Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 276 FETs or 69 Equivalent Gates
- Improvements over HCT374
  - — Improved Propagation Delays
  - — 50% Lower Quiescent Power
  - — Improved Input Noise and Latchup Immunity

ON Semiconductor

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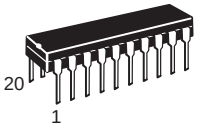
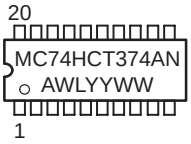
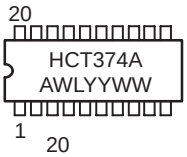
MARKING DIAGRAMS

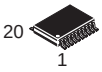


PDIP–20
P SUFFIX
CASE 738



SOIC WIDE–20
DW SUFFIX
CASE 751D





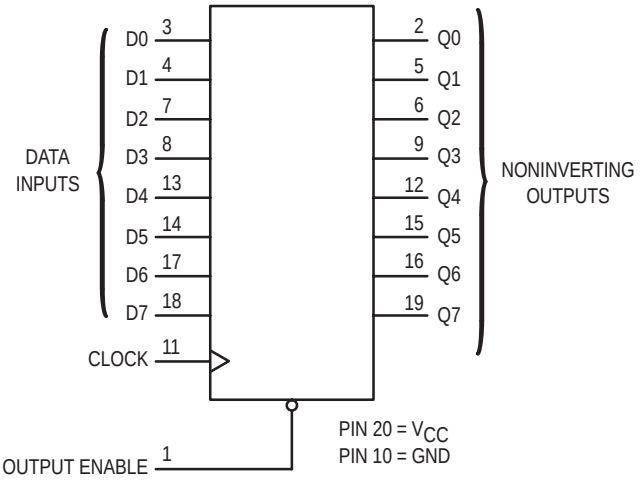
TSSOP–20
DT SUFFIX
CASE 948G

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

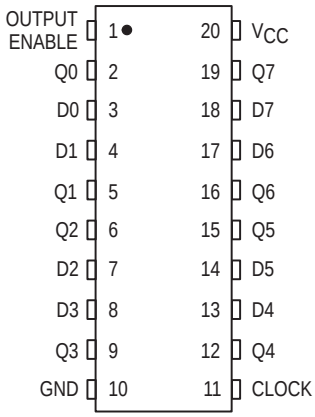
ORDERING INFORMATION

Device	Package	Shipping
MC74HCT374AN	PDIP–20	1440 / Box
MC74HCT374ADW	SOIC–WIDE	38 / Rail
MC74HCT374ADWR2	SOIC–WIDE	1000 / Reel
MC74HCT374ADT	TSSOP–20	75 / Rail
MC74HCT374ADTR2	TSSOP–20	2500 / Reel

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
Output Enable	**Clock**	**D**	**Q**
L	↑	H	H
L	↑	L	L
L	L,H,↓	X	No Change
H	X	X	Z

X = don't care
Z = high impedance

Design Criteria	Value	Units
Internal Gate Count*	69	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	.0075	pJ

*Equivalent to a two–input NAND gate.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC, SSOP or TSSOP Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6.0 mA	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6.0 mA	4.5	0.26	0.33	0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	5.5	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	5.5	4.0	40	160	μA

ΔI_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4 V, Any One Input V_{in} = V_{CC} or GND, Other Inputs I_{out} = 0 μA	5.5	≥ –55°C 2.9	25°C to 125°C 2.4	mA

NOTE: 1. Total Supply Current = $I_{CC} + \Sigma\Delta I_{CC}$.
NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	30	24	20	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	31	39	47	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	30	38	45	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	30	38	45	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	12	15	18	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Flip–Flop)*	65	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (V_{CC} = 5.0 V ± 10%, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Data to Clock (Figure 3)	12	15	18	ns
t_h	Minimum Hold Time, Clock to Data (Figure 3)	5.0	5.0	5.0	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	12	15	18	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	500	500	500	ns

SWITCHING WAVEFORMS

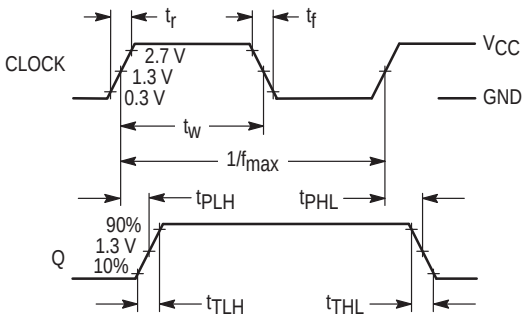


Figure 1.

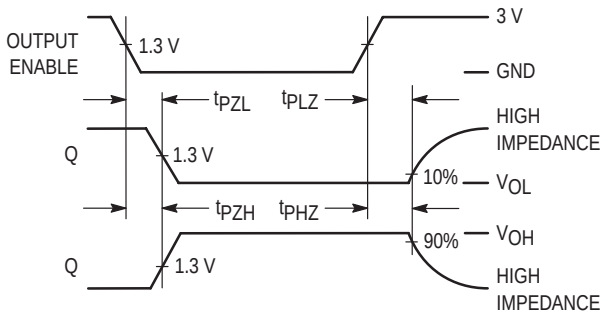


Figure 2.

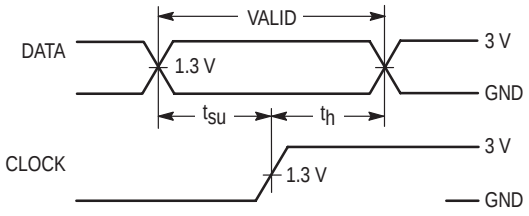
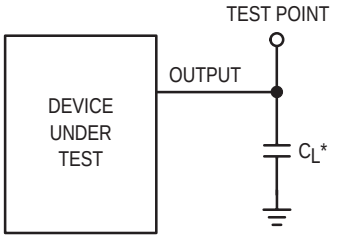


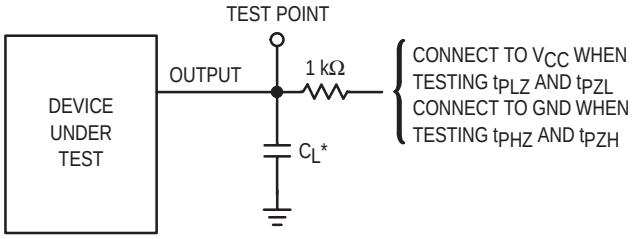
Figure 3.

TEST CIRCUITS



*Includes all probe and jig capacitance

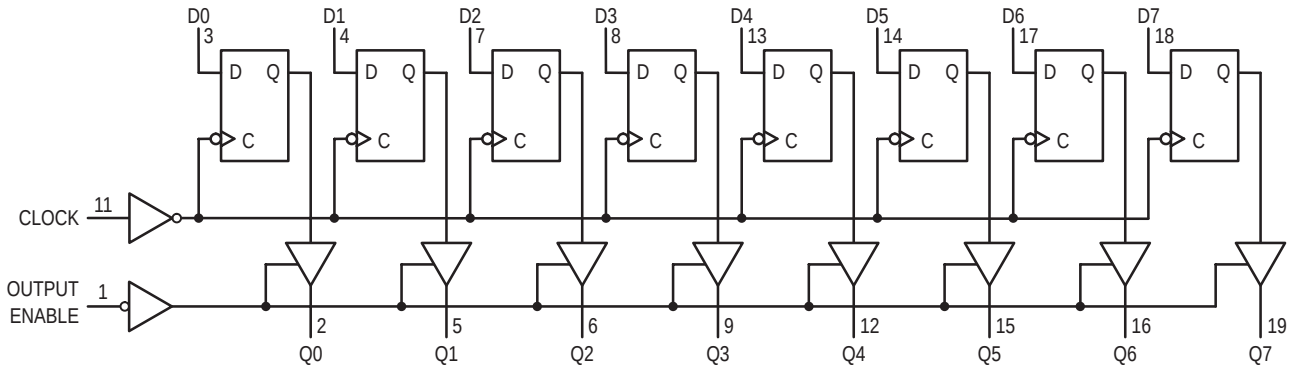
Figure 4.



*Includes all probe and jig capacitance

Figure 5.

EXPANDED LOGIC DIAGRAM



MC74HC390A

Dual 4-Stage Binary Ripple Counter with ÷ 2 and ÷ 5 Sections

High–Performance Silicon–Gate CMOS

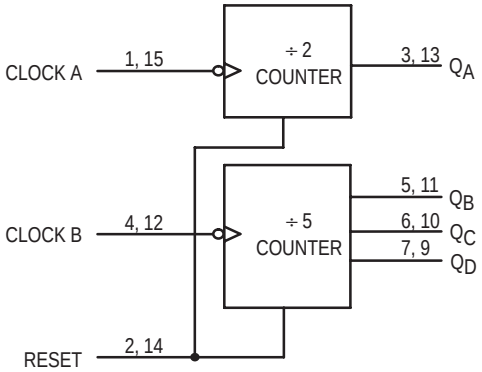
The MC74HC390A is identical in pinout to the LS390. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 4–bit counters, each composed of a divide–by–two and a divide–by–five section. The divide–by–two and divide–by–five counters have separate clock inputs, and can be cascaded to implement various combinations of ÷ 2 and/or ÷ 5 up to a ÷ 100 counter.

Flip–flops internal to the counters are triggered by high–to–low transitions of the clock input. A separate, asynchronous reset is provided for each 4–bit counter. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or strobes except when gated with the Clock of the HC390A.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No 7A
- Chip Complexity: 244 FETs or 61 Equivalent Gates

LOGIC DIAGRAM



PIN 16 = V_{CC}
PIN 8 = GND

FUNCTION TABLE

Clock A	Clock B	Reset	Action
X	X	H	Reset ÷ 2 and ÷ 5
↘	X	L	Increment ÷ 2
X	↘	L	Increment ÷ 5

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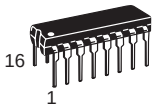
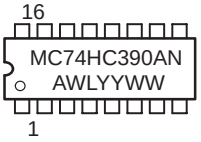
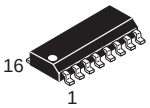
MARKING DIAGRAMS

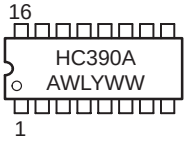


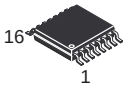
PDIP–16
N SUFFIX
CASE 648



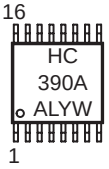


SO–16
D SUFFIX
CASE 751B



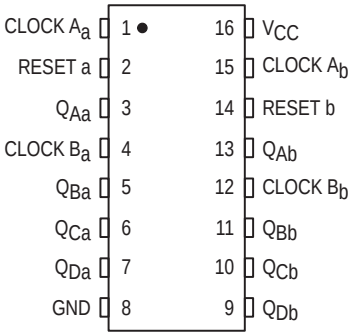


TSSOP–16
DT SUFFIX
CASE 948F



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HC390AN	PDIP–16	2000 / Box
MC74HC390AD	SOIC–16	48 / Rail
MC74HC390ADR2	SOIC–16	2500 / Reel
MC74HC390ADT	TSSOP–16	96 / Rail
MC74HC390ADTR2	TSSOP–16	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1) V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 4.0 mA $\|I_{out}\|$ ≤ 5.2 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 4.0 mA $\|I_{out}\|$ ≤ 5.2 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0 μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_f = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	2.0 3.0 4.5 6.0	10 15 30 50	9 14 28 45	8 12 25 40	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock A to QA (Figures 1 and 3)	2.0 3.0 4.5 6.0	70 40 24 20	80 45 30 26	90 50 36 31	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock A to QC (QA connected to Clock B) (Figures 1 and 3)	2.0 3.0 4.5 6.0	200 160 58 49	250 185 65 62	300 210 70 68	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock B to QB (Figures 1 and 3)	2.0 3.0 4.5 6.0	70 40 26 22	80 45 33 28	90 50 39 33	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock B to QC (Figures 1 and 3)	2.0 3.0 4.5 6.0	90 56 37 31	105 70 46 39	180 100 56 48	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock B to QD (Figures 1 and 3)	2.0 3.0 4.5 6.0	70 40 26 22	80 45 33 28	90 50 39 33	ns
t_{PHL}	Maximum Propagation Delay, Reset to any Q (Figures 2 and 3)	2.0 3.0 4.5 6.0	80 48 30 26	95 65 38 33	110 75 44 39	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 15	110 36 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

1. For propagation delays with loads other than 50 pF, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Counter)*	35	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock A or Clock B (Figure 2)	2.0 3.0 4.5 6.0	25 15 10 9	30 20 13 11	40 30 15 13	ns
t_w	Minimum Pulse Width, Clock A, Clock B (Figure 1)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 15	110 36 22 19	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 3.0 4.5 6.0	75 27 20 18	95 32 24 22	110 36 30 28	ns
t_f, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

PIN DESCRIPTIONS

INPUTS

Clock A (Pins 1, 15) and Clock B (Pins 4, 15)

Clock A is the clock input to the ÷ 2 counter; Clock B is the clock input to the ÷ 5 counter. The internal flip–flops are toggled by high–to–low transitions of the clock input.

CONTROL INPUTS

Reset (Pins 2, 14)

Asynchronous reset. A high at the Reset input prevents counting, resets the internal flip–flops, and forces Q_A through Q_D low.

OUTPUTS

Q_A (Pins 3, 13)

Output of the ÷ 2 counter.

Q_B, Q_C, Q_D (Pins 5, 6, 7, 9, 10, 11)

Outputs of the ÷ 5 counter. Q_D is the most significant bit. Q_A is the least significant bit when the counter is connected for BCD output as in Figure 4. Q_B is the least significant bit when the counter is operating in the bi–quinary mode as in Figure 5.

SWITCHING WAVEFORMS

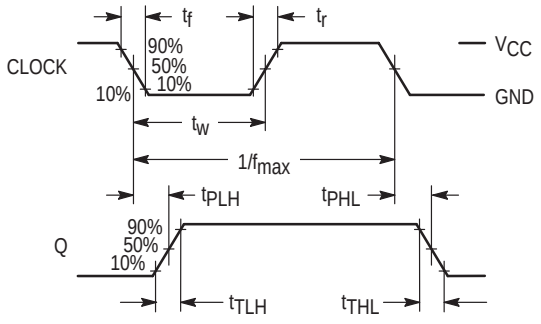


Figure 1.

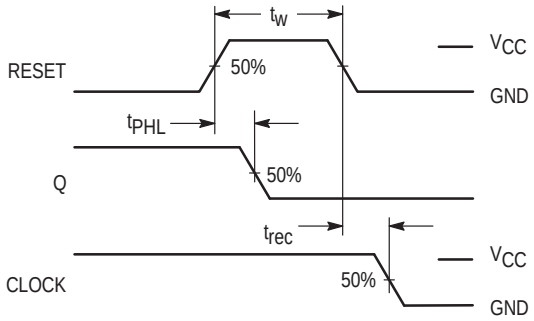
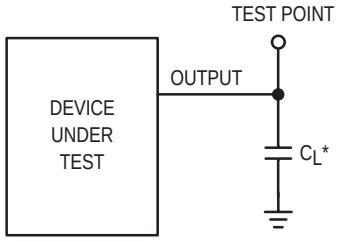


Figure 2.

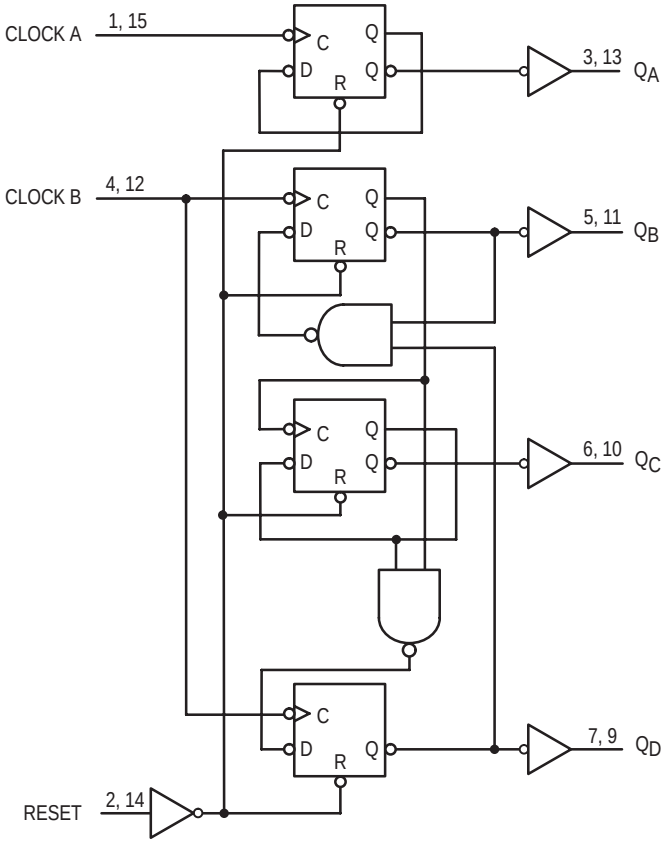
TEST CIRCUIT



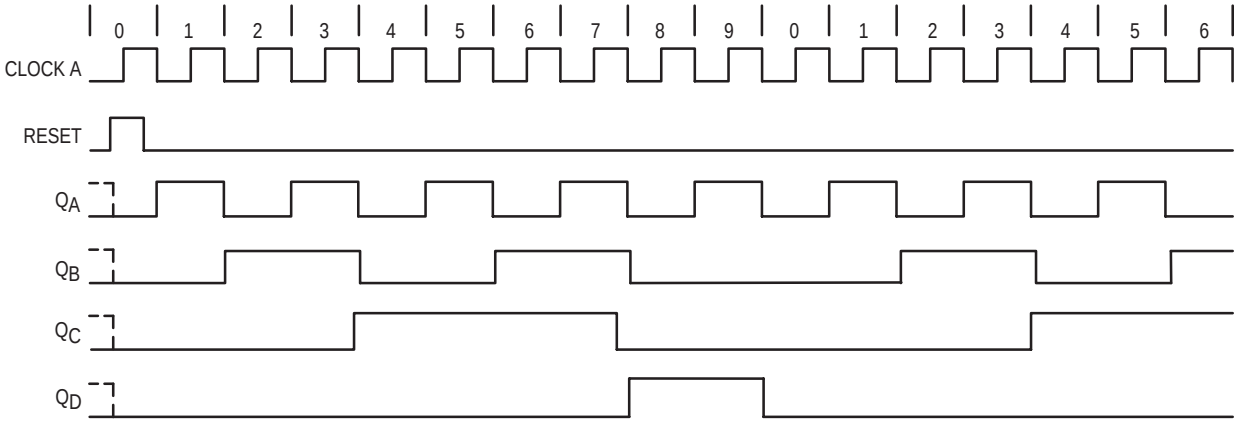
*Includes all probe and jig capacitance

Figure 3.

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM
(Q_A Connected to Clock B)



APPLICATIONS INFORMATION

Each half of the MC54/74HC390A has independent ÷ 2 and ÷ 5 sections (except for the Reset function). The ÷ 2 and ÷ 5 counters can be connected to give BCD or bi–quinary (2–5) count sequences. If Output Q_A is connected to the Clock B input (Figure 4), a decade divider with BCD output is obtained. The function table for the BCD count sequence is given in Table 1.

To obtain a bi–quinary count sequence, the input signals connected to the Clock B input, and output Q_D is connected to the Clock A input (Figure 5). Q_A provides a 50% duty cycle output. The bi–quinary count sequence function table is given in Table 2.

Table 1. BCD Count Sequence*

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

*Q_A connected to Clock B input.

Table 2. Bi–Quinary Count Sequence**

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L

**Q_D connected to Clock A input.

CONNECTION DIAGRAMS

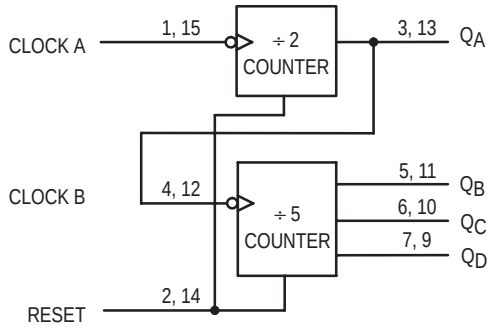


Figure 4. BCD Count

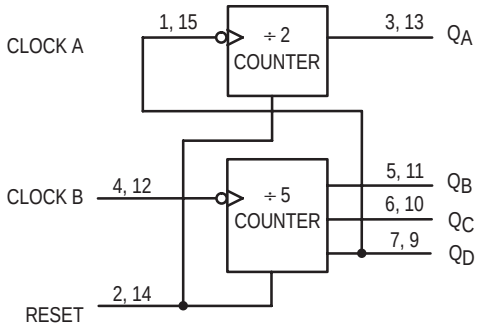


Figure 5. Bi-Quinary Count

MC74HC393A

Dual 4-Stage Binary Ripple Counter

High–Performance Silicon–Gate CMOS

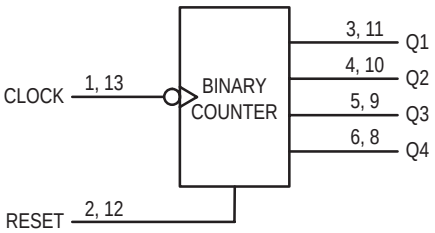
The MC74HC393A is identical in pinout to the LS393. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 4–bit binary ripple counters with parallel outputs from each counter stage. A ÷ 256 counter can be obtained by cascading the two binary counters.

Internal flip–flops are triggered by high–to–low transitions of the clock input. Reset for the counters is asynchronous and active–high. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the Clock of the HC393A.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 236 FETs or 59 Equivalent Gates

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

FUNCTION TABLE

Inputs		
Clock	**Reset**	**Outputs**
X	H	L
H	L	No Change
L	L	No Change
↗	L	No Change
↘	L	Advance to Next State

ON Semiconductor

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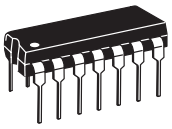
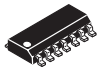
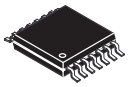
MARKING DIAGRAMS



PDIP–14
N SUFFIX
CASE 646



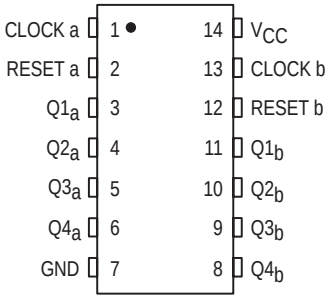
SOIC–14
D SUFFIX
CASE 751A



TSSOP–14
DT SUFFIX
CASE 948G

A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HC393AN	PDIP–14	2000 / Box
MC74HC393AD	SOIC–14	55 / Rail
MC74HC393ADR2	SOIC–14	2500 / Reel
MC74HC393ADT	TSSOP–14	96 / Rail
MC74HC393ADTR2	TSSOP–14	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0 V	0	1000	ns
		V_{CC} = 3.0 V	0	600	
	(Figure 1)	V_{CC} = 4.5 V	0	500	
		V_{CC} = 6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit – 55 to 25°C	Guaranteed Limit ≤ 85°C	Guaranteed Limit ≤ 125°C	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.80	0.5 0.9 1.35 1.80	0.5 0.9 1.35 1.80	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 4.0 mA $\|I_{out}\|$ ≤ 5.2 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 2.4$ mA $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	2.0 3.0 4.5 6.0	10 15 30 50	9 14 28 45	8 12 25 40	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q1 (Figures 1 and 3)	2.0 3.0 4.5 6.0	70 40 24 20	80 45 30 26	90 50 36 31	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q2 (Figures 1 and 3)	2.0 3.0 4.5 6.0	100 56 34 20	105 70 45 38	180 100 55 48	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q3 (Figures 1 and 3)	2.0 3.0 4.5 6.0	130 80 44 37	150 105 55 47	180 130 70 58	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q4 (Figures 1 and 3)	2.0 3.0 4.5 6.0	160 110 52 44	250 185 65 55	300 210 82 65	ns
t_{PHL}	Maximum Propagation Delay, Reset to any Q (Figures 2 and 3)	2.0 3.0 4.5 6.0	80 48 30 26	95 65 38 33	110 75 50 43	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Counter)*	35	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 3.0 4.5 6.0	25 15 10 9	30 20 13 11	40 30 15 13	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 15	110 36 22 19	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 15	110 36 22 19	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

PIN DESCRIPTIONS

INPUTS
Clock (Pins 1, 13)

Clock input. The internal flip–flops are toggled and the counter state advances on high–to–low transitions of the clock input.

CONTROL INPUTS
Reset (Pins 2, 12)

Active–high, asynchronous reset. A separate reset is provided for each counter. A high at the Reset input prevents counting and forces all four outputs low.

OUTPUTS
Q1, Q2, Q3, Q4 (Pins 3, 4, 5, 6, 8, 9, 10, 11)

Parallel binary outputs Q4 is the most significant bit.

SWITCHING WAVEFORMS

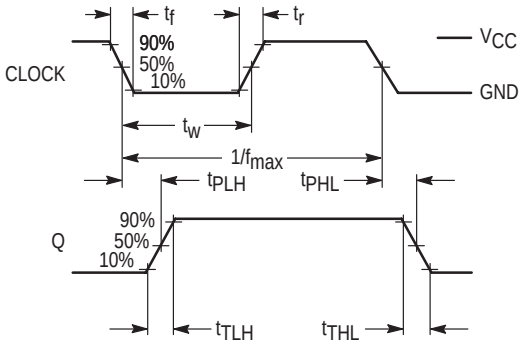


Figure 1.

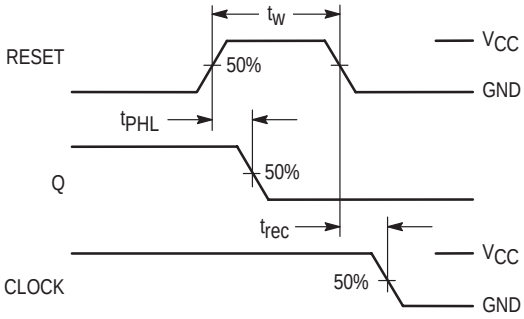
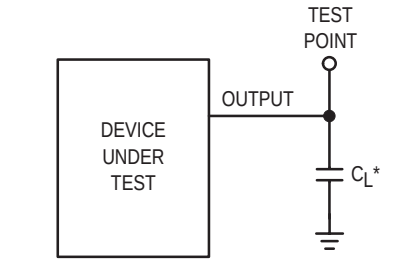


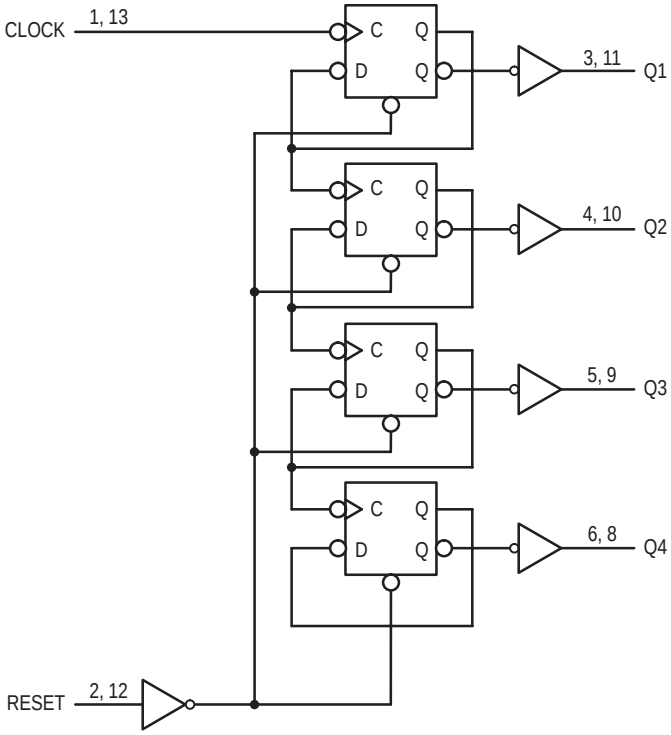
Figure 2.



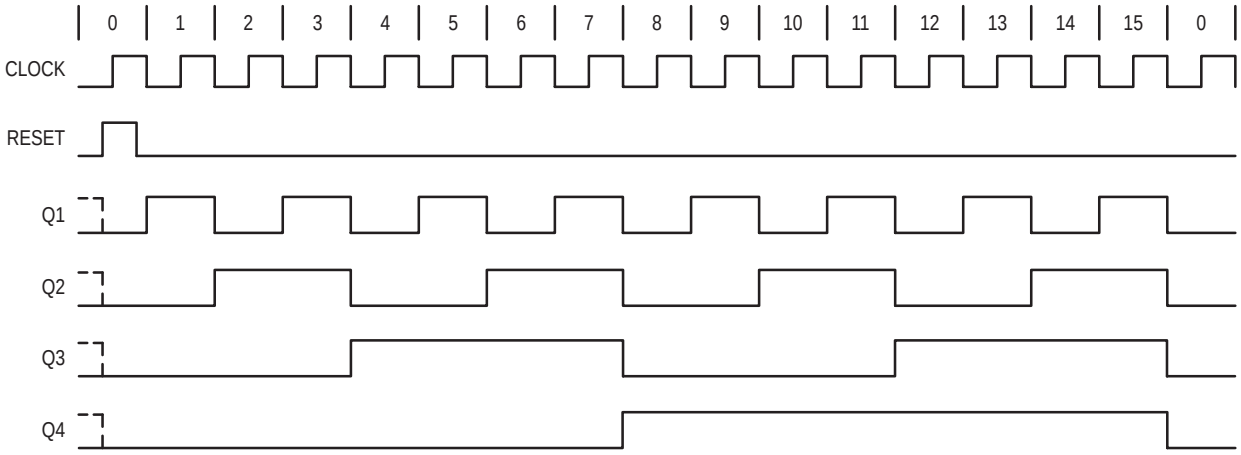
*Includes all probe and jig capacitance

Figure 3. Test Circuit

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM



COUNT SEQUENCE

Count	Outputs			
	Q4	Q3	Q2	Q1
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

MC74HC540A

Octal 3-State Inverting Buffer/Line Driver/Line Receiver

High–Performance Silicon–Gate CMOS

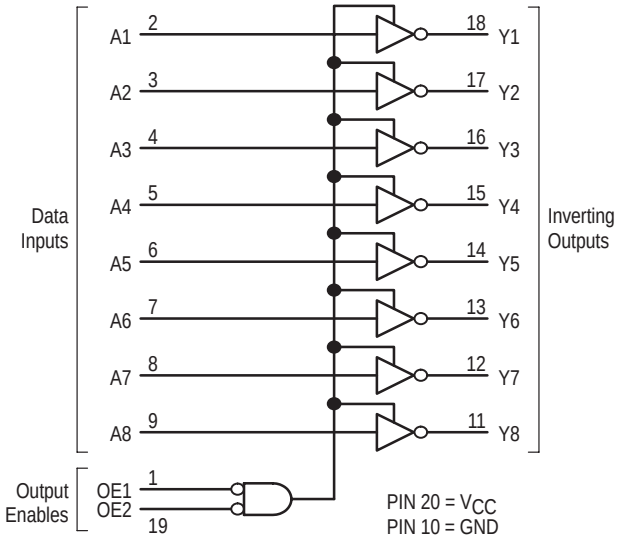
The MC74HC540A is identical in pinout to the LS540. The device inputs are compatible with Standard CMOS outputs. External pullup resistors make them compatible with LSTTL outputs.

The HC540A is an octal inverting buffer/line driver/line receiver designed to be used with 3–state memory address drivers, clock drivers, and other bus–oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active–low output enables.

The HC540A is similar in function to the HC541A, which has non–inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2 to 6V
- Low Input Current: 1μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 124 FETs or 31 Equivalent Gates

LOGIC DIAGRAM



FUNCTION TABLE

Inputs			Output Y
OE1	OE2	A	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

Z = High Impedance
X = Don't Care

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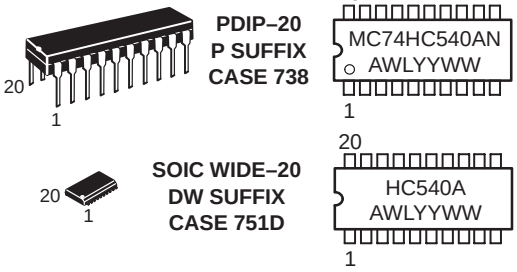
MARKING DIAGRAMS

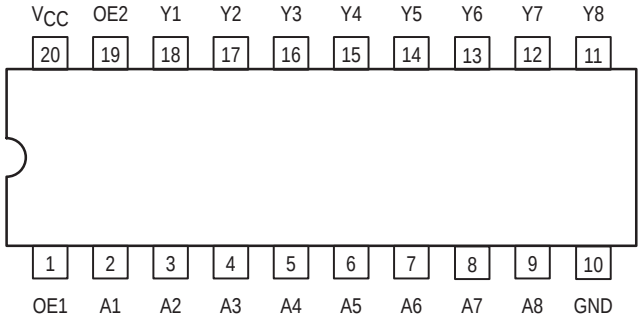


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74HC540AN	PDIP–20	1440 / Box
MC74HC540ADW	SOIC–WIDE	38 / Rail
MC74HC540ADWR2	SOIC–WIDE	1000 / Reel

Pinout: 20–Lead Packages (Top View)



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air Plastic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP or SOIC Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature Range, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise/Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit –55 to 25°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1V $\|I_{out}\|$ ≤ 20μA	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = V_{CC} – 0.1V $\|I_{out}\|$ ≤ 20μA	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IL} $\|I_{out}\|$ ≤ 20μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IL} $\|I_{out}\|$ ≤ 3.6mA $\|I_{out}\|$ ≤ 6.0mA $\|I_{out}\|$ ≤ 7.8mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} $\|I_{out}\|$ ≤ 20μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} $\|I_{out}\|$ ≤ 3.6mA $\|I_{out}\|$ ≤ 6.0mA $\|I_{out}\|$ ≤ 7.8mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
I_{OZ}	Maximum Three–State Leakage Current	Output in High Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0 3.0 4.5 6.0	80 30 18 15	100 40 23 20	120 55 28 25	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 3.0 4.5 6.0	110 45 25 21	140 60 31 26	165 75 38 31	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 3.0 4.5 6.0	110 45 25 21	140 60 31 26	165 75 38 31	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 3.0 4.5 6.0	60 22 12 10	75 28 15 13	90 34 18 15	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High Impedance State)		15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V, V_{EE} = 0 V	
C_{PD}	Power Dissipation Capacitance (Per Buffer)*	35	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

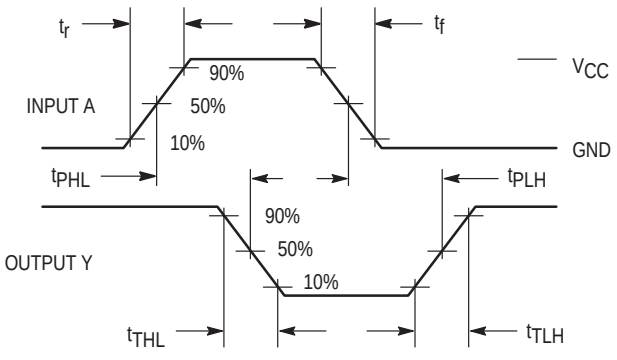


Figure 1.

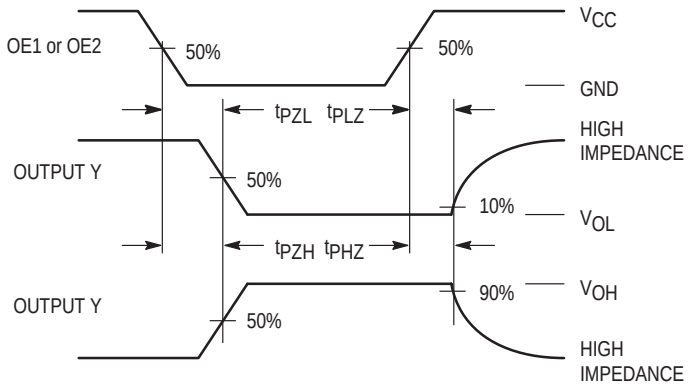
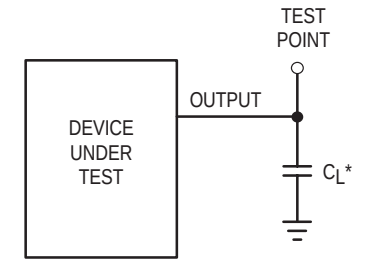


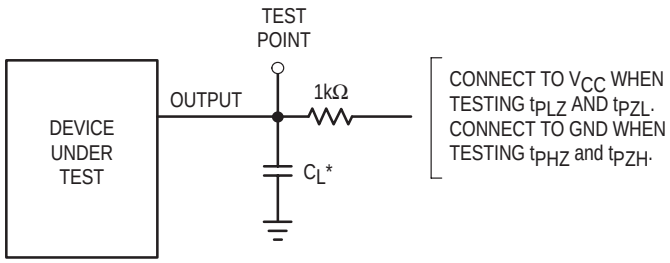
Figure 2.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 3.



*Includes all probe and jig capacitance

Figure 4.

PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, A5, A6, A7, A8 (PINS 2, 3, 4, 5, 6, 7, 8, 9) — Data input pins. Data on these pins appear in inverted form on the corresponding Y outputs, when the outputs are enabled.

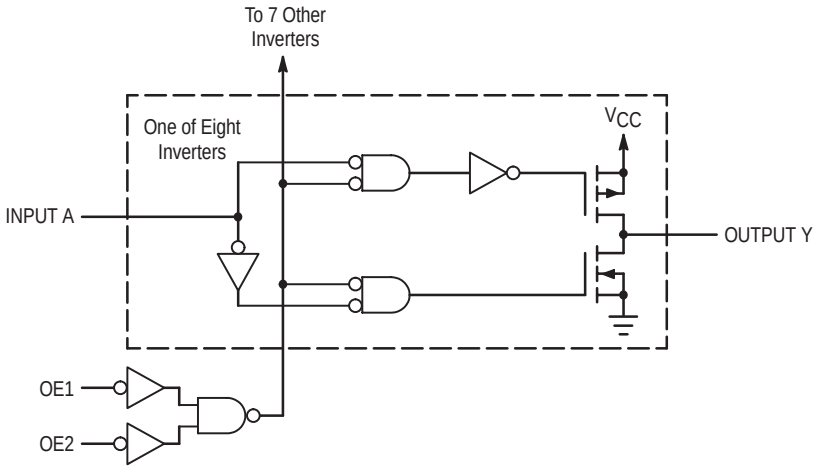
CONTROLS

OE1, OE2 (PINS 1, 19) — Output enables (active–low). When a low voltage is applied to both of these pins, the outputs are enabled and the device functions as an inverter. When a hgih voltage is applied to either input, the outputs assume the high impedance state.

OUTPUTS

Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11) — Device outputs. Depending upon the state of the output enable pins, these outputs are either inverting outputs or high–impedance outputs.

LOGIC DETAIL



MC74HC541A

Octal 3-State Non-Inverting Buffer/Line Driver/ Line Receiver

High–Performance Silicon–Gate CMOS

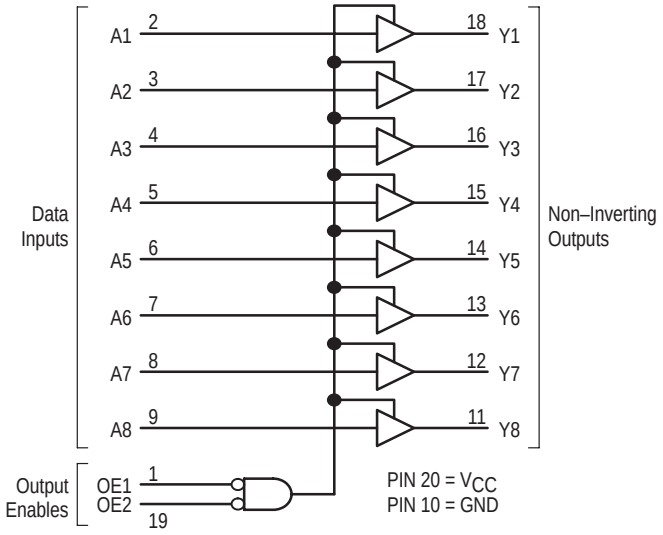
The MC74HC541A is identical in pinout to the LS541. The device inputs are compatible with Standard CMOS outputs. External pullup resistors make them compatible with LSTTL outputs.

The HC541A is an octal non–inverting buffer/line driver/line receiver designed to be used with 3–state memory address drivers, clock drivers, and other bus–oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active–low output enables.

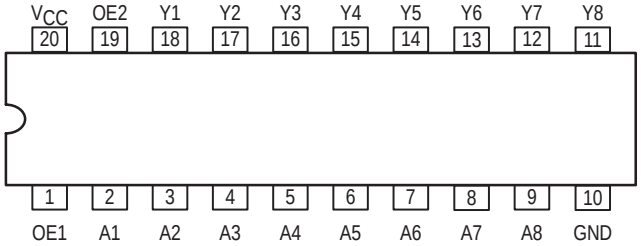
The HC541A is similar in function to the HC540A, which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2 to 6V
- Low Input Current: 1μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates

LOGIC DIAGRAM



Pinout: 20–Lead Packages (Top View)



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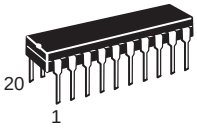
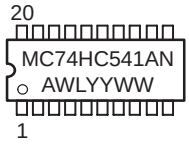
MARKING DIAGRAMS



PDIP–20
P SUFFIX
CASE 738



SOIC WIDE–20
DW SUFFIX
CASE 751D

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

FUNCTION TABLE

Inputs			Output Y
OE1	OE2	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Z = High Impedance
X = Don't Care

ORDERING INFORMATION

Device	Package	Shipping
MC74HC541AN	PDIP–20	1440 / Box
MC74HC541ADW	SOIC–WIDE	38 / Rail
MC74HC541ADWR2	SOIC–WIDE	1000 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP or SOIC Package	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature Range, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise/Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1V $\|I_{out}\|$ ≤ 20μA	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = V_{CC} – 0.1V $\|I_{out}\|$ ≤ 20μA	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IL} $\|I_{out}\|$ ≤ 20μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IL} $\|I_{out}\|$ ≤ 3.6mA $\|I_{out}\|$ ≤ 6.0mA $\|I_{out}\|$ ≤ 7.8mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} $\|I_{out}\|$ ≤ 20μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} $\|I_{out}\|$ ≤ 3.6mA $\|I_{out}\|$ ≤ 6.0mA $\|I_{out}\|$ ≤ 7.8mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
I_{OZ}	Maximum Three–State Leakage Current	Output in High Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0 3.0 4.5 6.0	80 30 18 15	100 40 23 20	120 55 28 25	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 3.0 4.5 6.0	110 45 25 21	140 60 31 26	165 75 38 31	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 3.0 4.5 6.0	110 45 25 21	140 60 31 26	165 75 38 31	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 3.0 4.5 6.0	60 22 12 10	75 28 15 13	90 34 18 15	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High Impedance State)		15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V, V_{EE} = 0 V	
C_{PD}	Power Dissipation Capacitance (Per Buffer)*	35	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

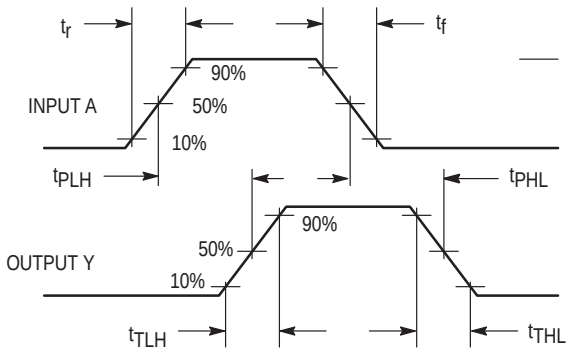


Figure 1.

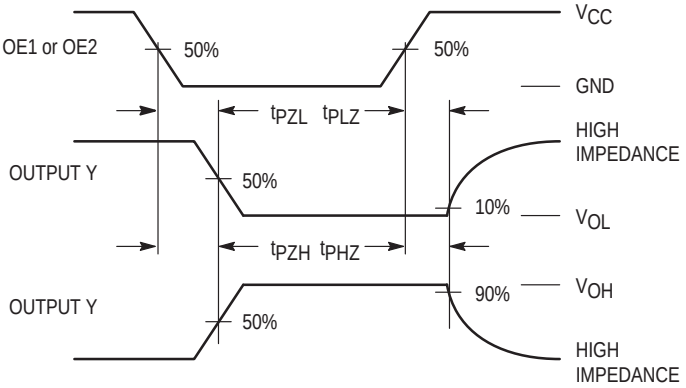
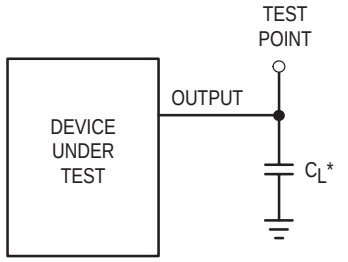


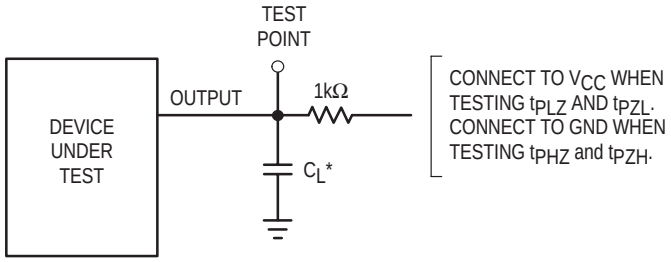
Figure 2.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 3.



*Includes all probe and jig capacitance

Figure 4.

PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, A5, A6, A7, A8 (PINS 2, 3, 4, 5, 6, 7, 8, 9) — Data input pins. Data on these pins appear in non–inverted form on the corresponding Y outputs, when the outputs are enabled.

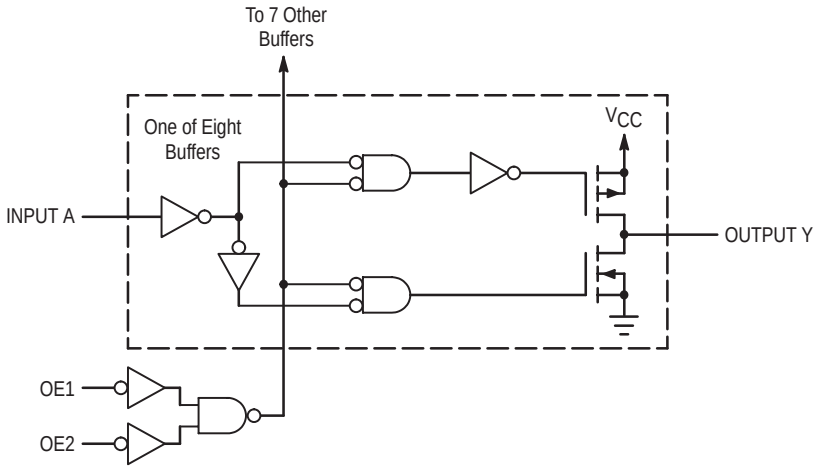
CONTROLS

OE1, OE2 (PINS 1, 19) — Output enables (active–low). When a low voltage is applied to both of these pins, the outputs are enabled and the device functions as an non–inverting buffer. When a high voltage is applied to either input, the outputs assume the high impedance state.

OUTPUTS

Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11) — Device outputs. Depending upon the state of the output enable pins, these outputs are either non–inverting outputs or high–impedance outputs.

LOGIC DETAIL



MC74HCT541A

Octal 3-State Non-Inverting Buffer/Line Driver/ Line Receiver With LSTTL-Compatible Inputs

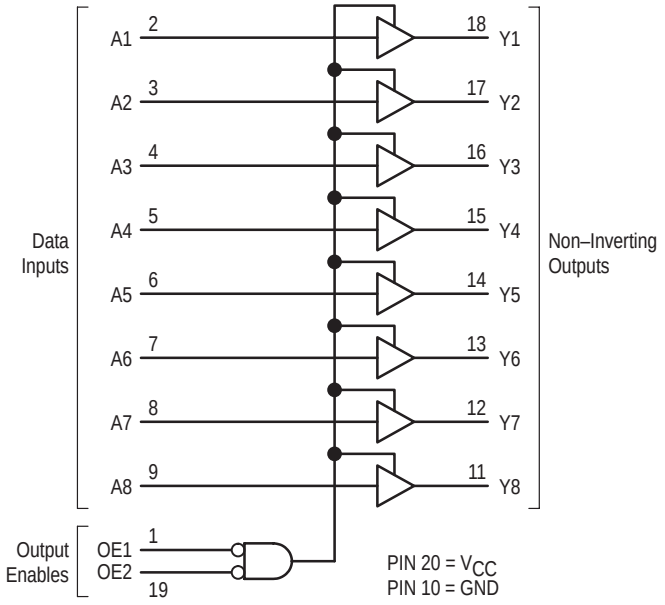
High–Performance Silicon–Gate CMOS

The MC74HCT541A is identical in pinout to the LS541. This device may be used as a level converter for interfacing TTL or NMOS outputs to high speed CMOS inputs.

The HCT541A is an octal non–inverting buffer/line driver/line receiver designed to be used with 3–state memory address drivers, clock drivers, and other bus–oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active–low output enables.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS–Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5V
- Low Input Current: 1μA
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates

LOGIC DIAGRAM



ON Semiconductor

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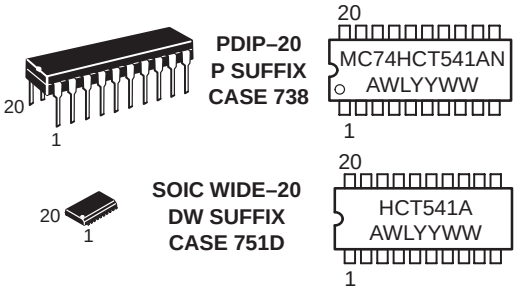
MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

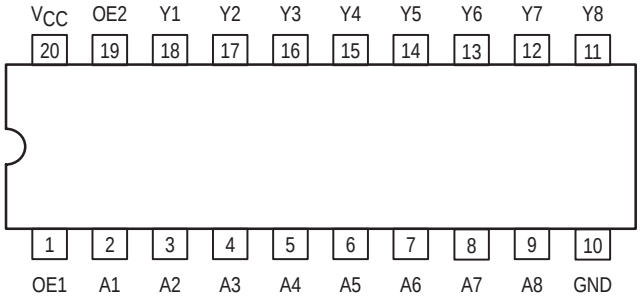
Device	Package	Shipping
MC74HCT541AN	PDIP–20	1440 / Box
MC74HCT541ADW	SOIC–WIDE	38 / Rail
MC74HCT541ADWR2	SOIC–WIDE	1000 / Reel

FUNCTION TABLE

Inputs			Output Y
OE1	OE2	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Z = High Impedance
X = Don't Care

Pinout: 20–Lead Packages (Top View)



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air Plastic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP or SOIC Package	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature Range, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise/Fall Time (Figure 1)	0	500	ns

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1V or V_{CC} – 0.1V $\|I_{out}\|$ ≤ 20μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1V or V_{CC} – 0.1V $\|I_{out}\|$ ≤ 20μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6.0mA	4.5	3.98	3.84	3.70	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6.0mA	4.5	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	5.5	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	Output in High Impedance State V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0μA	5.5	4	40	160	μA

ΔI_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4V, Any One Input V_{in} = V_{CC} or GND, Other Inputs I_{out} = 0μA	5.5	≥ –55°C 2.9	25 to 125°C 2.4	mA

1. Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).
2. Total Supply Current = I_{CC} + $\Sigma\Delta I_{CC}$.

AC CHARACTERISTICS (V_{CC} = 5.0V, C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	23	28	32	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	30	34	38	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	30	34	38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High Impedance State)	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Buffer)*	55	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

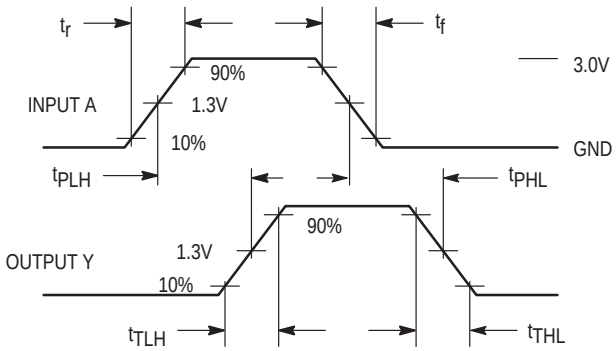


Figure 1.

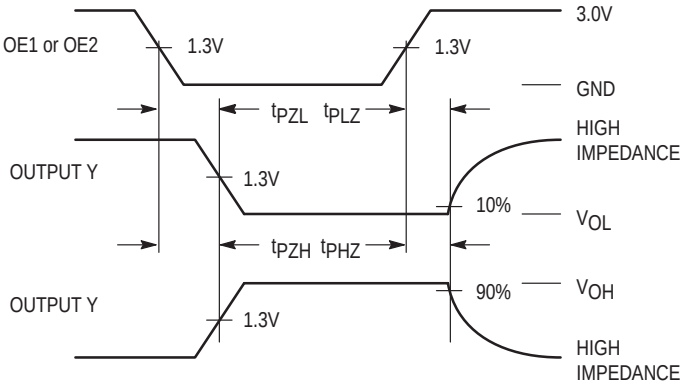
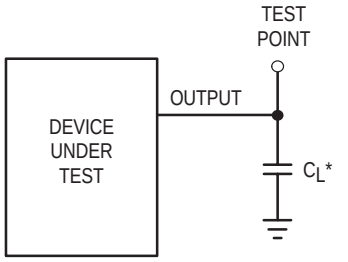


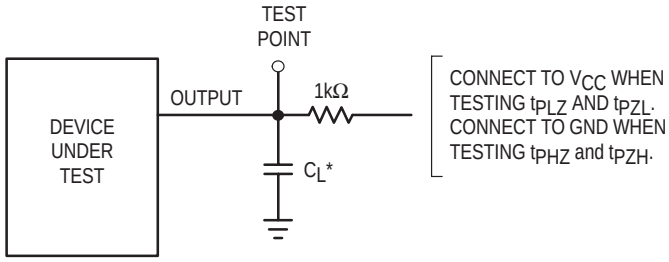
Figure 2.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 3.



*Includes all probe and jig capacitance

Figure 4.

PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, A5, A6, A7, A8 (PINS 2, 3, 4, 5, 6, 7, 8, 9) — Data input pins. Data on these pins appear in non–inverted form on the corresponding Y outputs, when the outputs are enabled.

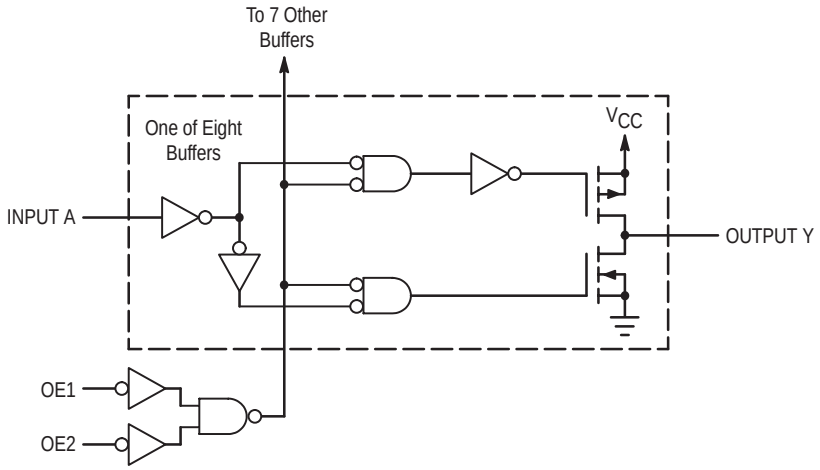
CONTROLS

OE1, OE2 (PINS 1, 19) — Output enables (active–low). When a low voltage is applied to both of these pins, the outputs are enabled and the device functions as a non–inverting buffer. When a high voltage is applied to either input, the outputs assume the high impedance state.

OUTPUTS

Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11) — Device outputs. Depending upon the state of the output enable pins, these outputs are either non–inverting outputs or high–impedance outputs.

LOGIC DETAIL



MC74HC573A

Octal 3-State Noninverting Transparent Latch

High–Performance Silicon–Gate CMOS

The MC74HC573A is identical in pinout to the LS573. The devices are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

The HC573A is identical in function to the HC373A but has the data inputs on the opposite side of the package from the outputs to facilitate PC board layout.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 218 FETs or 54.5 Equivalent Gates

ON Semiconductor

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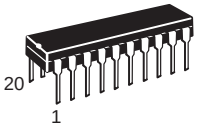
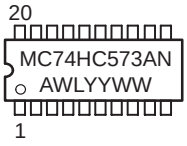
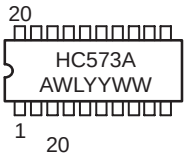
MARKING DIAGRAMS

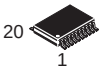


PDIP–20
P SUFFIX
CASE 738

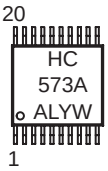


SOIC WIDE–20
DW SUFFIX
CASE 751D





TSSOP–20
DT SUFFIX
CASE 948G

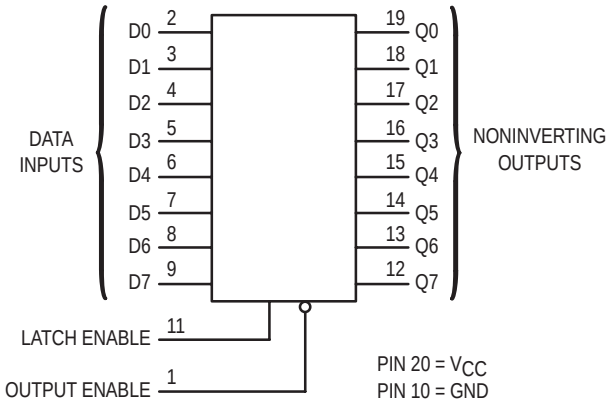


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

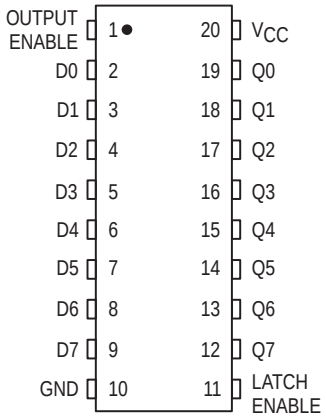
ORDERING INFORMATION

Device	Package	Shipping
MC74HC573AN	PDIP–20	1440 / Box
MC74HC573ADW	SOIC–WIDE	38 / Rail
MC74HC573ADWR2	SOIC–WIDE	1000 / Reel
MC74HC573ADT	TSSOP–20	75 / Rail
MC74HC573ADTR2	TSSOP–20	2500 / Reel

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
Output Enable	**Latch Enable**	**D**	**Q**
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

X = Don't Care
Z = High Impedance

Design Criteria	Value	Units
Internal Gate Count*	54.5	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	0.0075	pJ

*Equivalent to a two–input NAND gate.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, TSSOP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: –10 mW/°C from 65° to 125°C
SOIC Package: –7 mW/°C from 65° to 125°C
TSSOP Package: –6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time V_{CC} = 2.0 V (Figure 1) V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1 8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 2.4mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{OL}	Maximum Low–Level Output Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq$ 2.4mA $\|I_{out}\| \leq$ 6.0 mA $\|I_{out}\| \leq$ 7.8 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	6.0	– 0.5	– 5.0	– 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND $\|I_{out}\|$ = 0 μA	6.0	4.0	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	2.0 3.0 4.5 6.0	150 100 30 26	190 140 38 33	225 180 45 38	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	2.0 3.0 4.5 6.0	160 105 32 27	200 145 40 34	240 190 48 41	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 3.0 4.5 6.0	150 100 30 26	190 125 38 33	225 150 45 38	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 3.0 4.5 6.0	150 100 30 26	190 125 38 33	225 150 45 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0 3.0 4.5 6.0	60 27 12 10	75 32 15 13	90 36 18 15	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)		15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	23	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Fig.	V_{CC} Volts	Guaranteed Limit						Unit
				– 55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
t_{su}	Minimum Setup Time, Input D to Latch Enable	4	2.0 3.0 4.5 6.0	50 40 10 9.0		65 50 13 11		75 60 15 13		ns
t_h	Minimum Hold Time, Latch Enable to Input D	4	2.0 3.0 4.5 6.0	5.0 5.0 5.0 5.0		5.0 5.0 5.0 5.0		5.0 5.0 5.0 5.0		ns
t_w	Minimum Pulse Width, Latch Enable	2	2.0 3.0 4.5 6.0	75 60 15 13		95 80 19 16		110 90 22 19		ns
t_r, t_f	Maximum Input Rise and Fall Times	1	2.0 3.0 4.5 6.0		1000 800 500 400		1000 800 500 400		1000 800 500 400	ns

SWITCHING WAVEFORMS

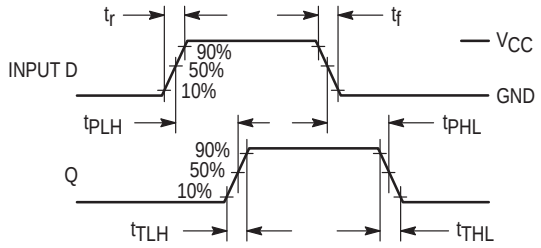


Figure 1.

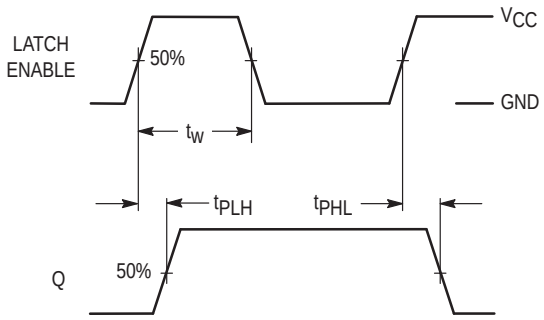


Figure 2.

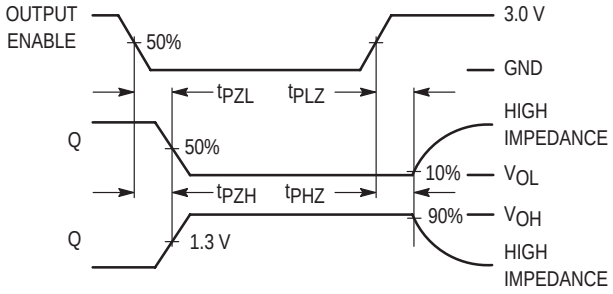


Figure 3.

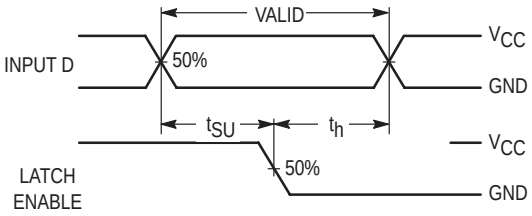
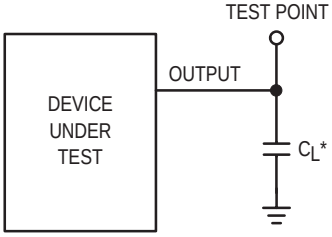
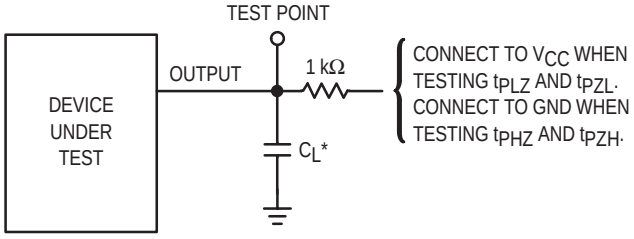


Figure 4.



*Includes all probe and jig capacitance

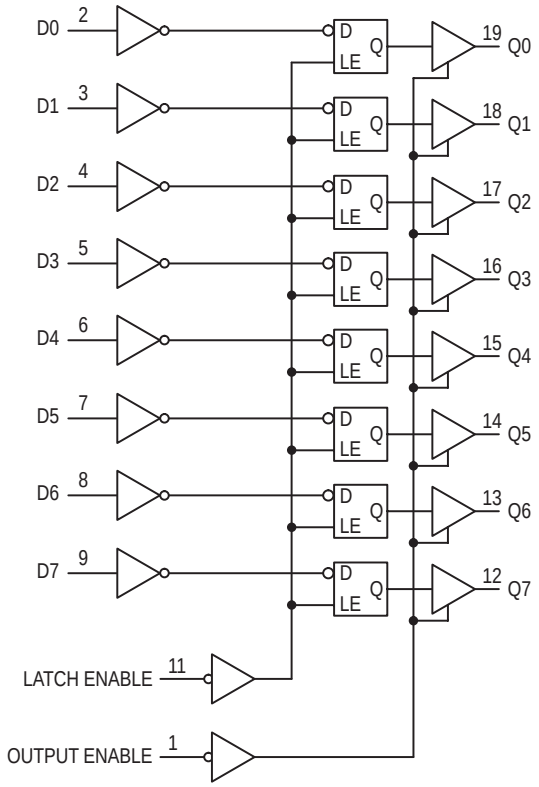
Figure 5. Test Circuit



*Includes all probe and jig capacitance

Figure 6. Test Circuit

EXPANDED LOGIC DIAGRAM



MC74HCT573A

Octal 3-State Noninverting Transparent Latch with LSTTL Compatible Inputs

High–Performance Silicon–Gate CMOS

The MC74HCT573A is identical in pinout to the LS573. This device may be used as a level converter for interfacing TTL or NMOS outputs to High–Speed CMOS inputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold times becomes latched.

The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high–impedance state. Thus, data may be latched even when the outputs are not enabled.

The HCT573A is identical in function to the HCT373A but has the Data Inputs on the opposite side of the package from the outputs to facilitate PC board layout.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS–Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 10 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates
  - — Improved Propagation Delays
  - — 50% Lower Quiescent Power

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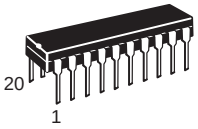
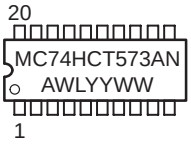
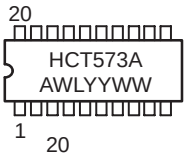
MARKING DIAGRAMS

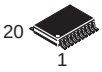


PDIP–20
P SUFFIX
CASE 738

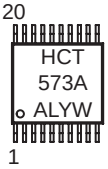


SOIC WIDE–20
DW SUFFIX
CASE 751D





TSSOP–20
DT SUFFIX
CASE 948G

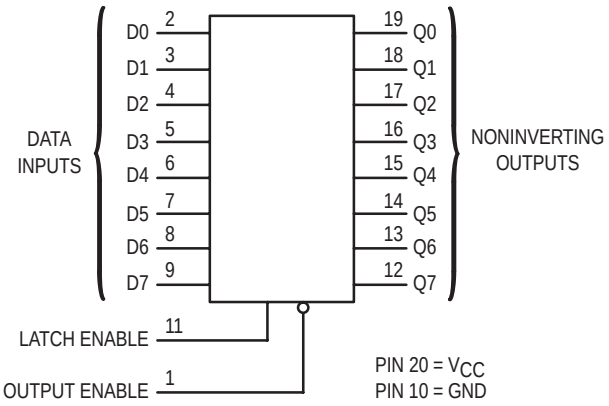


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

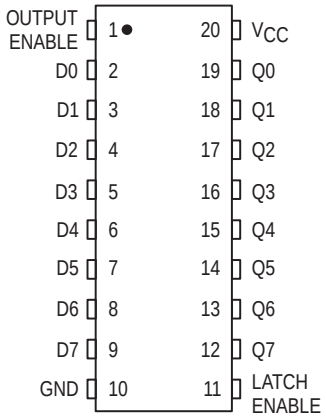
ORDERING INFORMATION

Device	Package	Shipping
MC74HCT573AN	PDIP–20	1440 / Box
MC74HCT573ADW	SOIC–WIDE	38 / Rail
MC74HCT573ADWR2	SOIC–WIDE	1000 / Reel
MC74HCT573ADT	TSSOP–20	75 / Rail
MC74HCT573ADTR2	TSSOP–20	2500 / Reel

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
Output Enable	**Latch Enable**	**D**	**Q**
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

X = Don't Care
Z = High Impedance

Design Criteria	Value	Units
Internal Gate Count*	58.5	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	0.0075	pJ

*Equivalent to a two–input NAND gate.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, TSSOP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: –10 mW/°C from 65° to 125°C
SOIC Package: –7 mW/°C from 65° to 125°C
TSSOP Package: –6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6.0 mA	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6.0 mA	4.5	0.26	0.33	0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	5.5	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} ≤ 0 μA	5.5	4.0	40	160	μA
ΔI_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4 V, Any One Input V_{in} = V_{CC} or GND, Other Inputs I_{out} = 0 μA	5.5	≥ – 55°C 2.9	25°C to 125°C 2.4		mA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input D to Output Q (Figures 1 and 5)	30	38	45	ns
t_{PLH} t_{PHL}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	30	38	45	ns
T_{PLZ}, T_{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	28	35	42	ns
t_{TZL}, t_{TZH}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	28	35	42	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, any Output (Figures 1 and 5)	12	15	18	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	48	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (V_{CC} = 5.0 V ± 10%, C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Fig.	Guaranteed Limit						Unit
			– 55 to 25°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
t_{su}	Minimum Setup Time, Input D to Latch Enable	4	10		13		15		ns
t_h	Minimum Hold Time, Latch Enable to Input D	4	5.0		5.0		5.0		ns
t_w	Minimum Pulse Width, Latch Enable	2	15		19		22		ns
t_r, t_f	Maximum Input Rise and Fall Times	1		500		500		500	ns

SWITCHING WAVEFORMS

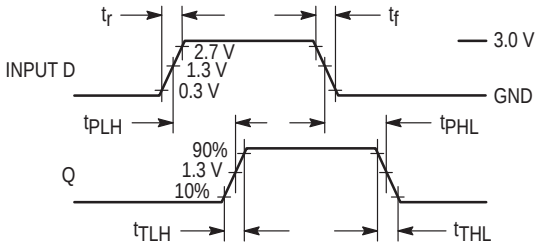


Figure 1.

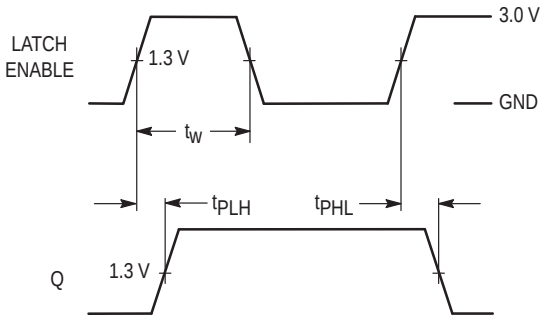


Figure 2.

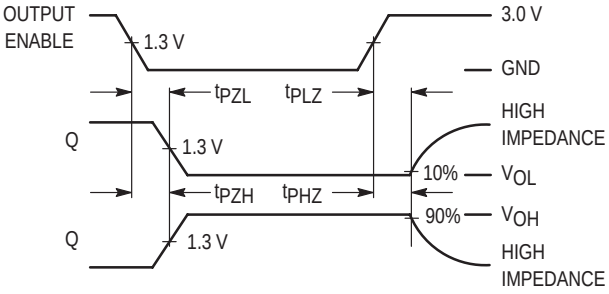


Figure 3.

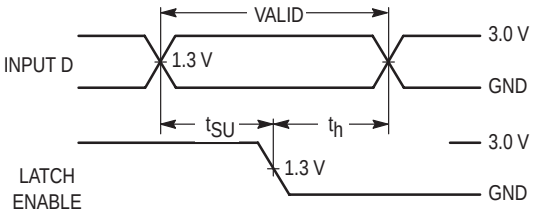
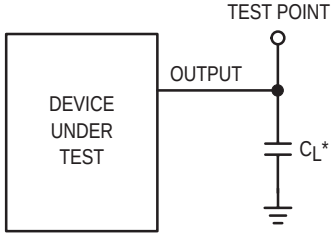
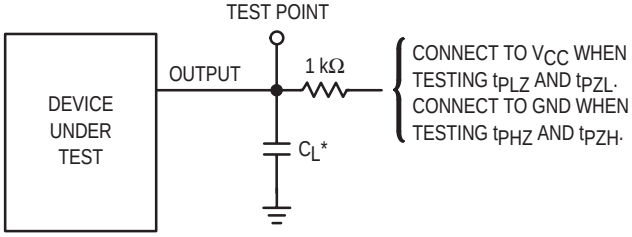


Figure 4.



*Includes all probe and jig capacitance

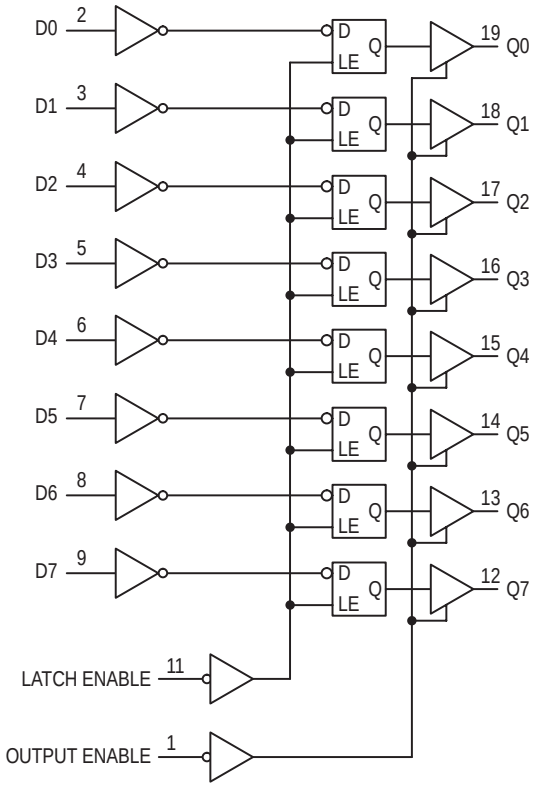
Figure 5. Test Circuit



*Includes all probe and jig capacitance

Figure 6. Test Circuit

EXPANDED LOGIC DIAGRAM



MC74HC574A

Octal 3-State Noninverting D Flip-Flop

High–Performance Silicon–Gate CMOS

The MC74HC574A is identical in pinout to the LS574. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Data meeting the setup time is clocked to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip–flops, but when Output Enable is high, all device outputs are forced to the high–impedance state. Thus, data may be stored even when the outputs are not enabled.

The HC574A is identical in function to the HC374A but has the flip–flop inputs on the opposite side of the package from the outputs to facilitate PC board layout.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 266 FETs or 66.5 Equivalent Gates

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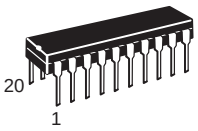
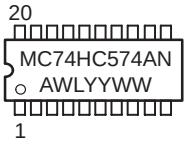
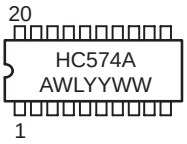
MARKING DIAGRAMS



PDIP–20
P SUFFIX
CASE 738



SOIC WIDE–20
DW SUFFIX
CASE 751D

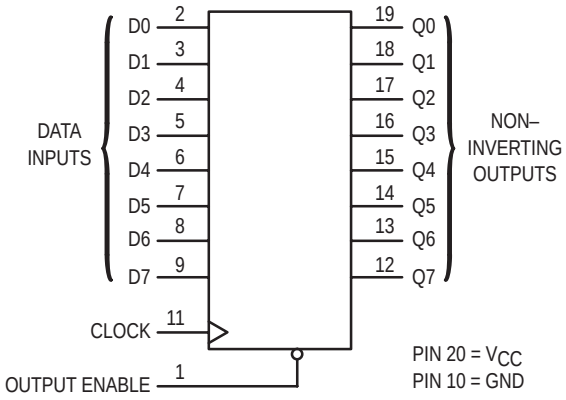


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

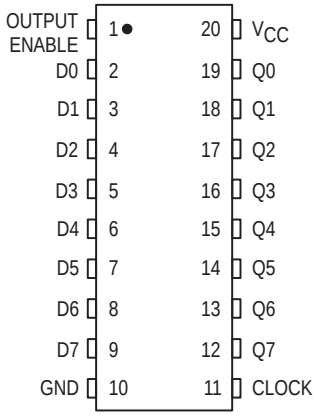
ORDERING INFORMATION

Device	Package	Shipping
MC74HC574AN	PDIP–20	1440 / Box
MC74HC574ADW	SOIC–WIDE	38 / Rail
MC74HC574ADWR2	SOIC–WIDE	1000 / Reel

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
OE	**Clock**	**D**	**Q**
L	↑	H	H
L	↑	L	L
L	L,H,↓	X	No Change
H	X	X	Z

X = Don't Care
Z = High Impedance

Design Criteria	Value	Units
Internal Gate Count*	66.5	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	0.0075	pJ

*Equivalent to a two–input NAND gate.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0 μA	6.0	4.0	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $\|I_{out}\|$ = 0 μA	6.0	4.0	40	160	μA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 3.0 4.5 6.0	6.0 15 30 35	4.8 10 24 28	4.0 8.0 20 24	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0 3.0 4.5 6.0	160 105 32 27	200 145 40 34	240 190 48 41	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0 3.0 4.5 6.0	150 100 30 26	190 125 38 33	225 150 45 38	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0 3.0 4.5 6 0	140 90 28 24	175 120 35 30	210 140 42 36	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, any Output (Figures 1 and 4)	2.0 3.0 4.5 6.0	60 27 12 10	75 32 15 13	90 36 18 15	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance, Output in High–Impedance State		15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	24	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Fig.	V_{CC} Volts	Guaranteed Limit						Unit
				– 55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
t_{su}	Minimum Setup Time, Data to Clock	3	2.0 3.0 4.6 6.0	50 40 10 9.0		65 50 13 11		75 60 15 13		ns
t_h	Minimum Hold Time, Clock to Data	3	2.0 3.0 4.5 6.0	5.0 5.0 5.0 5.0		5.0 5.0 5.0 5.0		5.0 5.0 5.0 5.0		ns
t_w	Minimum Pulse Width, Clock	1	2.0 3.0 4.5 6.0	75 60 15 13		95 80 19 16		110 90 22 19		ns
t_r, t_f	Maximum Input Rise and Fall Times	1	2.0 3.0 4.5 6.0		1000 800 500 400		1000 800 500 400		1000 800 500 400	ns

SWITCHING WAVEFORMS

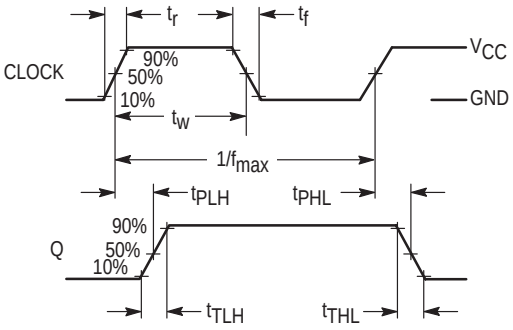


Figure 1.

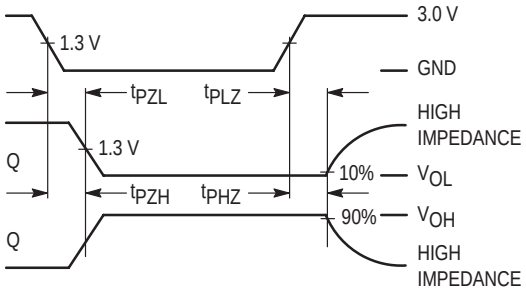


Figure 2.

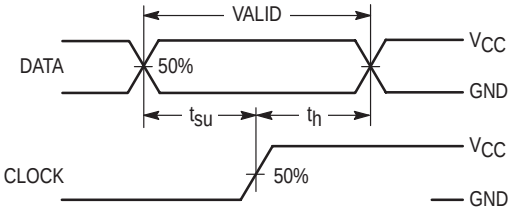
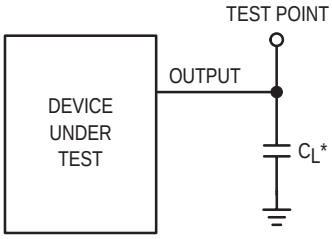
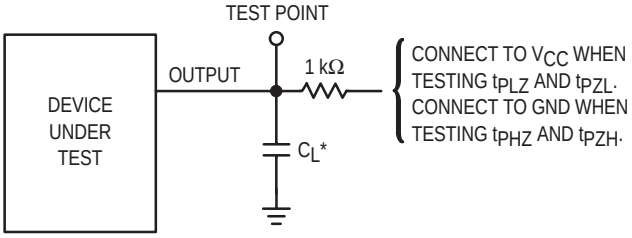


Figure 3.



*Includes all probe and jig capacitance

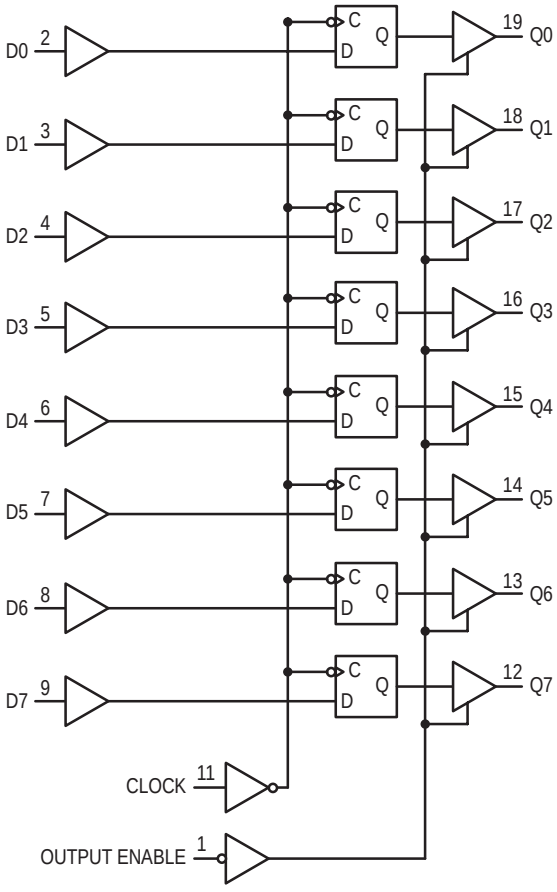
Figure 4.



*Includes all probe and jig capacitance

Figure 5. Test Circuit

EXPANDED LOGIC DIAGRAM



MC74HCT574A

Octal 3-State Noninverting D Flip-Flop with LSTTL-Compatible Inputs

High–Performance Silicon–Gate CMOS

The MC74HCT574A is identical in pinout to the LS574. This device may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

Data meeting the setup time is clocked to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip–flops, but when Output Enable is high, all device outputs are forced to the high–impedance state. Thus, data may be stored even when the outputs are not enabled.

The HCT574A is identical in function to the HCT374A but has the flip–flop inputs on the opposite side of the package from the outputs to facilitate PC board layout.

- Output Drive Capability: 15 LSTTL Loads
- TTL NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 286 FETs or 71.5 Equivalent Gates

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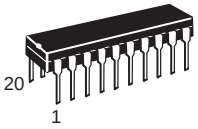
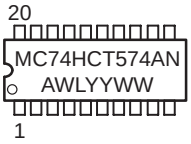
MARKING DIAGRAMS



PDIP–20
P SUFFIX
CASE 738



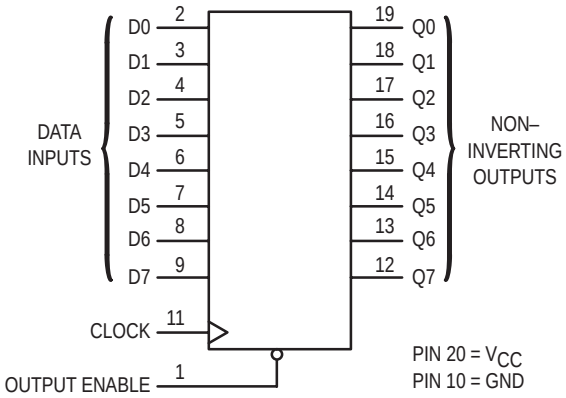
SOIC WIDE–20
DW SUFFIX
CASE 751D

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

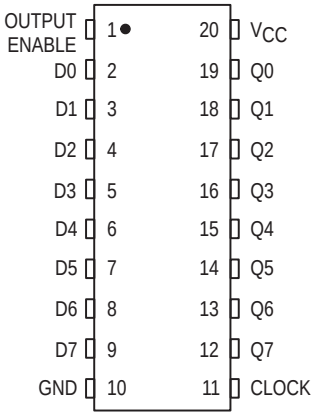
ORDERING INFORMATION

Device	Package	Shipping
MC74HCT574AN	PDIP–20	1440 / Box
MC74HCT574ADW	SOIC–WIDE	38 / Rail
MC74HCT574ADWR2	SOIC–WIDE	1000 / Reel

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
OE	**Clock**	**D**	**Q**
L	↑	H	H
L	↑	L	L
L	L,H,↓	X	No Change
H	X	X	Z

X = don't care
Z = high impedance

Design Criteria	Value	Units
Internal Gate Count*	71.5	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	0.0075	pJ

*Equivalent to a two–input NAND gate.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: –10 mW/°C from 65° to 125°C
SOIC Package: –7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6.0 mA	4.5	3.98	3.84	3.7	V
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6.0 mA	4.5	0.26	0.33	0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	5.5	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	5.5	4.0	40	160	μA

1. Output in high–impedance state.
NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
I_{OZ}	Maximum Three–State Leakage Current	V_{in} = V_{IL} or V_{IH} (Note 1) V_{out} = V_{CC} or GND	5.5	– 0.5	– 5.0	– 10	μA

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit		Unit
				≥ – 55°C	25°C to 125°C	
ΔI_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4 V, Any One Input V_{in} = V_{CC} or GND, Other Inputs I_{out} = 0 μA	5.5	2.9	2.4	mA

1. Output in high–impedance state.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, C_L = 50 pF, Input t_r = t_f = 6.0 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{MAX}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	30	24	20	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	30	38	45	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Propagation Delay Time, Output Enable to Q (Figures 2 and 5)	28	35	42	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1, 2 and 4)	12	15	18	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

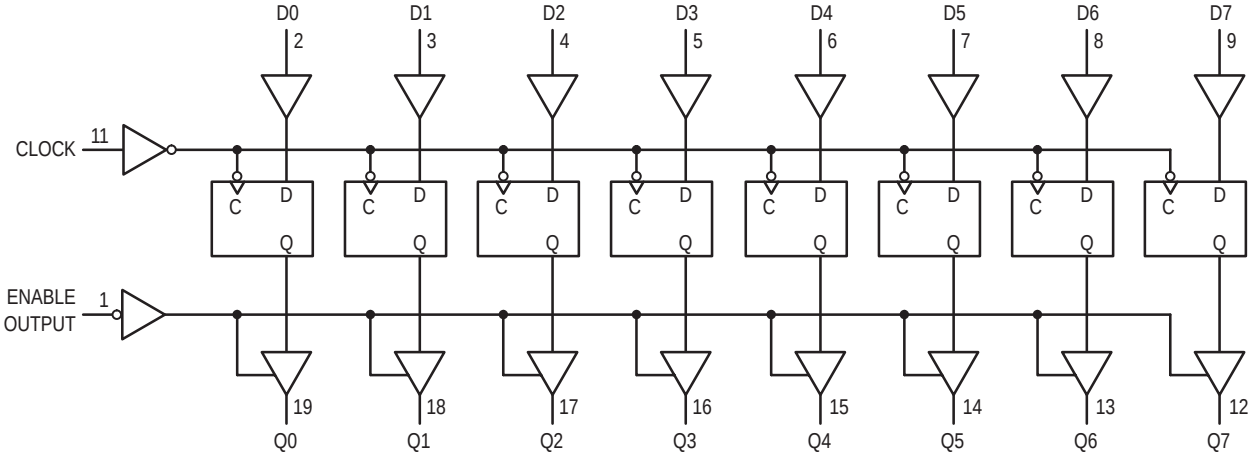
		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Flip–Flop)*	58	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (V_{CC} = 5.0 V ± 10%, C_L = 50 pF, Input t_r = t_f = 6.0 ns)

Symbol	Parameter	Fig.	Guaranteed Limit						Unit
			– 55 to 25°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
t_{su}	Minimum Setup Time, Data to Clock	3	10		13		15		ns
t_h	Minimum Hold Time, Clock to Data	3	5.0		5.0		5.0		ns
t_w	Minimum Pulse Width, Clock	1	15		19		22		ns
t_r, If	Maximum Input Rise and Fall Times	1		500		500		500	ns

EXPANDED LOGIC DIAGRAM



SWITCHING WAVEFORMS

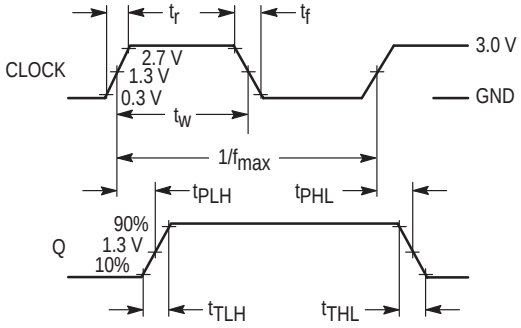


Figure 1.

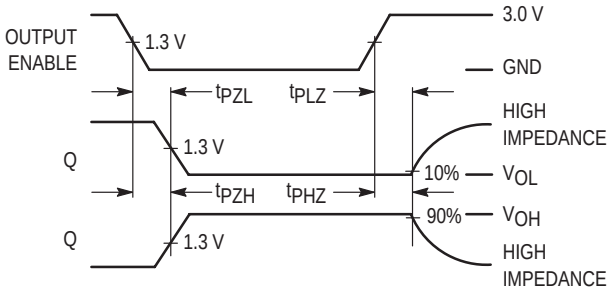


Figure 2.

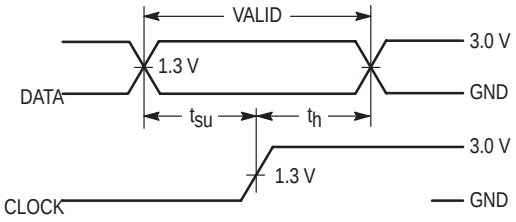
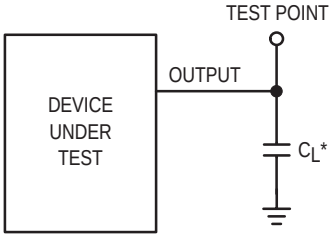
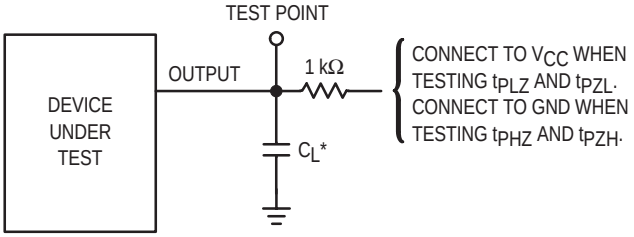


Figure 3.



*Includes all probe and jig capacitance

Figure 4. Test Circuit



*Includes all probe and jig capacitance

Figure 5. Test Circuit

MC74HC589A

8-Bit Serial or Parallel-Input/Serial-Output Shift Register with 3-State Output

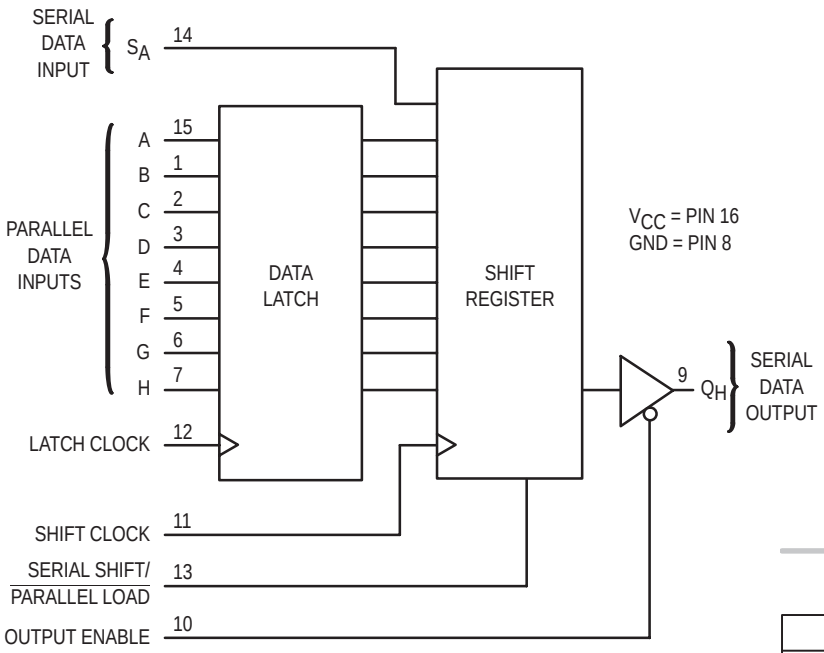
High–Performance Silicon–Gate CMOS

The MC74HC589A device consists of an 8–bit storage latch which feeds parallel data to an 8–bit shift register. Data can also be loaded serially (see Function Table). The shift register output, Q_H, is a three–state output, allowing this device to be used in bus–oriented systems.

The HC589A directly interfaces with the SPI serial data port on CMOS MPUs and MCUs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 526 FETs or 131.5 Equivalent Gates

LOGIC DIAGRAM



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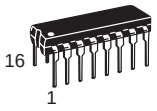
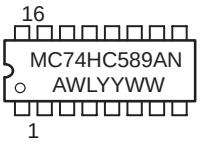
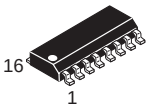
MARKING DIAGRAMS

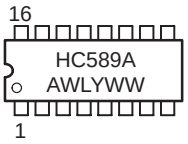


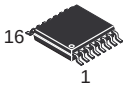
PDIP–16
N SUFFIX
CASE 648





SO–16
D SUFFIX
CASE 751B

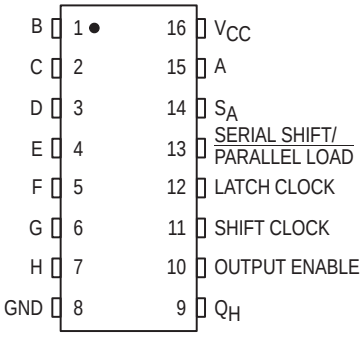




TSSOP–16
DT SUFFIX
CASE 948F

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HC589AN	PDIP–16	2000 / Box
MC74HC589AD	SOIC–16	48 / Rail
MC74HC589ADR2	SOIC–16	2500 / Reel
MC74HC589ADT	TSSOP–16	96 / Rail
MC74HC589ADTR2	TSSOP–16	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: –10 mW/°C from 65° to 125°C
SOIC Package: –7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0 V	0	1000	ns
		V_{CC} = 3.0 V	0	TBD	
	(Figure 1)	V_{CC} = 4.5 V	0	500	
		V_{CC} = 6.0 V		400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit – 55 to 25°C	Guaranteed Limit ≤ 85°C	Guaranteed Limit ≤ 125°C	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0 μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 8)	2.0 3.0 4.5 6.0	6.0 TBD 30 35	4.8 TBD 24 28	4.0 TBD 20 24	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Latch Clock to Q_H (Figures 1 and 8)	2.0 3.0 4.5 6.0	175 100 40 30	225 110 50 40	275 125 60 50	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Shift Clock to Q_H (Figures 2 and 8)	2.0 3.0 4.5 6.0	160 90 30 25	200 130 40 30	240 160 48 40	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Serial Shift/$\overline{\text{Parallel Load}}$ to Q_H (Figures 4 and 8)	2.0 3.0 4.5 6.0	160 90 30 25	200 130 40 30	240 160 48 40	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Q_H (Figures 3 and 9)	2.0 3.0 4.5 6.0	150 80 27 23	170 100 30 25	200 130 40 30	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Q_H (Figures 3 and 9)	2.0 3.0 4.5 6.0	150 80 27 23	170 100 30 25	200 130 40 30	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 8)	2.0 3.0 4.5 6.0	60 TBD 12 10	75 TBD 15 13	90 TBD 18 15	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)	—	15	15	15	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package)*	50	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, A–H to Latch Clock (Figure 5)	2.0 3.0 4.5 6.0	100 TBD 20 17	125 TBD 25 21	150 TBD 30 26	ns
t_{su}	Minimum Setup Time, Serial Data Input S_A to Shift Clock (Figure 6)	2.0 3.0 4.5 6.0	100 TBD 20 17	125 TBD 25 21	150 TBD 30 26	ns
t_{su}	Minimum Setup Time, Serial Shift/$\overline{\text{Parallel Load}}$ to Shift Clock (Figure 7)	2.0 3.0 4.5 6.0	100 TBD 20 17	125 TBD 25 21	150 TBD 30 26	ns
t_h	Minimum Hold Time, Latch Clock to A–H (Figure 5)	2.0 3.0 4.5 6.0	25 TBD 5 5	30 TBD 6 6	40 TBD 8 7	ns
t_h	Minimum Hold Time, Shift Clock to Serial Data Input S_A (Figure 6)	2.0 3.0 4.5 6.0	5 5 5 5	5 5 5 5	5 5 5 5	ns
t_w	Minimum Pulse Width, Shift Clock (Figure 2)	2.0 3.0 4.5 6.0	75 TBD 15 13	95 TBD 19 16	110 TBD 23 19	ns
t_w	Minimum Pulse Width, Latch Clock (Figure 1)	2.0 3.0 4.5 6.0	80 TBD 16 14	100 TBD 20 17	120 TBD 24 20	ns
t_w	Minimum Pulse Width, Serial Shift/$\overline{\text{Parallel Load}}$ (Figure 4)	2.0 3.0 4.5 6.0	80 TBD 16 14	100 TBD 20 17	120 TBD 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 3.0 4.5 6.0	1000 TBD 500 400	1000 TBD 500 400	1000 TBD 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

FUNCTION TABLE

Operation	Inputs						Resulting Function		
	Output Enable	Serial Shift/ $\overline{\text{Parallel Load}}$	Latch Clock	Shift Clock	Serial Input S_A	Parallel Inputs A–H	Data Latch Contents	Shift Register Contents	Output Q_H
Force output into high impedance state	H	X	X	X	X	X	X	X	Z
Load parallel data into data latch	L	H	↑	L, ↓	X	a–h	a–h	U	U
Transfer latch contents to shift register	L	L	L, ↓	X	X	X	U	LR_N SR_N	LR_H
Contents of input latch and shift register are unchanged	L	H	L, ↓	L, ↓	X	X	U	U	U
Load parallel data into data latch and shift register	L	L	↑	X	X	a–h	a–h	a–h	h
Shift serial data into shift register	L	H	X	↑	D	X	*	SR_A = D, SR_N SR_{N+1}	SR_G SR_H
Load parallel data in data latch and shift serial data into shift register	L	H	↑	↑	D	a–h	a–h	SR_A = D, SR_N SR_{N+1}	SR_G SR_H

LR = latch register contents
SR = shift register contents
a–h = data at parallel data inputs A–H
D = data (L, H) at serial data input S_A
U = remains unchanged
X = don't care
Z = high impedance
* = depends on Latch Clock input

SWITCHING WAVEFORMS

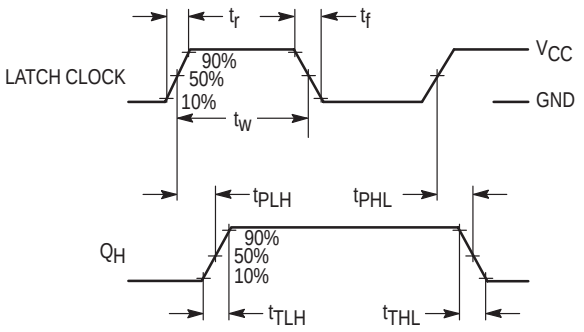


Figure 1. (Serial Shift/$\overline{\text{Parallel Load}}$ = L)

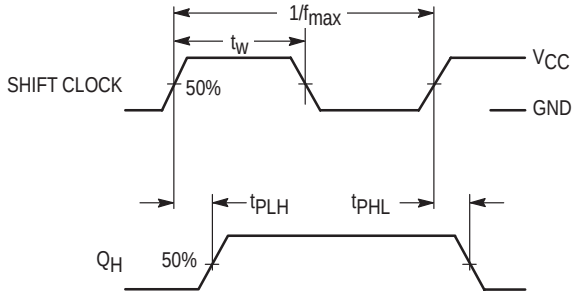
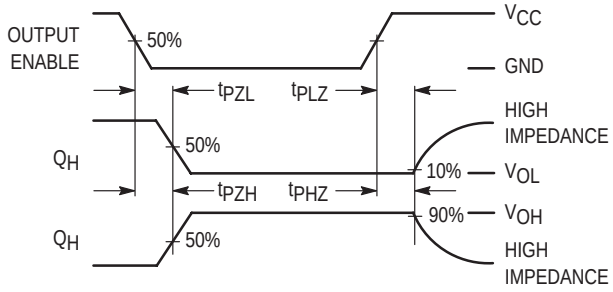


Figure 2. (Serial Shift/$\overline{\text{Parallel Load}}$ = H)



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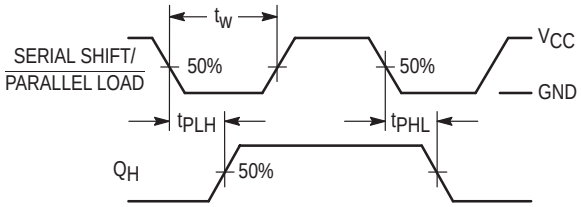

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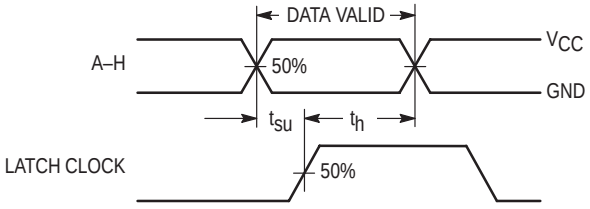


Figure 5.

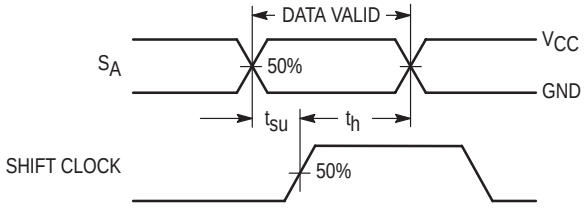


Figure 6.

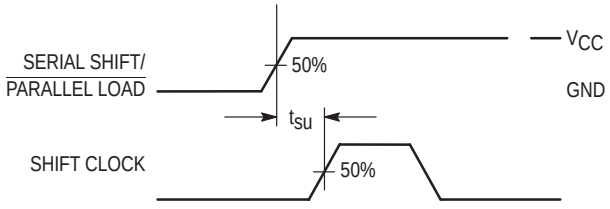
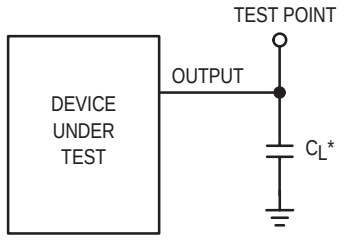


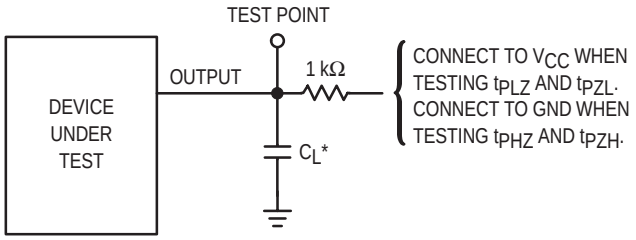
Figure 7.



*Includes all probe and jig capacitance

Figure 8. Test Circuit

TEST CIRCUIT



*Includes all probe and jig capacitance

Figure 9.

PIN DESCRIPTIONS

DATA INPUTS
A, B, C, D, E, F, G, H (Pins 15, 1, 2, 3, 4, 5, 6, 7)

Parallel data inputs. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.

S_A (Pin 14)

Serial data input. Data on this input is shifted into the shift register on the rising edge of the Shift Clock input if Serial Shift/$\overline{\text{Parallel Load}}$ is high. Data on this input is ignored when Serial Shift/$\overline{\text{Parallel Load}}$ is low.

CONTROL INPUTS
Serial Shift/$\overline{\text{Parallel Load}}$ (Pin 13)

Shift register mode control. When a high level is applied to this pin, the shift register is allowed to serially shift data. When a low level is applied to this pin, the shift register accepts parallel data from the data latch.

Shift Clock (Pin 11)

Serial shift clock. A low–to–high transition on this input shifts data on the serial data input into the shift register and data in stage H is shifted out Q_H, being replaced by the data previously stored in stage G.

Latch Clock (Pin 12)

Data latch clock. A low–to–high transition on this input loads the parallel data on inputs A–H into the data latch.

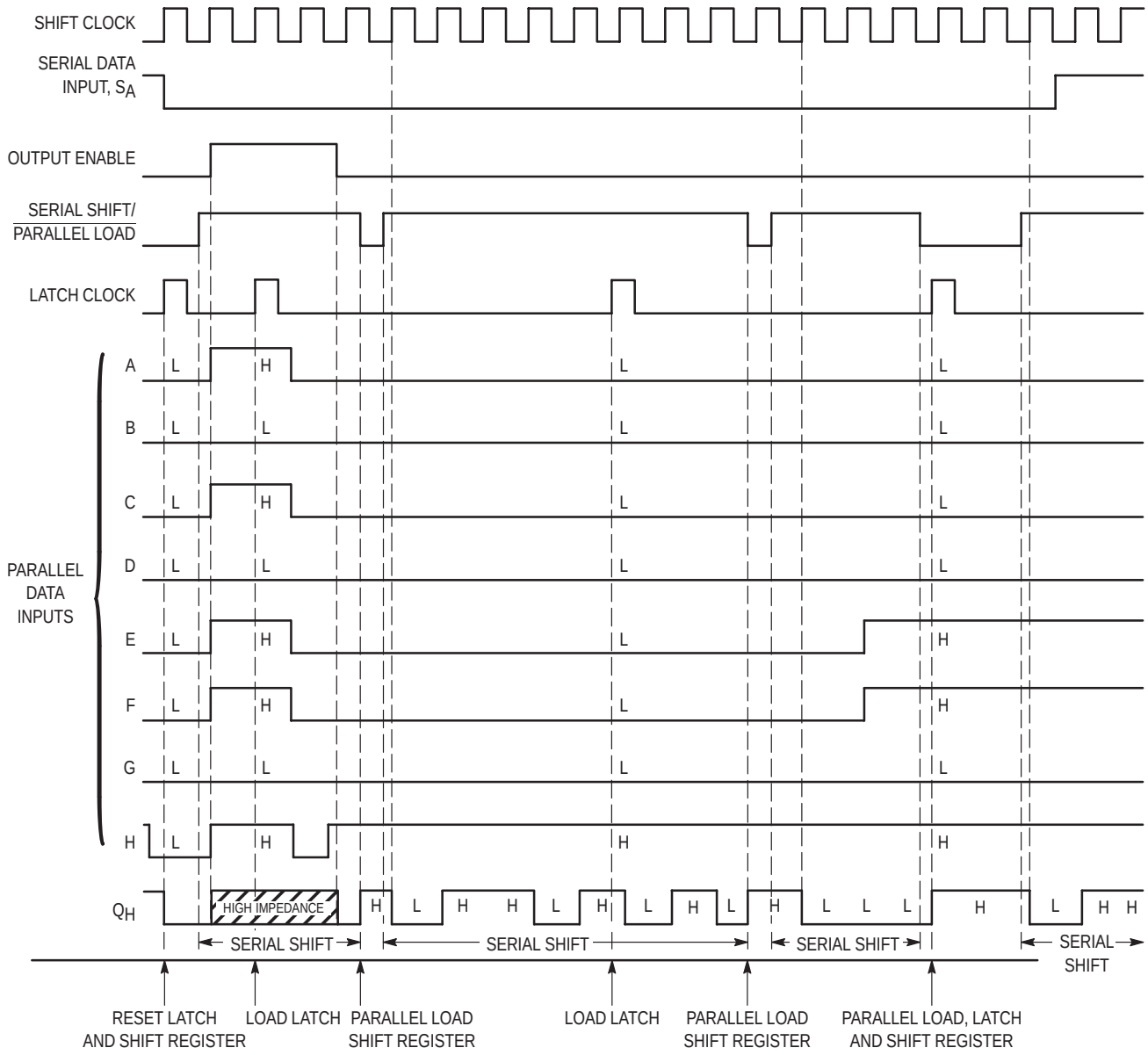
Output Enable (Pin 10)

Active–low output enable A high level applied to this pin forces the Q_H output into the high impedance state. A low level enables the output. This control does not affect the state of the input latch or the shift register.

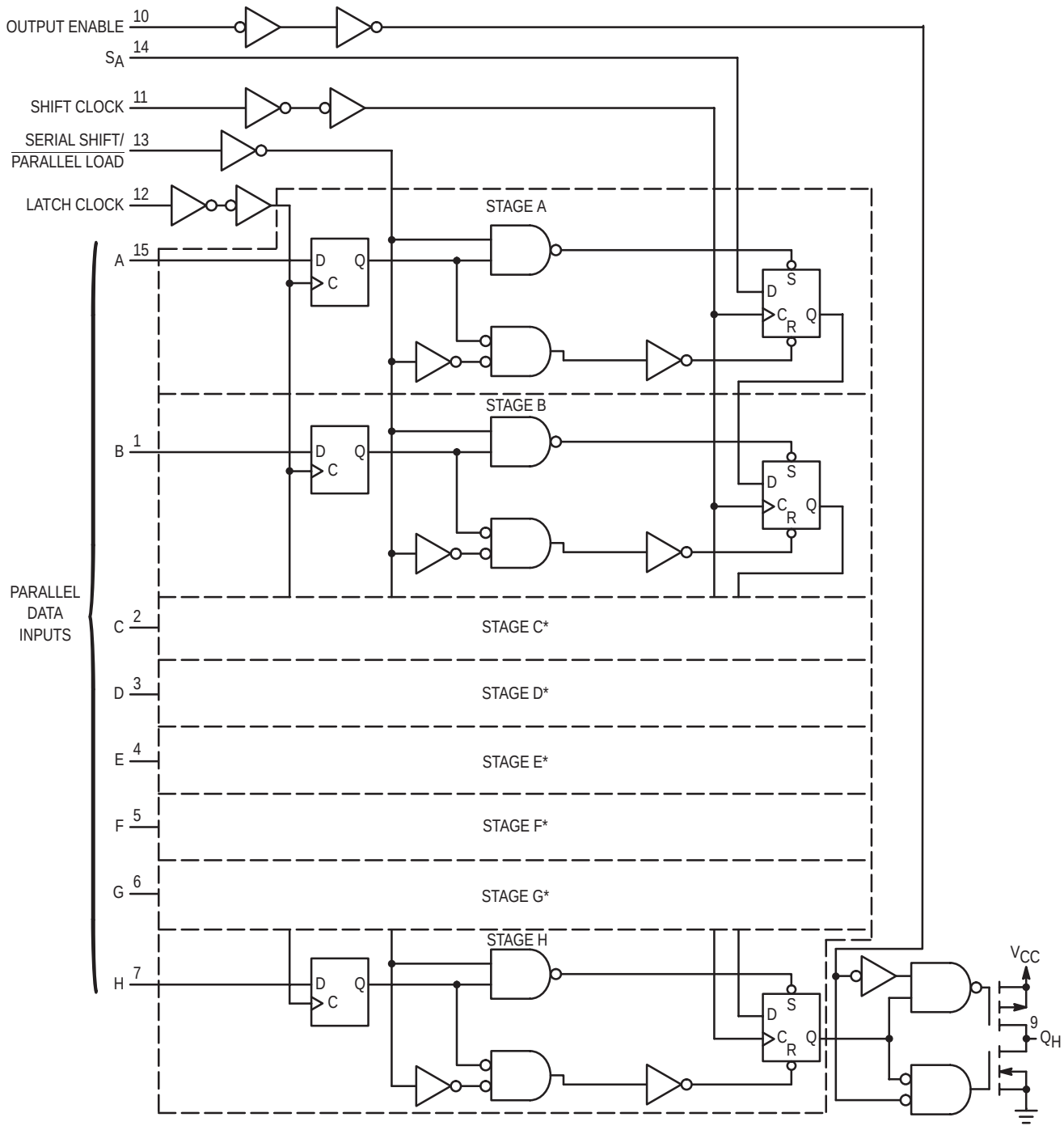
OUTPUT
Q_H (Pin 9)

Serial data output. This pin is the output from the last stage of the shift register. This is a 3–state output.

TIMING DIAGRAM



LOGIC DETAIL



*NOTE: Stages C thru G (not shown in detail) are identical to stages A and B above.

MC74HC595A

8-Bit Serial-Input/Serial or Parallel-Output Shift Register with Latched 3-State Outputs

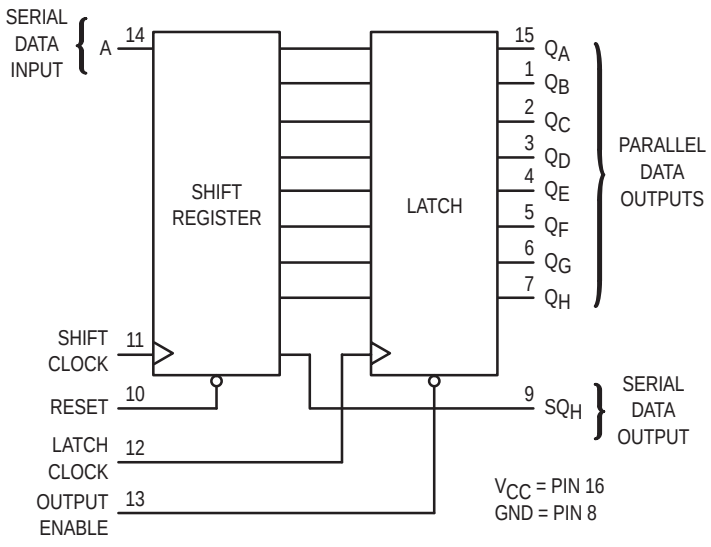
High–Performance Silicon–Gate CMOS

The MC74HC595A consists of an 8–bit shift register and an 8–bit D–type latch with three–state parallel outputs. The shift register accepts serial data and provides a serial output. The shift register also provides parallel data to the 8–bit latch. The shift register and latch have independent clock inputs. This device also has an asynchronous reset for the shift register.

The HC595A directly interfaces with the SPI serial data port on CMOS MPUs and MCUs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 328 FETs or 82 Equivalent Gates
- Improvements over HC595
  - — Improved Propagation Delays
  - — 50% Lower Quiescent Power
  - — Improved Input Noise and Latchup Immunity

LOGIC DIAGRAM



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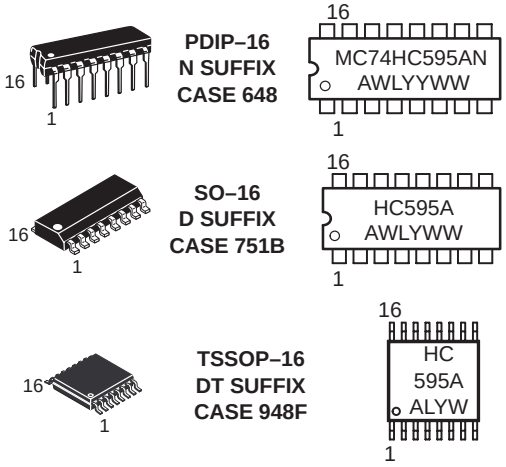
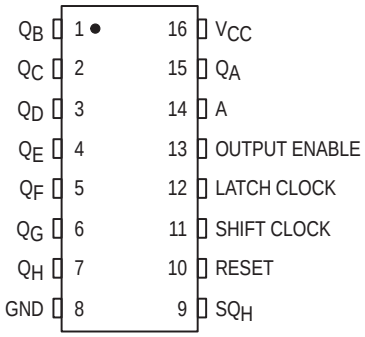
MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HC595AN	PDIP–16	2000 / Box
MC74HC595AD	SOIC–16	48 / Rail
MC74HC595ADR2	SOIC–16	2500 / Reel
MC74HC595ADT	TSSOP–16	96 / Rail
MC74HC595ADTR2	TSSOP–16	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage, Q_A – Q_H	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V_{OL}	Maximum Low–Level Output Voltage, Q_A – Q_H	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{OH}	Minimum High–Level Output Voltage, SQ_H	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 2.4$ mA $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	3.0 4.5 6.0	2.98 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V_{OL}	Maximum Low–Level Output Voltage, SQ_H	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 2.4$ mA $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three–State Leakage Current, $Q_A - Q_H$	Output in High–Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μA	6.0	4.0	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 7)	2.0 3.0 4.5 6.0	6.0 15 30 35	4.8 10 24 28	4.0 8.0 20 24	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Shift Clock to SQ_H (Figures 1 and 7)	2.0 3.0 4.5 6.0	140 100 28 24	175 125 35 30	210 150 42 36	ns
t_{PHL}	Maximum Propagation Delay, Reset to SQ_H (Figures 2 and 7)	2.0 3.0 4.5 6.0	145 100 29 25	180 125 36 31	220 150 44 38	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Latch Clock to $Q_A - Q_H$ (Figures 3 and 7)	2.0 3.0 4.5 6.0	140 100 28 24	175 125 35 30	210 150 42 36	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to $Q_A - Q_H$ (Figures 4 and 8)	2.0 3.0 4.5 6.0	150 100 30 26	190 125 38 33	225 150 45 38	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to $Q_A - Q_H$ (Figures 4 and 8)	2.0 3.0 4.5 6.0	135 90 27 23	170 110 34 29	205 130 41 35	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, $Q_A - Q_H$ (Figures 3 and 7)	2.0 3.0 4.5 6.0	60 23 12 10	75 27 15 13	90 31 18 15	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{TLH}, t_{THL}	Maximum Output Transition Time, SQ_H (Figures 1 and 7)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State), $Q_A – Q_H$	—	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package)*	300	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to – 55°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Serial Data Input A to Shift Clock (Figure 5)	2.0 3.0 4.5 6.0	50 40 10 9.0	65 50 13 11	75 60 15 13	ns
t_{su}	Minimum Setup Time, Shift Clock to Latch Clock (Figure 6)	2.0 3.0 4.5 6.0	75 60 15 13	95 70 19 16	110 80 22 19	ns
t_h	Minimum Hold Time, Shift Clock to Serial Data Input A (Figure 5)	2.0 3.0 4.5 6.0	5.0 5.0 5.0 5.0	5.0 5.0 5.0 5.0	5.0 5.0 5.0 5.0	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 2)	2.0 3.0 4.5 6.0	50 40 10 9.0	65 50 13 11	75 60 15 13	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 3.0 4.5 6.0	60 45 12 10	75 60 15 13	90 70 18 15	ns
t_w	Minimum Pulse Width, Shift Clock (Figure 1)	2.0 3.0 4.5 6.0	50 40 10 9.0	65 50 13 11	75 60 15 13	ns
t_w	Minimum Pulse Width, Latch Clock (Figure 6)	2.0 3.0 4.5 6.0	50 40 10 9.0	65 50 13 11	75 60 15 13	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

FUNCTION TABLE

Operation	Inputs					Resulting Function			
	Reset	Serial Input A	Shift Clock	Latch Clock	Output Enable	Shift Register Contents	Latch Register Contents	Serial Output SQ_H	Parallel Outputs $Q_A - Q_H$
Reset shift register	L	X	X	L, H, ↓	L	L	U	L	U
Shift data into shift register	H	D	↑	L, H, ↓	L	D SR_A; SR_N SR_{N+1}	U	SR_G SR_H	U
Shift register remains unchanged	H	X	L, H, ↓	L, H, ↓	L	U	U	U	U
Transfer shift register contents to latch register	H	X	L, H, ↓	↑	L	U	SR_N LR_N	U	SR_N
Latch register remains unchanged	X	X	X	L, H, ↓	L	*	U	*	U
Enable parallel outputs	X	X	X	X	L	*	**	*	Enabled
Force outputs into high impedance state	X	X	X	X	H	*	**	*	Z

SR = shift register contents
LR = latch register contents
D = data (L, H) logic level
U = remains unchanged
↑ = Low–to–High
↓ = High–to–Low
* = depends on Reset and Shift Clock inputs
** = depends on Latch Clock input

PIN DESCRIPTIONS

INPUTS

A (Pin 14)

Serial Data Input. The data on this pin is shifted into the 8–bit serial shift register.

CONTROL INPUTS

Shift Clock (Pin 11)

Shift Register Clock Input. A low– to–high transition on this input causes the data at the Serial Input pin to be shifted into the 8–bit shift register.

Reset (Pin 10)

Active–low, Asynchronous, Shift Register Reset Input. A low on this pin resets the shift register portion of this device only. The 8–bit latch is not affected.

Latch Clock (Pin 12)

Storage Latch Clock Input. A low–to–high transition on this input latches the shift register data.

Output Enable (Pin 13)

Active–low Output Enable. A low on this input allows the data from the latches to be presented at the outputs. A high on this input forces the outputs (Q_A–Q_H) into the high–impedance state. The serial output is not affected by this control unit.

OUTPUTS

$Q_A - Q_H$ (Pins 15, 1, 2, 3, 4, 5, 6, 7)

Noninverted, 3–state, latch outputs.

SQ_H (Pin 9)

Noninverted, Serial Data Output. This is the output of the eighth stage of the 8–bit shift register. This output does not have three–state capability.

SWITCHING WAVEFORMS

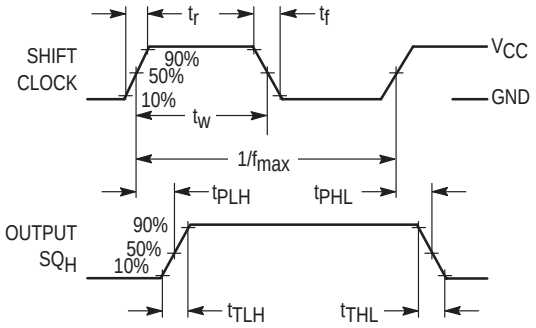


Figure 1.

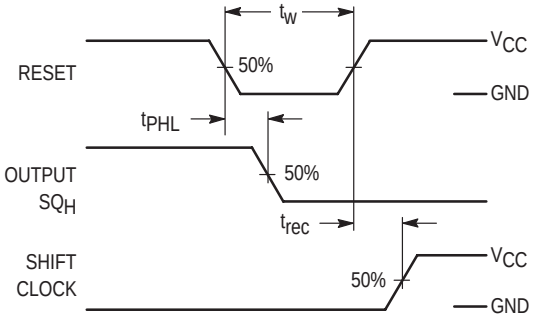


Figure 2.

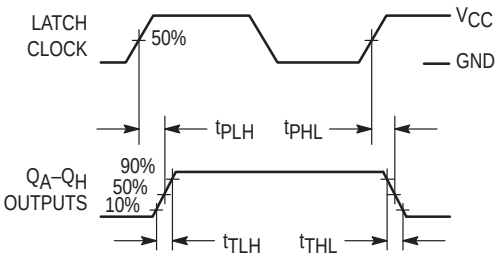


Figure 3.

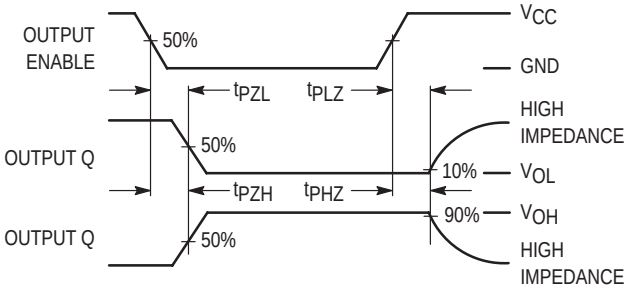


Figure 4.

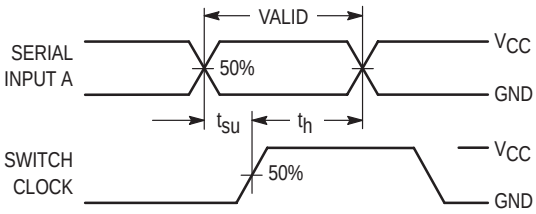


Figure 5.

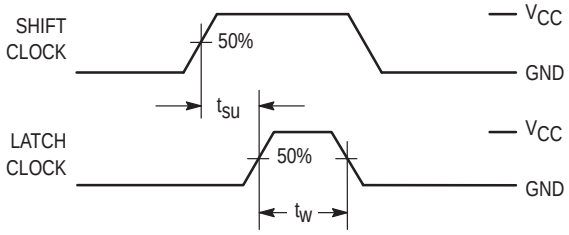
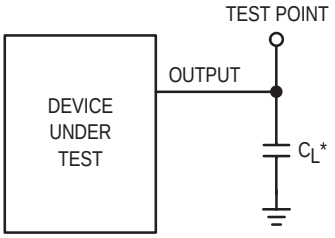


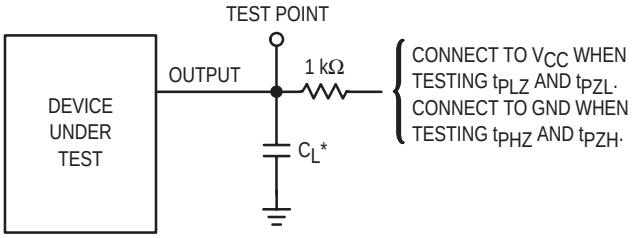
Figure 6.

TEST CIRCUITS



*Includes all probe and jig capacitance

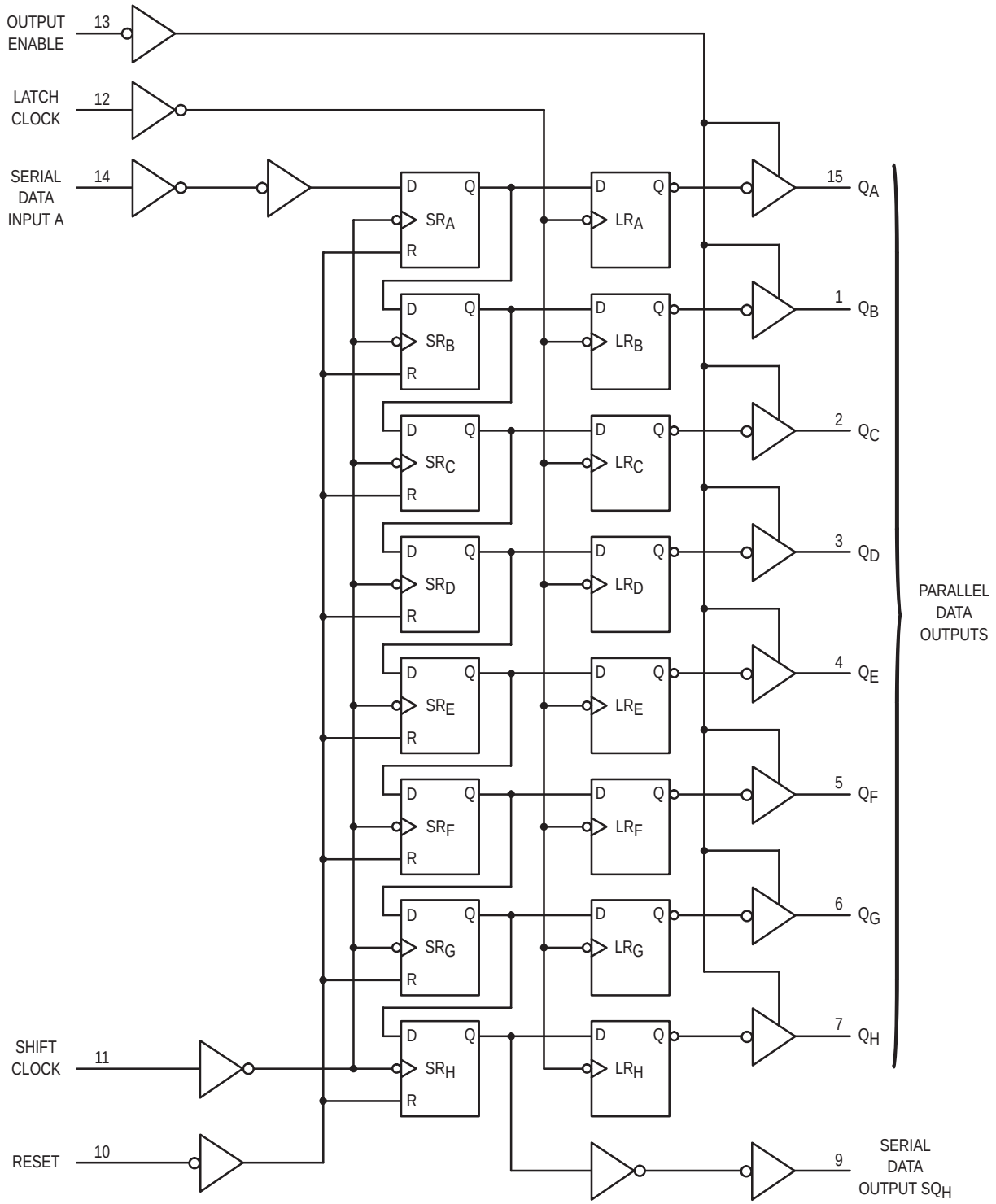
Figure 7.



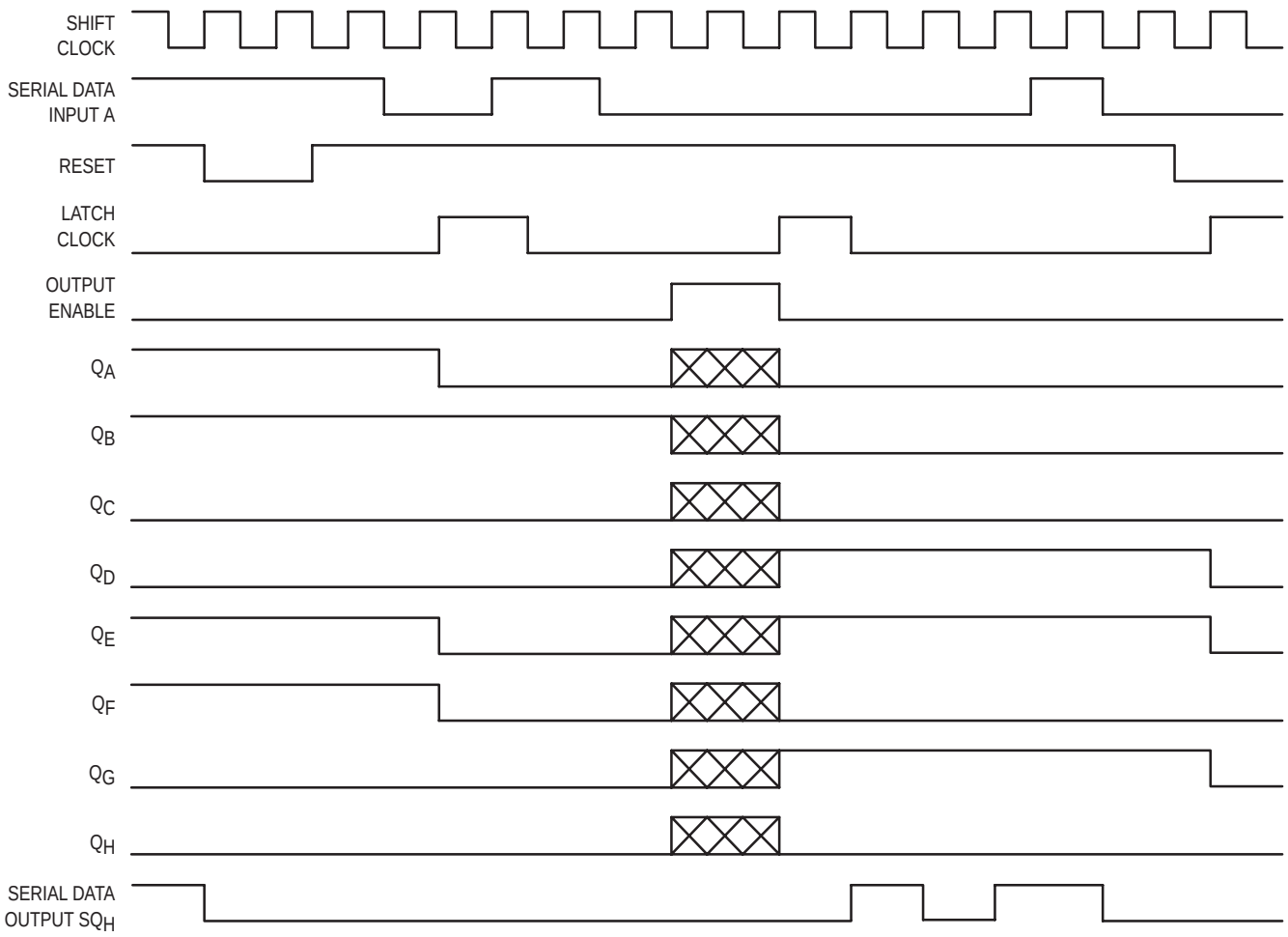
*Includes all probe and jig capacitance

Figure 8.

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM



NOTE: ⊠ implies that the output is in a high–impedance state.

MC74HC4020A

14-Stage Binary Ripple Counter

High–Performance Silicon–Gate CMOS

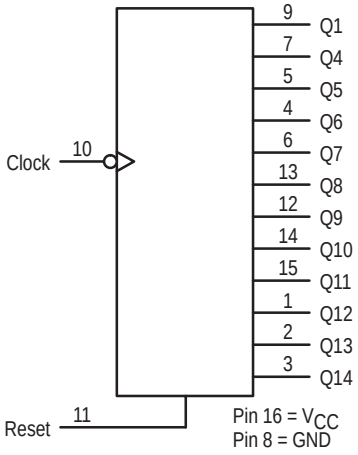
The MC74C4020A is identical in pinout to the standard CMOS MC14020B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

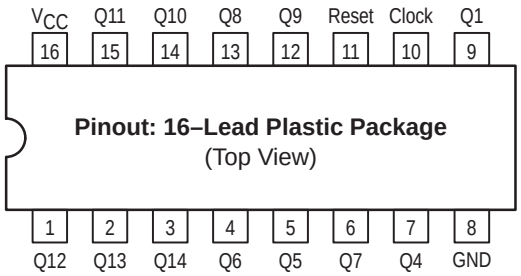
This device consists of 14 master–slave flip–flops with 12 stages brought out to pins. The output of each flip–flop feeds the next and the frequency at each output is half of that of the preceding one. Reset is asynchronous and active–high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the HC4020A for some designs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With JEDEC Standard No. 7A Requirements
- Chip Complexity: 398 FETs or 99.5 Equivalent Gates

LOGIC DIAGRAM





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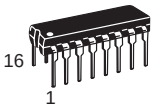
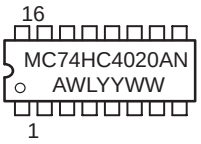
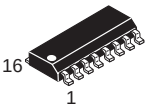
MARKING DIAGRAMS

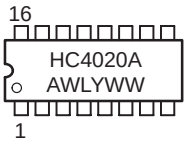


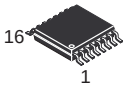
PDIP–16
N SUFFIX
CASE 648



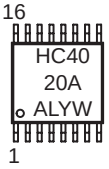


SO–16
D SUFFIX
CASE 751B





TSSOP–16
DT SUFFIX
CASE 948F



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

FUNCTION TABLE

Clock	Reset	Output State
⌐‾	L	No Charge
‾⌐	L	Advance to Next State
X	H	All Outputs Are Low

ORDERING INFORMATION

Device	Package	Shipping
MC74HC4020AN	PDIP–16	2000 / Box
MC74HC4020AD	SOIC–16	48 / Rail
MC74HC4020ADR2	SOIC–16	2500 / Reel
MC74HC4020ADT	TSSOP–16	96 / Rail
MC74HC4020ADTR2	TSSOP–16	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature Range, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise/Fall Time (Figure 1) V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit –55 to 25°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1V or V_{CC} –0.1V $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1V or V_{CC} – 0.1V $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} =V_{IH} or V_{IL} $\|I_{out}\| \le 2.4mA$ $\|I_{out}\| \le 4.0mA$ $\|I_{out}\| \le 5.2mA$	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 2.4mA$ $\|I_{out}\| \le 4.0mA$ $\|I_{out}\| \le 5.2mA$	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 3.0 4.5 6.0	10 15 30 50	9.0 14 28 50	8.0 12 25 40	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q1* (Figures 1 and 4)	2.0 3.0 4.5 6.0	96 63 31 25	106 71 36 30	115 88 40 35	ns
t_{PHL}	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 4)	2.0 3.0 4.5 6.0	45 30 30 26	52 36 35 32	65 40 40 35	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Qn to Qn+1 (Figures 3 and 4)	2.0 3.0 4.5 6.0	69 40 17 14	80 45 21 15	90 50 28 22	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 15	110 36 22 19	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

* For T_A = 25°C and C_L = 50 pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:

V_{CC} = 2.0 V: t_P = [93.7 + 59.3 (n–1)] ns
V_{CC} = 3.0 V: t_P = [61.5 + 34.4 (n–1)] ns
V_{CC} = 4.5 V: t_P = [30.25 + 14.6 (n–1)] ns
V_{CC} = 6.0 V: t_P = [24.4 + 12 (n–1)] ns

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package)*	38	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 3.0 4.5 6.0	30 20 5 4	40 25 8 6	50 30 12 9	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 3.0 4.5 6.0	70 40 15 13	80 45 19 16	90 50 24 20	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 3.0 4.5 6.0	70 40 15 13	80 45 19 16	90 50 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

PIN DESCRIPTIONS

INPUTS

Clock (Pin 10)

Negative–edge triggering clock input. A high–to–low transition on this input advances the state of the counter.

Reset (Pin 11)

Active–high reset. A high level applied to this input asynchronously resets the counter to its zero state, thus forcing all Q outputs low.

OUTPUTS

Q1, Q4—Q14 (Pins 9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3)

Active–high outputs. Each Qn output divides the Clock input frequency by 2^N.

SWITCHING WAVEFORMS

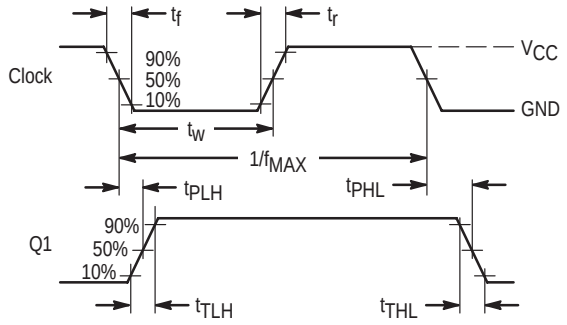


Figure 1.

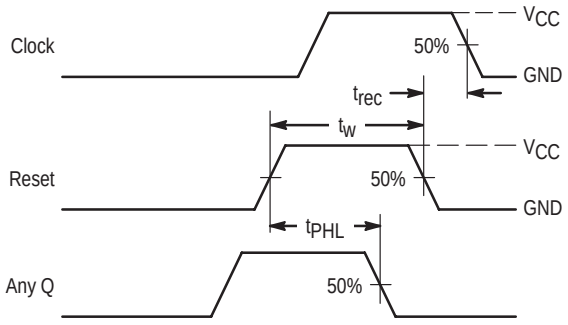


Figure 2.

SWITCHING WAVEFORMS (continued)

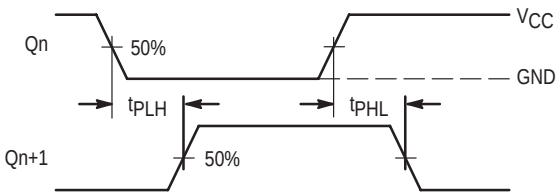
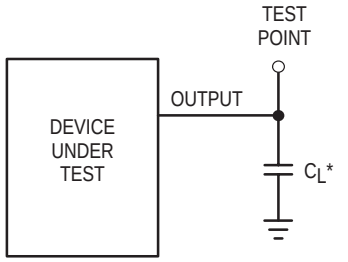


Figure 3.



*Includes all probe and jig capacitance

Figure 4. Test Circuit

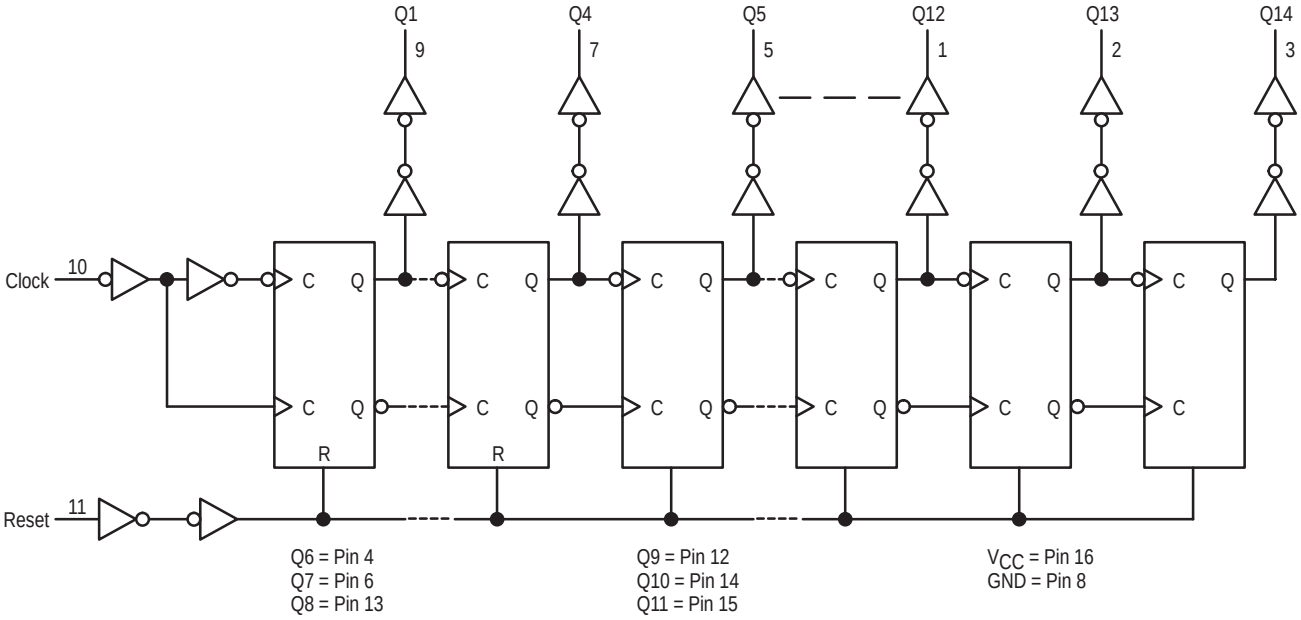


Figure 5. Expanded Logic Diagram

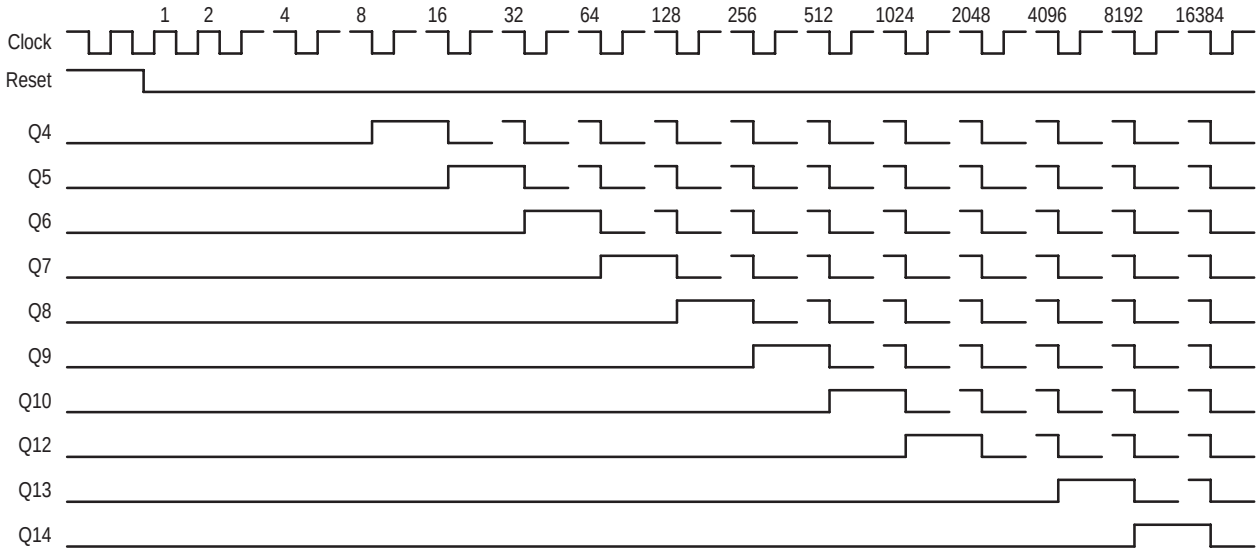


Figure 6. Timing Diagram

APPLICATIONS INFORMATION

Time–Base Generator

A 60Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the input of the MC54/74HC14A, Schmitt-trigger inverter. The HC14A squares–up the input waveform and feeds the HC4020A. Selecting outputs Q5, Q10, Q11, and Q12 causes a reset every 3600 clocks. The HC20 decodes the counter outputs, produces a single (narrow) output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.

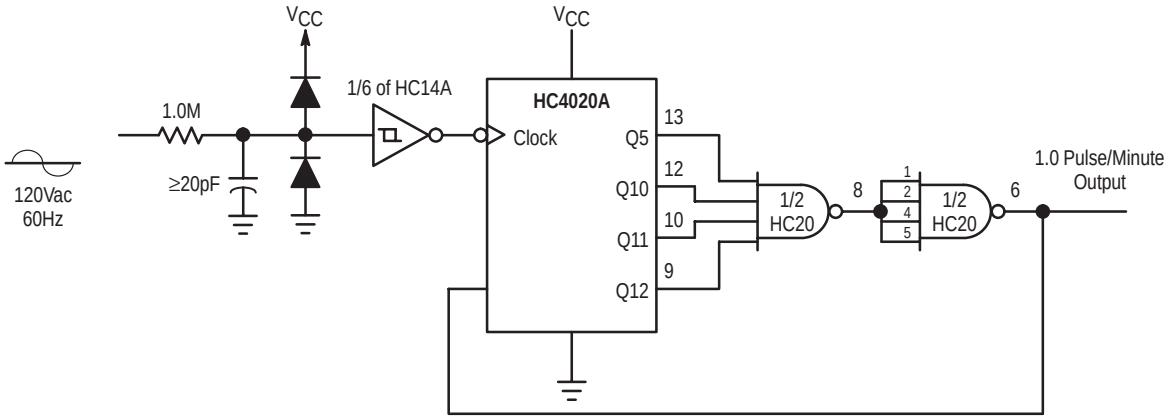


Figure 7. Time–Base Generator

MC74HC4040A

12-Stage Binary Ripple Counter

High–Performance Silicon–Gate CMOS

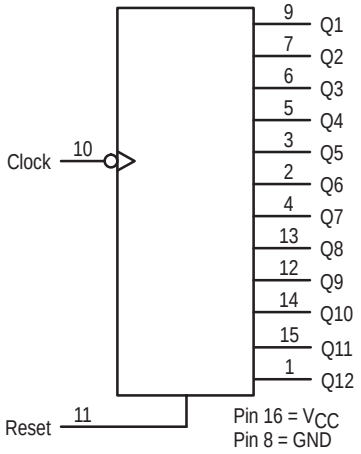
The MC74C4040A is identical in pinout to the standard CMOS MC14040. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

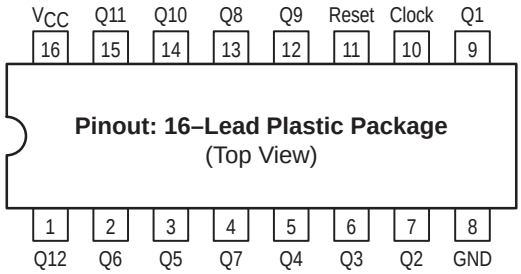
This device consists of 12 master–slave flip–flops. The output of each flip–flop feeds the next and the frequency at each output is half of that of the preceding one. The state counter advances on the negative–going edge of the Clock input. Reset is asynchronous and active–high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the HC4040A for some designs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With JEDEC Standard No. 7A Requirements
- Chip Complexity: 398 FETs or 99.5 Equivalent Gates

LOGIC DIAGRAM





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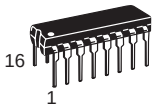
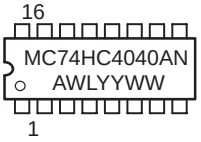
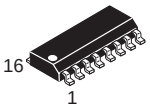
MARKING DIAGRAMS

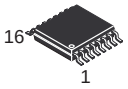


PDIP–16
N SUFFIX
CASE 648

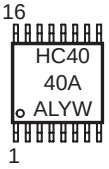




SO–16
D SUFFIX
CASE 751B



TSSOP–16
DT SUFFIX
CASE 948F



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

FUNCTION TABLE

Clock	Reset	Output State
⌐	L	No Charge
¬	L	Advance to Next State
X	H	All Outputs Are Low

ORDERING INFORMATION

Device	Package	Shipping
MC74HC4040AN	PDIP–16	2000 / Box
MC74HC4040AD	SOIC–16	48 / Rail
MC74HC4040ADR2	SOIC–16	2500 / Reel
MC74HC4040ADT	TSSOP–16	96 / Rail
MC74HC4040ADTR2	TSSOP–16	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature Range, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1) V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit –55 to 25°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1V or V_{CC} –0.1V $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1V or V_{CC} – 0.1V $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} =V_{IH} or V_{IL} $\|I_{out}\| \le 2.4mA$ $\|I_{out}\| \le 4.0mA$ $\|I_{out}\| \le 5.2mA$	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 2.4$mA	3.0	0.26	0.33	0.40	
		$\|I_{out}\| \le 4.0$mA	4.5	0.26	0.33	0.40	
		$\|I_{out}\| \le 5.2$mA	6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	10	9.0	8.0	MHz
		3.0	15	14	12	
		4.5	30	28	25	
		6.0	50	45	40	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q1* (Figures 1 and 4)	2.0	96	106	115	ns
		3.0	63	71	88	
		4.5	31	36	40	
		6.0	25	30	35	
t_{PHL}	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 4)	2.0	45	52	65	ns
		3.0	30	36	40	
		4.5	30	35	40	
		6.0	26	32	35	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Qn to Qn+1 (Figures 3 and 4)	2.0	69	80	90	ns
		3.0	40	45	50	
		4.5	17	21	28	
		6.0	14	15	22	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	15	19	
C_{in}	Maximum Input Capacitance		10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

* For T_A = 25°C and C_L = 50 pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:

V_{CC} = 2.0 V: t_P = [93.7 + 59.3 (n–1)] ns V_{CC} = 4.5 V: t_P = [30.25 + 14.6 (n–1)] ns

V_{CC} = 3.0 V: t_P = [61.5 + 34.4 (n–1)] ns V_{CC} = 6.0V: t_P = [24.4 + 12 (n–1)] ns

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package)*	31	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 3.0 4.5 6.0	30 20 5 4	40 25 8 6	50 30 12 9	ns
t_W	Minimum Pulse Width, Clock (Figure 1)	2.0 3.0 4.5 6.0	70 40 15 13	80 45 19 16	90 50 24 20	ns
t_W	Minimum Pulse Width, Reset (Figure 2)	2.0 3.0 4.5 6.0	70 40 15 13	80 45 19 16	90 50 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

PIN DESCRIPTIONS

INPUTS

Clock (Pin 10)

Negative–edge triggering clock input. A high–to–low transition on this input advances the state of the counter.

Reset (Pin 11)

Active–high reset. A high level applied to this input asynchronously resets the counter to its zero state, thus forcing all Q outputs low.

OUTPUTS

Q1 thru Q12 (Pins 9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1)

Active–high outputs. Each Qn output divides the Clock input frequency by 2^N.

SWITCHING WAVEFORMS

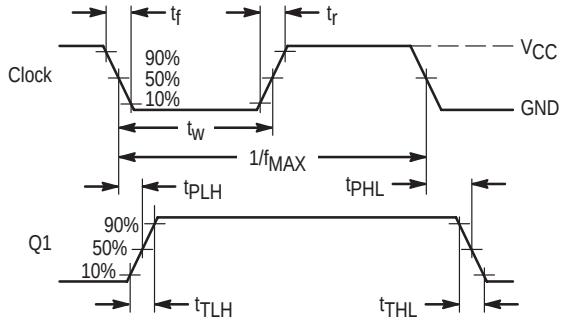


Figure 1.

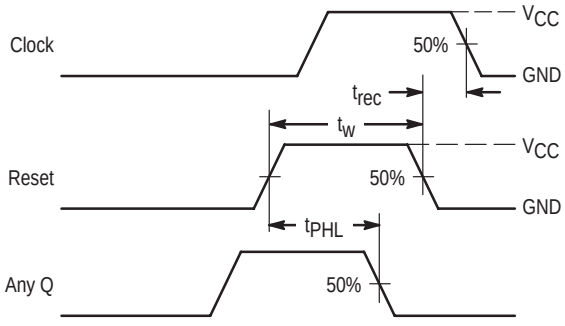


Figure 2.

SWITCHING WAVEFORMS (continued)

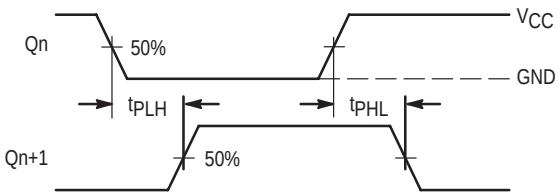
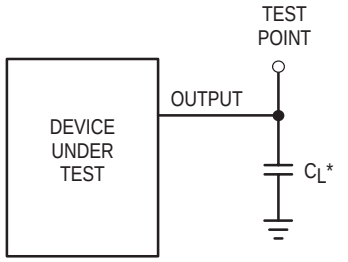


Figure 3.



*Includes all probe and jig capacitance

Figure 4. Test Circuit

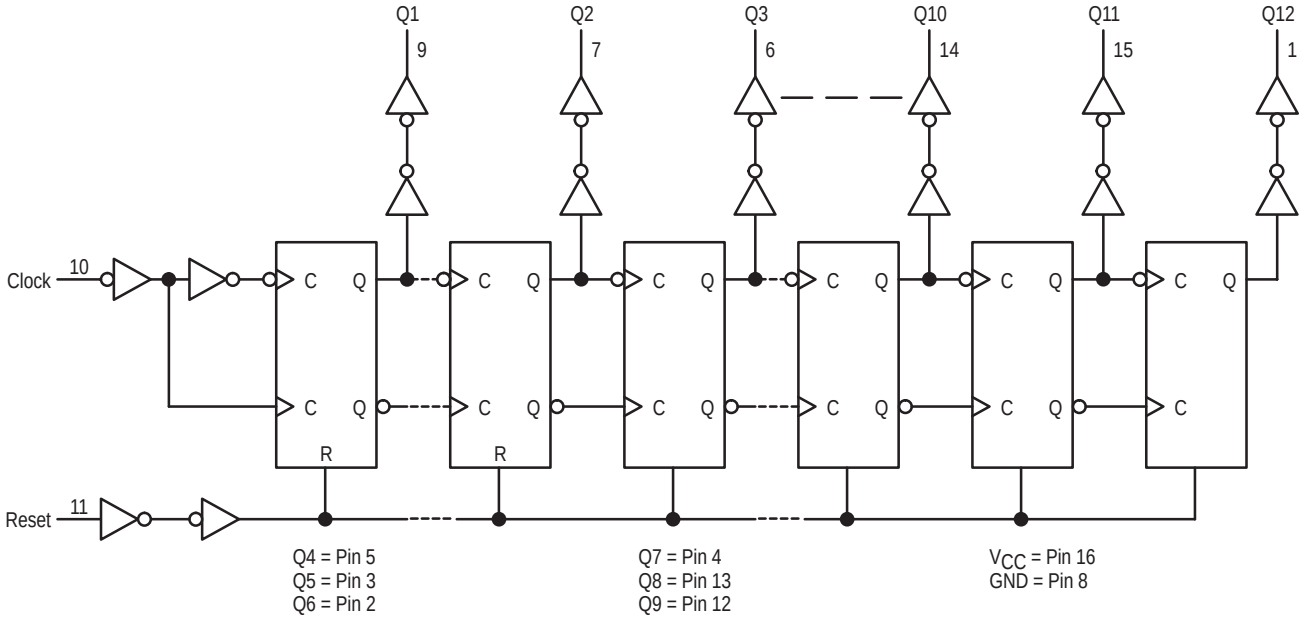


Figure 5. Expanded Logic Diagram

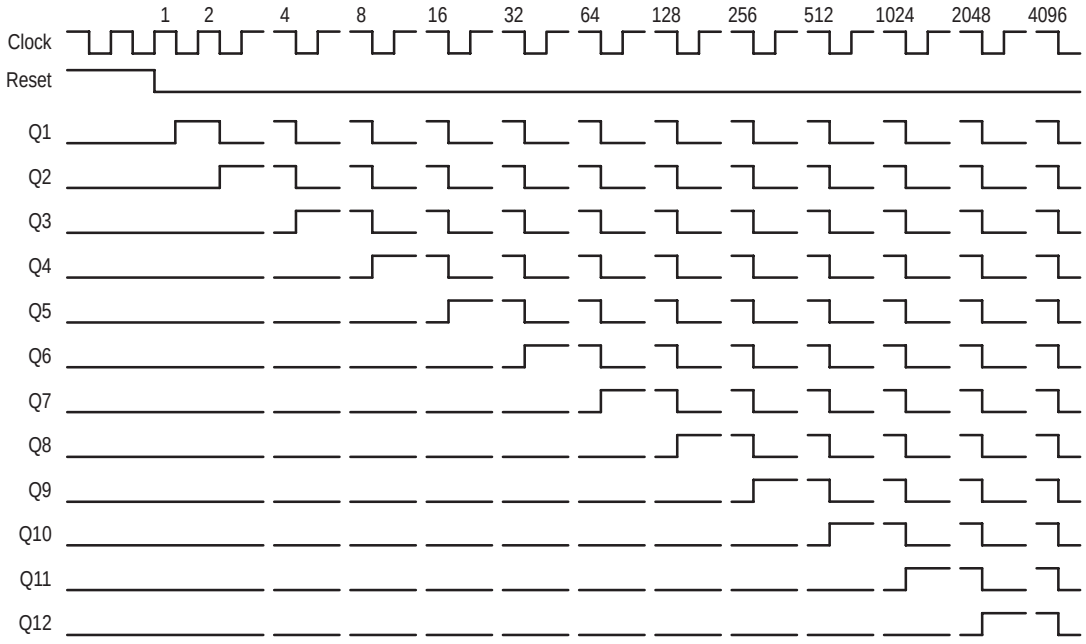


Figure 6. Timing Diagram

APPLICATIONS INFORMATION

Time–Base Generator

A 60Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the input of the MC54/74HC14A, Schmitt-trigger inverter. The HC14A squares–up the input waveform and feeds the HC4040A. Selecting outputs Q5, Q10, Q11, and Q12 causes a reset every 3600 clocks. The HC20 decodes the counter outputs, produces a single (narrow) output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.

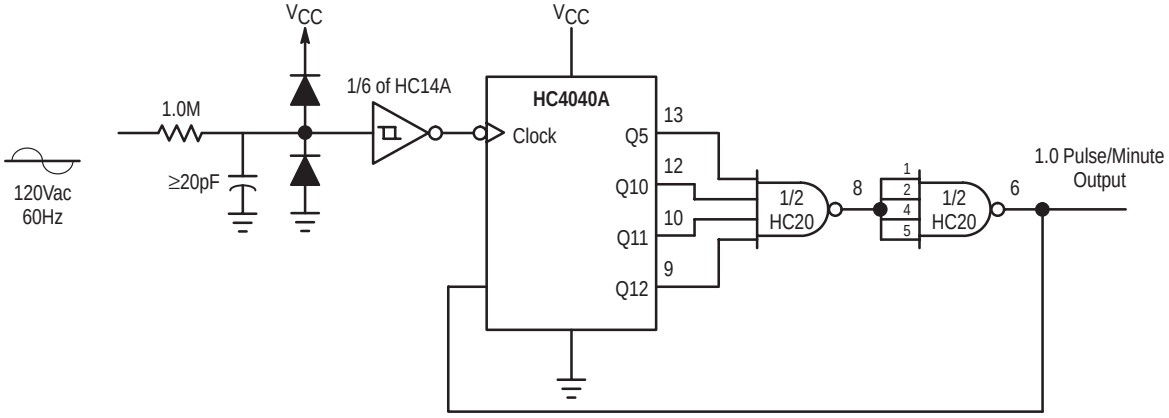


Figure 7. Time–Base Generator

MC74HC4046A

Phase-Locked Loop
High–Performance Silicon–Gate CMOS

The MC74HC4046A is similar in function to the MC14046 Metal gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC4046A phase–locked loop contains three phase comparators, a voltage–controlled oscillator (VCO) and unity gain op–amp DEM_{OUT}. The comparators have two common signal inputs, $COMP_{IN}$, and SIG_{IN}. Input SIG_{IN} and $COMP_{IN}$ can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor to small voltage signals). The self–bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal $PC1_{OUT}$ and maintains 90 degrees phase shift at the center frequency between SIG_{IN} and $COMP_{IN}$ signals (both at 50% duty cycle). Phase comparator 2 (with leading–edge sensing logic) provides digital error signals $PC2_{OUT}$ and PCP_{OUT} and maintains a 0 degree phase shift between SIG_{IN} and $COMP_{IN}$ signals (duty cycle is immaterial). The linear VCO produces an output signal VCO_{OUT} whose frequency is determined by the voltage of input VCO_{IN} signal and the capacitor and resistors connected to pins C1A, C1B, R1 and R2. The unity gain op–amp output DEM_{OUT} with an external resistor is used where the VCO_{IN} signal is needed but no loading can be tolerated. The inhibit input, when high, disables the VCO and all op–amps to minimize standby power consumption.

Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage–to–frequency conversion and motor speed control.

- Output Drive Capability: 10 LSTTL Loads
- Low Power Consumption Characteristic of CMOS Devices
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 3.0 to 6.0 V
- Low Input Current: 1.0 μA Maximum (except SIG_{IN} and $COMP_{IN}$)
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Low Quiescent Current: 80 μA Maximum (VCO disabled)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on all Inputs
- Chip Complexity: 279 FETs or 70 Equivalent Gates

ON Semiconductor

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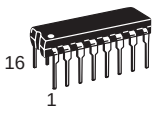
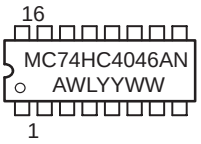
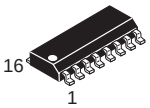
MARKING DIAGRAMS

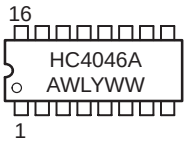


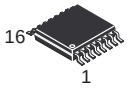
PDIP–16
N SUFFIX
CASE 648



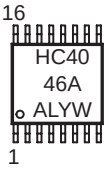


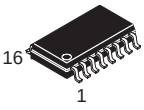
SO–16
D SUFFIX
CASE 751B





TSSOP–16
DT SUFFIX
CASE 948F





SOEIAJ–16
F SUFFIX
CASE 966

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

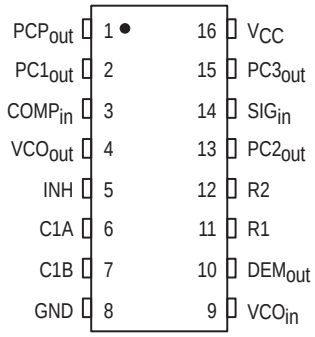
ORDERING INFORMATION

Device	Package	Shipping
MC74HC4046AN	PDIP–16	2000 / Box
MC74HC4046AD	SOIC–16	48 / Rail
MC74HC4046ADR2	SOIC–16	2500 / Reel
MC74HC4046AF	SOIC–EIAJ	See Note 1.
MC74HC4046AFEL	SOIC–EIAJ	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

Pin No.	Symbol	Name and Function
1	PCP_{OUT}	Phase Comparator Pulse Output
2	$PC1_{OUT}$	Phase Comparator 1 Output
3	$COMP_{IN}$	Comparator Input
4	VCO_{OUT}	VCO Output
5	INH	Inhibit Input
6	C1A	Capacitor C1 Connection A
7	C1B	Capacitor C1 Connection B
8	GND	Ground (0 V) V_{SS}
9	VCO_{IN}	VCO Input
10	DEM_{OUT}	Demodulator Output
11	R1	Resistor R1 Connection
12	R2	Resistor R2 Connection
13	$PC2_{OUT}$	Phase Comparator 2 Output
14	SIG_{IN}	Signal Input
15	$PC3_{OUT}$	Phase Comparator 3 Output
16	V_{CC}	Positive Supply Voltage

PIN ASSIGNMENT



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 1.5 to V_{CC} + 1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air Plastic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP and SOIC Package†	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		3.0	6.0	V
V_{CC}	DC Supply Voltage (Referenced to GND) NON–VCO		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Pin 5)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

[Phase Comparator Section]

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} Volts	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage DC Coupled SIG_{IN}, $COMP_{IN}$	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20$ μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage DC Coupled SIG_{IN}, $COMP_{IN}$	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20$ μA	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage PCP_{OUT}, PCn_{OUT}	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	 4.5 6.0	 3.98 5.48	 3.84 5.34	 3.7 5.2	

(continued)

[Phase Comparator Section]

DC ELECTRICAL CHARACTERISTICS – continued (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} Volts	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{OL}	Maximum Low–Level Output Voltage Qa–Qh PCP_{OUT}, PCn_{OUT}	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	 4.5 6.0	 0.26 0.26	 0.33 0.33	 0.4 0.4	
I_{in}	Maximum Input Leakage Current SIG_{IN}, $COMP_{IN}$	V_{in} = V_{CC} or GND	2.0 3.0 4.5 6.0	± 3.0 ± 7.0 ± 18.0 ± 30.0	± 4.0 ± 9.0 ± 23.0 ± 38.0	± 5.0 ± 11.0 ± 27.0 ± 45.0	μA
I_{OZ}	Maximum Three–State Leakage Current $PC2_{OUT}$	Output in High–Impedance State V_{in} = V_{IH} or V_{IL} V_{out} = V_{CC} or GND	6.0	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package) (VCO disabled) Pins 3, 5 and 14 at V_{CC} Pin 9 at GND; Input Leakage at Pins 3 and 14 to be excluded	V_{in} = V_{CC} or GND $\|I_{out}\|$ = 0 μA	6.0	4.0	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

[Phase Comparator Section]

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6.0 ns)

Symbol	Parameter	V_{CC} Volts	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, SIG_{IN}/$COMP_{IN}$ to $PC1_{OUT}$ (Figure 1)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, SIG_{IN}/$COMP_{IN}$ to PCP_{OUT} (Figure 1)	2.0 4.5 6.0	340 68 58	425 85 72	510 102 87	ns

[Phase Comparator Section]

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

t_{PLH}, t_{PHL}	Maximum Propagation Delay, $SIG_{IN}/COMP_{IN}$ to $PC3_{OUT}$ (Figure 1)	2.0 4.5 6.0	270 54 46	340 68 58	405 81 69	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, $SIG_{IN}/COMP_{IN}$ Output Disable Time to $PC2_{OUT}$ (Figures 2 and 3)	2.0 4.5 6.0	200 40 34	250 50 43	300 60 51	ns
t_{PZH}, t_{PZL}	Maximum Propagation Delay, $SIG_{IN}/COMP_{IN}$ Output Enable Time to $PC2_{OUT}$ (Figures 2 and 3)	2.0 4.5 6.0	230 46 39	290 58 49	345 69 59	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time (Figure 1)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns

[VCO Section]

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} Volts	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage INH	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20\ \mu A$	3.0 4.5 6.0	2.1 3.15 4.2	2.1 3.15 4.2	2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage INH	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20\ \mu A$	3.0 4.5 6.0	0.90 1.35 1.8	0.9 1.35 1.8	0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage VCO_{OUT}	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 20\ \mu A$	3.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.7 5.2	
V_{OL}	Maximum Low–Level Output Voltage VCO_{OUT}	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20\ \mu A$	3.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.4 0.4	
I_{in}	Maximum Input Leakage Current INH, VCO_{IN}	$V_{in} = V_{CC}$ or GND	6.0	0.1	1.0	1.0	μA
				Min **Max**	**Min** **Max**	**Min** **Max**	
$V_{VCO_{IN}}$	Operating Voltage Range at VCO_{IN} over the range specified for R1; For linearity see Fig. 15A, Parallel value of R1 and R2 should be > 2.7 kΩ	INH = V_{IL}	3.0 4.5 6.0	0.1 1.0 0.1 2.5 0.1 4.0	0.1 1.0 0.1 2.5 0.1 4.0	0.1 1.0 0.1 2.5 0.1 4.0	V
R1	Resistor Range		3.0 4.5 6.0	3.0 300 3.0 300 3.0 300	3.0 300 3.0 300 3.0 300	3.0 300 3.0 300 3.0 300	kΩ
R2			3.0 4.5 6.0	3.0 300 3.0 300 3.0 300	3.0 300 3.0 300 3.0 300	3.0 300 3.0 300 3.0 300	
C1	Capacitor Range		3.0 4.5 6.0	40 No Limit 40 40			pF

[VCO Section]

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} Volts	Guaranteed Limit						Unit
			– 55 to 25°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
Δf/T	Frequency Stability with Temperature Changes (Figure 13A, B, C)	3.0 4.5 6.0							%/K
fo	VCO Center Frequency (Duty Factor = 50%) (Figure 14A, B, C, D)	3.0 4.5 6.0	3 11 13						MHz
ΔfVCO	VCO Frequency Linearity	3.0 4.5 6.0	See Figures 15A, B, C						%
∂ VCO	Duty Factor at VCO_{OUT}	3.0 4.5 6.0	Typical 50%						%

[Demodulator Section]

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} Volts	Guaranteed Limit						Unit
				– 55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
RS	Resistor Range	At RS > 300 kΩ the Leakage Current can Influence $VDEM_{OUT}$	3.0 4.5 6.0	50 50 50	300 300 300					kΩ
V_{OFF}	Offset Voltage VCO_{IN} to $VDEM_{OUT}$	Vi = $VVCO_{IN}$ = 1/2 V_{CC}; Values taken over RS Range.	3.0 4.5 6.0	See Figure 12						mV
RD	Dynamic Output Resistance at DEM_{OUT}	$VDEM_{OUT}$ = 1/2 V_{CC}	3.0 4.5 6.0	Typical 25 Ω						Ω

SWITCHING WAVEFORMS

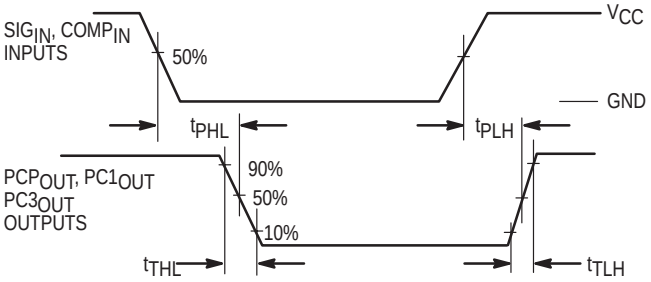


Figure 1.

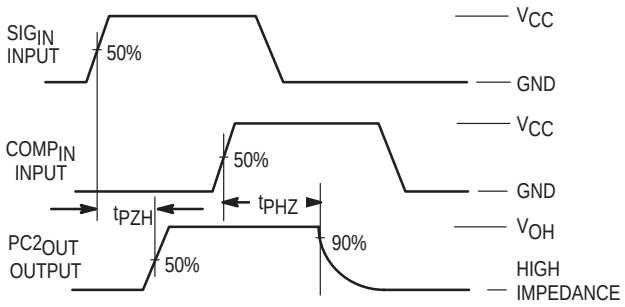


Figure 2.

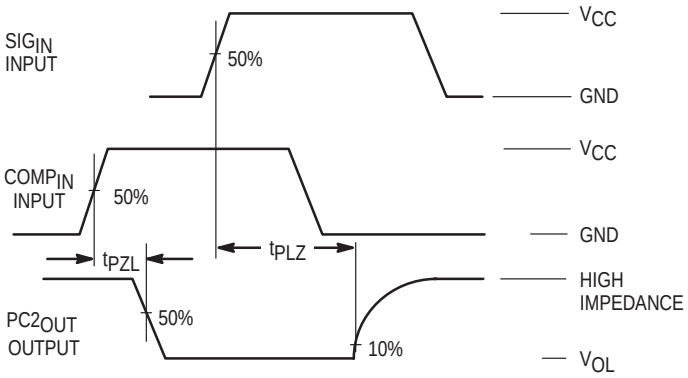


Figure 3.

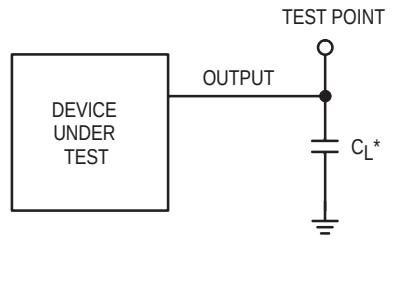


Figure 4. Test Circuit

DETAILED CIRCUIT DESCRIPTION

Voltage Controlled Oscillator/Demodulator Output

The VCO requires two or three external components to operate. These are R1, R2, C1. Resistor R1 and Capacitor C1 are selected to determine the center frequency of the VCO (see typical performance curves Figure 14). R2 can be used to set the offset frequency with 0 volts at VCO input. For example, if R2 is decreased, the offset frequency is increased. If R2 is omitted the VCO range is from 0 Hz. The effect of R2 is shown in Figure 24, typical performance curves. By increasing the value of R2 the lock range of the PLL is increased and the gain (volts/Hz) is decreased. Thus, for a narrow lock range, large swings on the VCO input will cause less frequency variation.

Internally, the resistors set a current in a current mirror, as shown in Figure 5. The mirrored current drives one side of the capacitor. Once the voltage across the capacitor charges up to V_{ref} of the comparators, the oscillator logic flips the capacitor which causes the mirror to charge the opposite side of the capacitor. The output from the internal logic is then taken to VCO output (Pin 4).

The input to the VCO is a very high impedance CMOS input and thus will not load down the loop filter, easing the filters design. In order to make signals at the VCO input accessible without degrading the loop performance, the VCO input voltage is buffered through a unity gain Op–amp to Demod Output. This Op–amp can drive loads of 50K ohms or more and provides no loading effects to the VCO input voltage (see Figure 12).

An inhibit input is provided to allow disabling of the VCO and all Op–amps (see Figure 5). This is useful if the internal VCO is not being used. A logic high on inhibit disables the VCO and all Op–amps, minimizing standby power consumption.

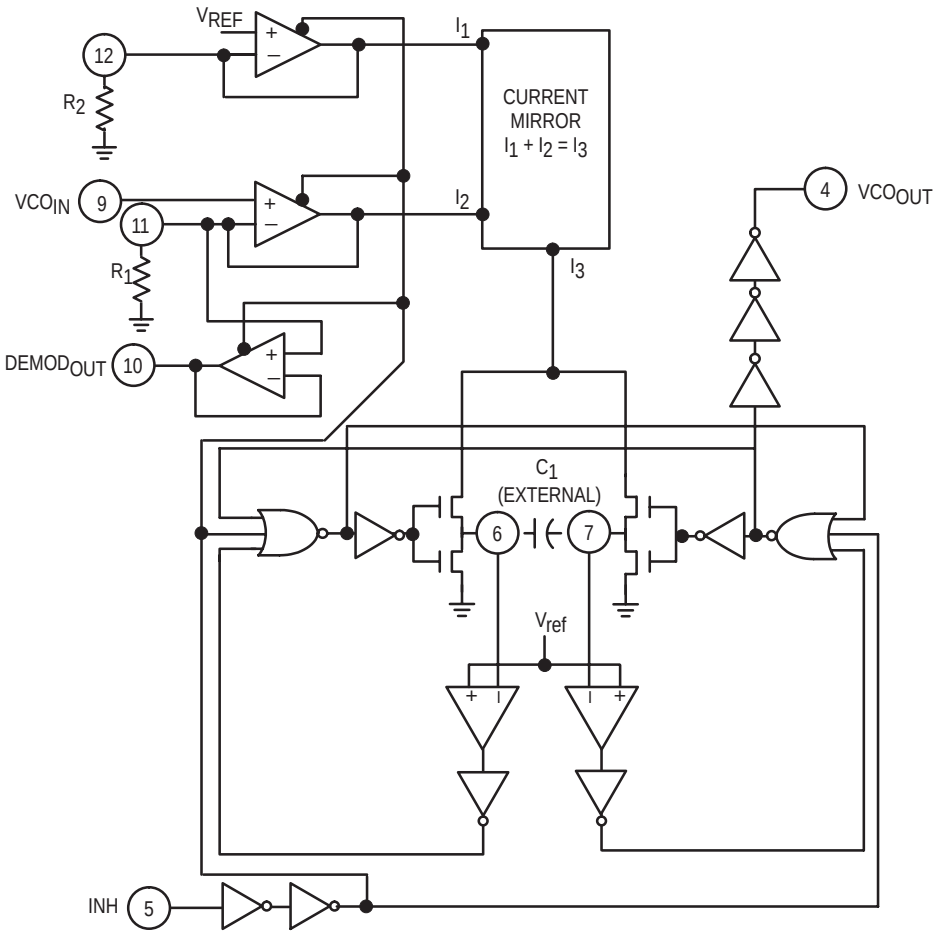


Figure 5. Logic Diagram for VCO

The output of the VCO is a standard high speed CMOS output with an equivalent LS–TTL fan out of 10. The VCO output is approximately a square wave. This output can either directly feed the $COMP_{IN}$ of the phase comparators or feed external prescalers (counters) to enable frequency synthesis.

Phase Comparators

All three phase comparators have two inputs, SIG_{IN} and $COMP_{IN}$. The SIG_{IN} and $COMP_{IN}$ have a special DC bias network that enables AC coupling of input signals. If the signals are not AC coupled, standard 74HC input levels are required. Both input structures are shown in Figure 6. The outputs of these comparators are essentially standard 74HC outputs (comparator 2 is TRI–STATEABLE). In normal operation V_{CC} and ground voltage levels are fed to the loop filter. This differs from some phase detectors which supply a current to the loop filter and should be considered in the design. (The MC14046 also provides a voltage).

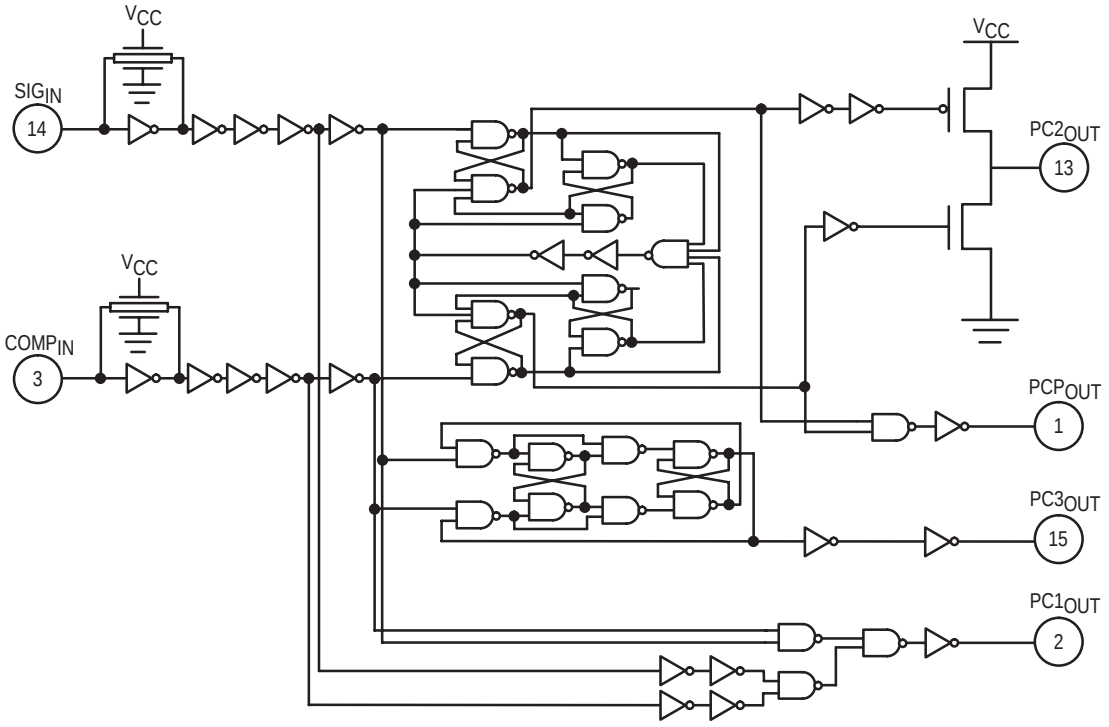


Figure 6. Logic Diagram for Phase Comparators

Phase Comparator 1

This comparator is a simple XOR gate similar to the 74HC86. Its operation is similar to an overdriven balanced modulator. To maximize lock range the input frequencies must have a 50% duty cycle. Typical input and output waveforms are shown in Figure 7. The output of the phase detector feeds the loop filter which averages the output voltage. The frequency range upon which the PLL will lock onto if initially out of lock is defined as the capture range. The capture range for phase detector 1 is dependent on the loop filter design. The capture range can be as large as the lock range, which is equal to the VCO frequency range.

To see how the detector operates, refer to Figure 7. When two square wave signals are applied to this comparator, an output waveform (whose duty cycle is dependent on the phase difference between the two signals) results. As the phase difference increases, the output duty cycle increases and the voltage after the loop filter increases. In order to achieve lock when the PLL input frequency increases, the VCO input voltage must increase and the phase difference between $COMP_{IN}$ and SIG_{IN} will increase. At an input frequency equal to f_{min}, the VCO input is at 0 V. This requires the phase detector output to be grounded; hence, the two input signals must be in phase. When the input frequency is f_{max}, the VCO input must be V_{CC} and the phase detector inputs must be 180 degrees out of phase.

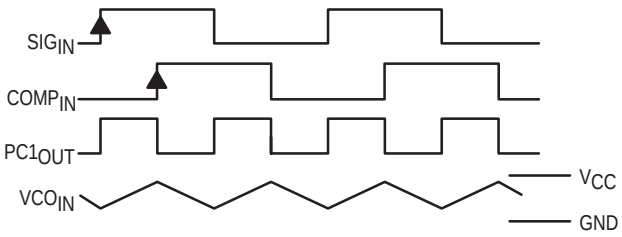


Figure 7. Typical Waveforms for PLL Using Phase Comparator 1

The XOR is more susceptible to locking onto harmonics of the SIG_{IN} than the digital phase detector 2. For instance, a signal 2 times the VCO frequency results in the same output duty cycle as a signal equal to the VCO frequency. The difference is that the output frequency of the 2f example is twice that of the other example. The loop filter and VCO range should be designed to prevent locking on to harmonics.

Phase Comparator 2

This detector is a digital memory network. It consists of four flip–flops and some gating logic, a three state output and a phase pulse output as shown in Figure 6. This comparator acts only on the positive edges of the input signals and is independent of duty cycle.

Phase comparator 2 operates in such a way as to force the PLL into lock with 0 phase difference between the VCO output and the signal input positive waveform edges. Figure 8 shows some typical loop waveforms. First assume that SIG_{IN} is leading the $COMP_{IN}$. This means that the VCO's frequency must be increased to bring its leading edge into proper phase alignment. Thus the phase detector 2 output is set high. This will cause the loop filter to charge up the VCO input, increasing the VCO frequency. Once the leading edge of the $COMP_{IN}$ is detected, the output goes TRI–STATE holding the VCO input at the loop filter voltage. If the VCO still lags the SIG_{IN} then the phase detector will again charge up the VCO input for the time between the leading edges of both waveforms.

If the VCO leads the SIG_{IN} then when the leading edge of the VCO is seen; the output of the phase comparator goes low. This discharges the loop filter until the leading edge of the SIG_{IN} is detected at which time the output disables itself again. This has the effect of slowing down the VCO to again make the rising edges of both waveforms coincidental.

When the PLL is out of lock, the VCO will be running either slower or faster than the SIG_{IN}. If it is running slower the phase detector will see more SIG_{IN} rising edges and so the output of the phase comparator will be high a majority of the time, raising the VCO's frequency. Conversely, if the VCO is running faster than the SIG_{IN}, the output of the detector will be low most of the time and the VCO's output frequency will be decreased.

As one can see, when the PLL is locked, the output of phase comparator 2 will be disabled except for minor corrections at the leading edge of the waveforms. When PC_2 is TRI–STATED, the PCP output is high. This output can be used to determine when the PLL is in the locked condition.

This detector has several interesting characteristics. Over the entire VCO frequency range there is no phase difference between the $COMP_{IN}$ and the SIG_{IN}. The lock range of the PLL is the same as the capture range. Minimal power was consumed in the loop filter since in lock the detector output is a high impedance. When no SIG_{IN} is present, the detector will see only VCO leading edges, so the comparator output will stay low, forcing the VCO to f_{min}.

Phase comparator 2 is more susceptible to noise, causing the PLL to unlock. If a noise pulse is seen on the SIG_{IN}, the comparator treats it as another positive edge of the SIG_{IN} and will cause the output to go high until the VCO leading edge is seen, potentially for an entire SIG_{IN} period. This would cause the VCO to speed up during that time. When using PC_1, the output of that phase detector would be disturbed for only the short duration of the noise spike and would cause less upset.

Phase Comparator 3

This is a positive edge–triggered sequential phase detector using an RS flip–flop as shown in Figure 6. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$
are not important. It has some similar characteristics to the edge sensitive comparator. To see how this detector works, assume input pulses are applied to the SIG_{IN} and $COMP_{IN}$'s as shown in Figure 9. When the SIG_{IN} leads the $COMP_{IN}$, the flop is set. This will charge the loop filter and cause the VCO to speed up, bringing the comparator into phase with the SIG_{IN}. The phase angle between SIG_{IN} and $COMP_{IN}$ varies from 0° to 360° and is 180° at f_o. The voltage swing for PC_3 is greater than for PC_2 but consequently has more ripple in the signal to the VCO. When no SIG_{IN} is present the VCO will be forced to f_{max} as opposed to f_{min} when PC_2 is used.

The operating characteristics of all three phase comparators should be compared to the requirements of the system design and the appropriate one should be used.

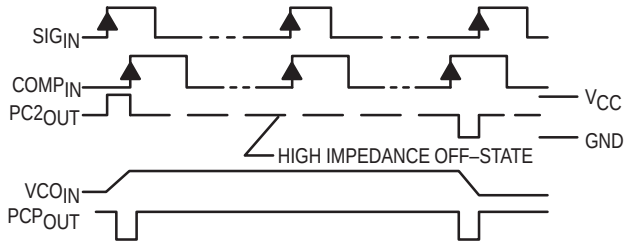


Figure 8. Typical Waveforms for PLL Using Phase Comparator 2

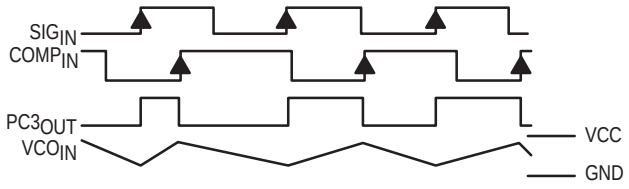


Figure 9. Typical Waveform for PLL Using Phase Comparator 3

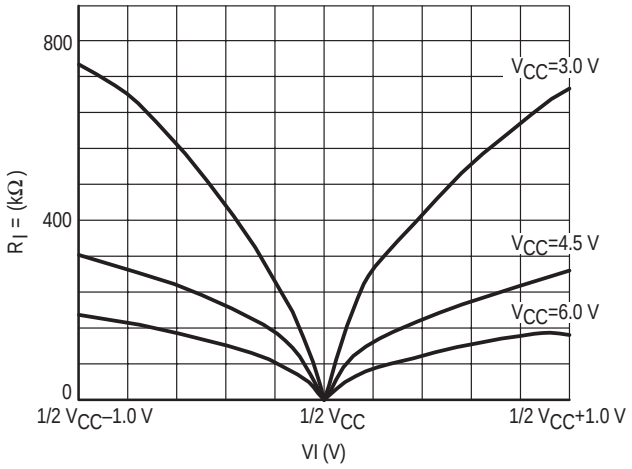


Figure 10. Input Resistance at SIG_{IN}, $COMP_{IN}$ with ΔV_I = 1.0 V at Self–Bias Point

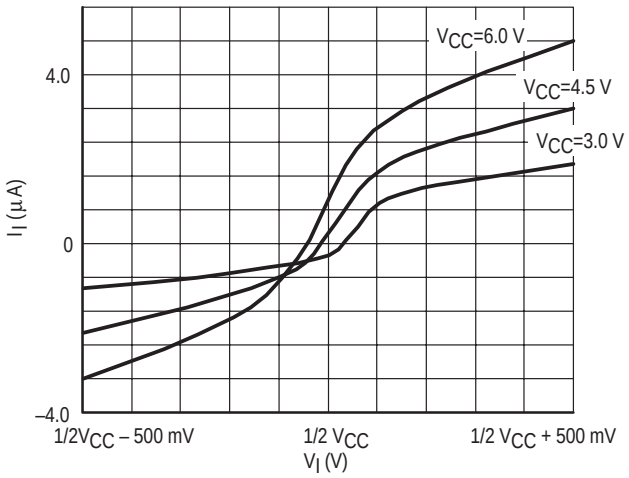


Figure 11. Input Current at SIG_{IN}, $COMP_{IN}$ with ΔV_I = 500 mV at Self–Bias Point

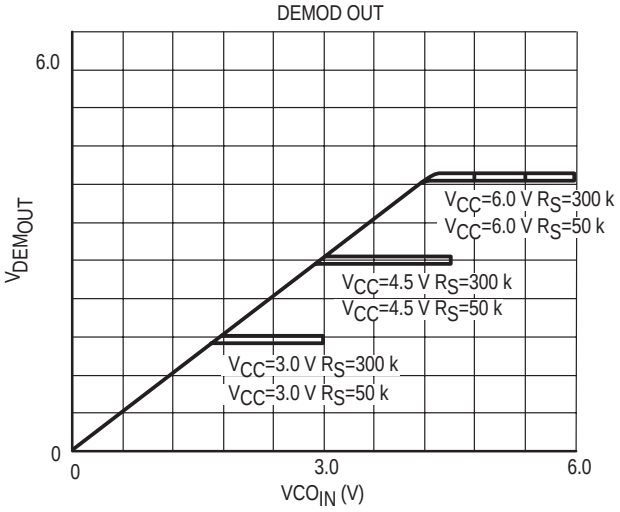


Figure 12. Offset Voltage at Demodulator Output as a Function of VCO_{IN} and R_S

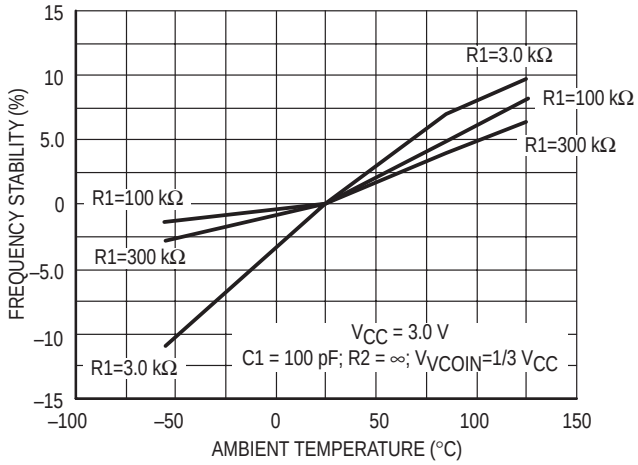


Figure 13A. Frequency Stability versus Ambient Temperature: V_{CC} = 3.0 V

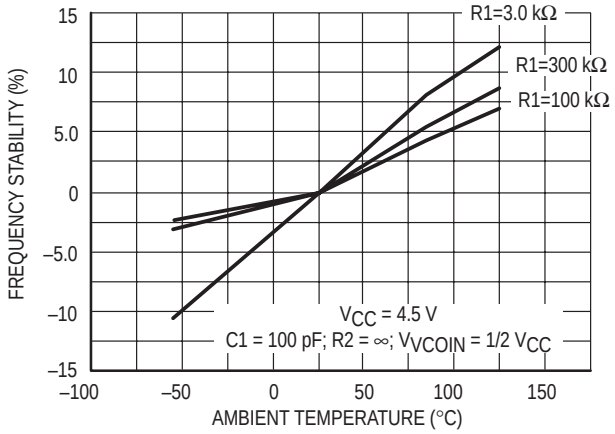


Figure 13B. Frequency Stability versus Ambient Temperature: V_{CC} = 4.5 V

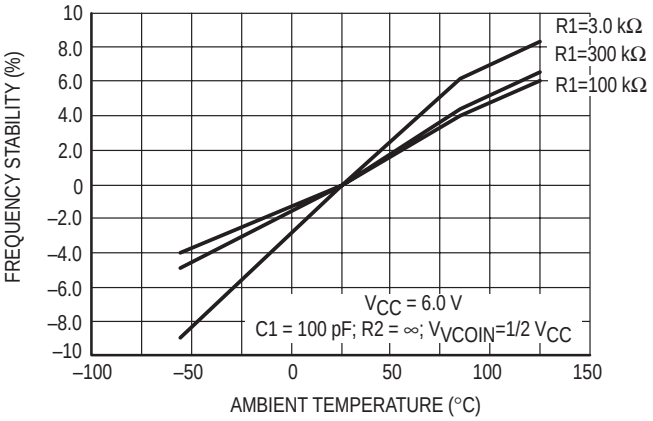


Figure 13C. Frequency Stability versus Ambient Temperature: V_{CC} = 6.0 V

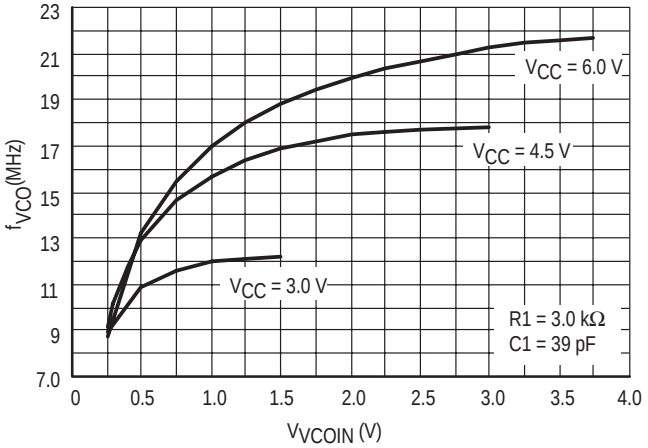


Figure 14A. VCO Frequency (f_{VCO}) as a Function of the VCO Input Voltage (V_{VCOIN})

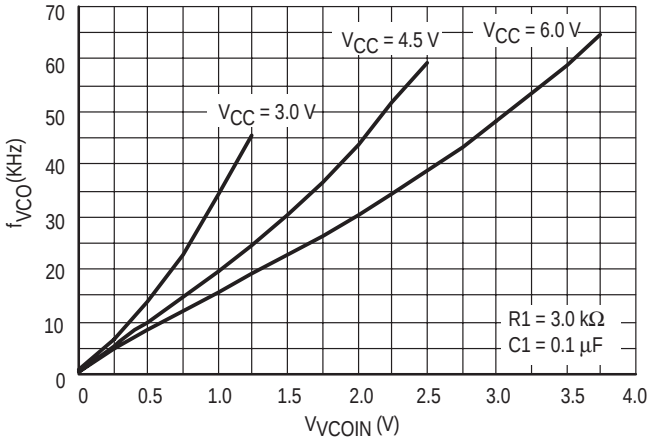


Figure 14B. VCO Frequency (f_{VCO}) as a Function of the VCO Input Voltage (V_{VCOIN})

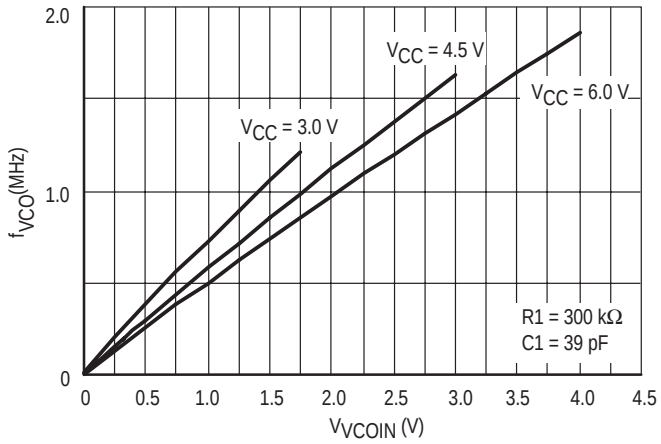


Figure 14C. VCO Frequency (f_{VCO}) as a Function of the VCO Input Voltage (V_{VCOIN})

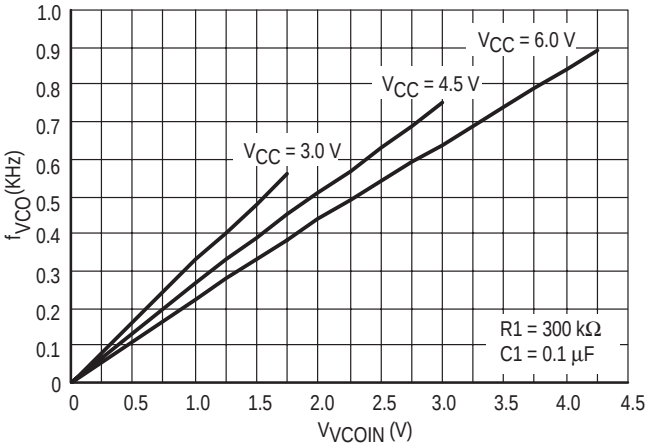


Figure 14D. VCO Frequency (f_{VCO}) as a Function of the VCO Input Voltage (V_{VCOIN})

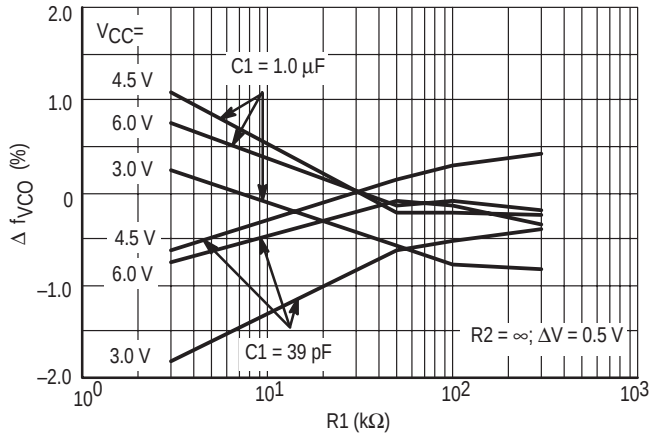
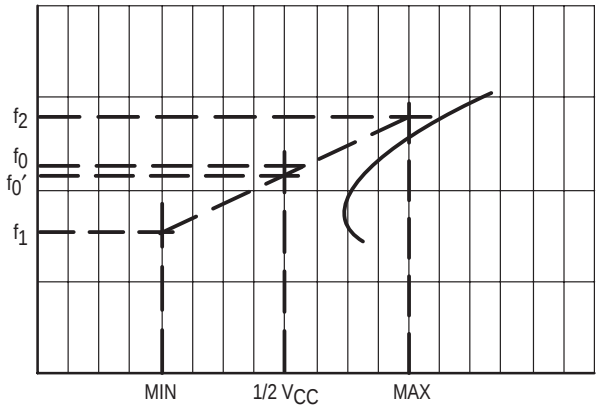


Figure 15A. Frequency Linearity versus R1, C1 and V_{CC}



ΔV = 0.5 V OVER THE V_{CC} RANGE: FOR VCO LINEARITY

$f_0' = (f_1 + f_2) / 2$

LINEARITY = $(f_0' - f_0) / f_0'$ x 100%

Figure 15B. Definition of VCO Frequency Linearity

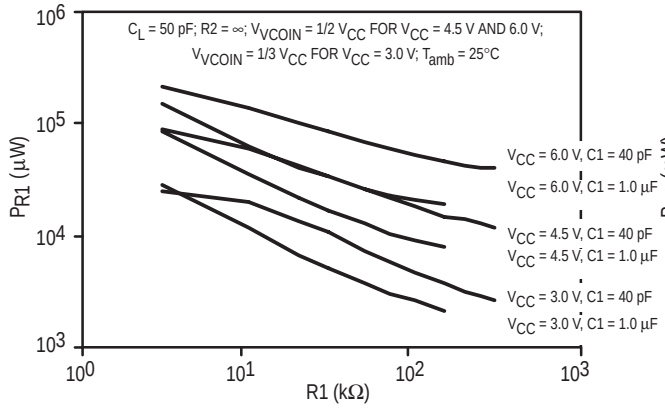


Figure 16. Power Dissipation versus R1

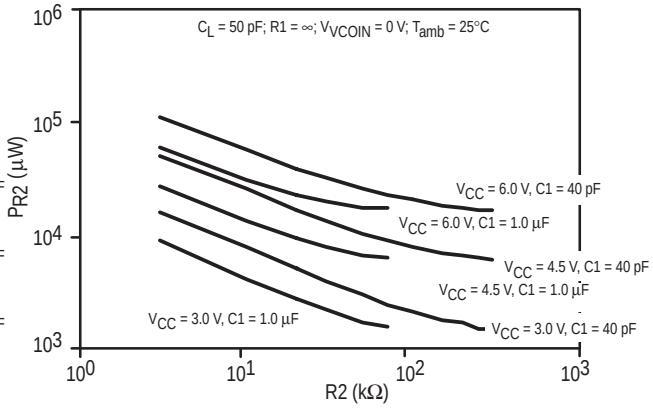


Figure 17. Power Dissipation versus R2

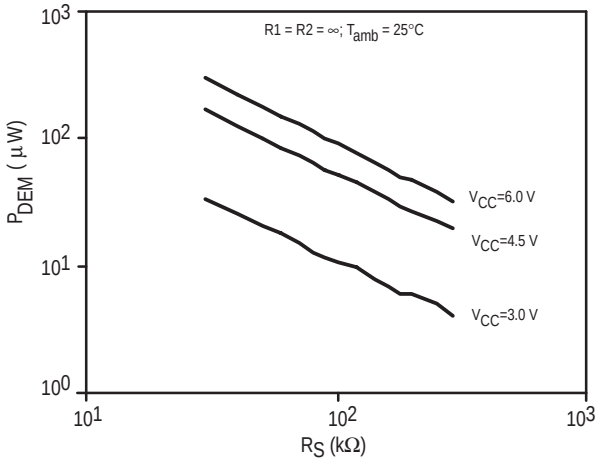


Figure 18. DC Power Dissipation of Demodulator versus R_S

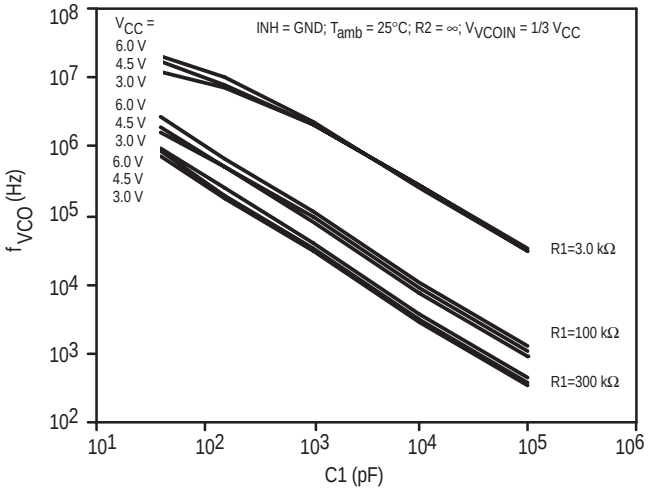


Figure 19. VCO Center Frequency versus C1

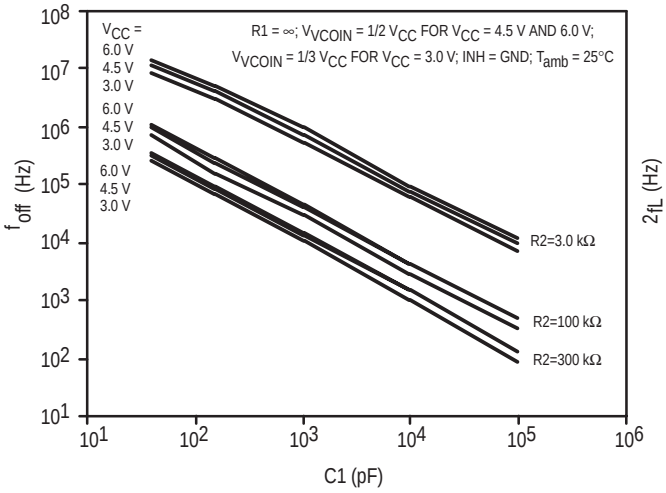


Figure 20. Frequency Offset versus C1

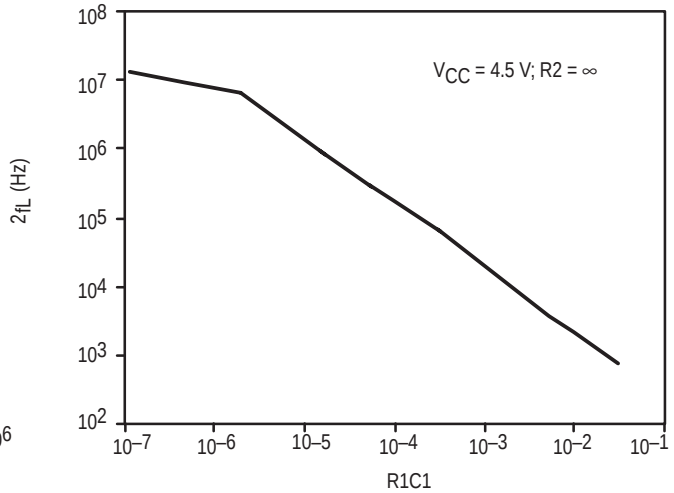


Figure 21. Typical Frequency Lock Range ($2f_L$) versus R_1C_1

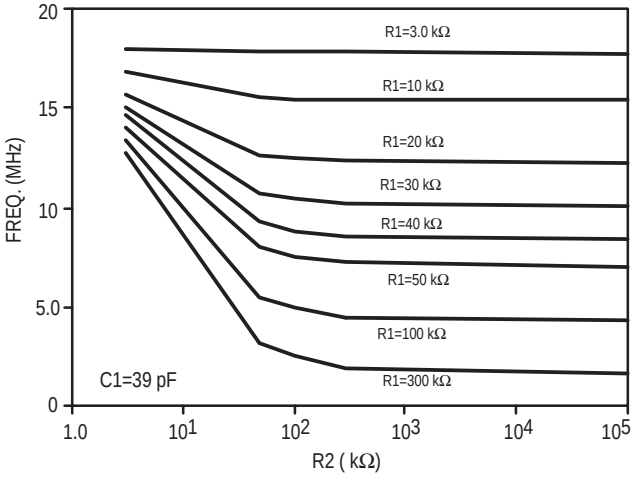


Figure 22. R2 versus f_{max}

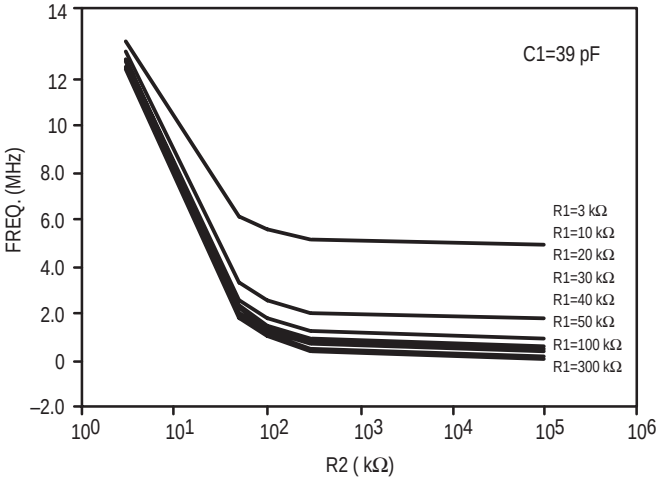


Figure 23. R2 versus f_{min}

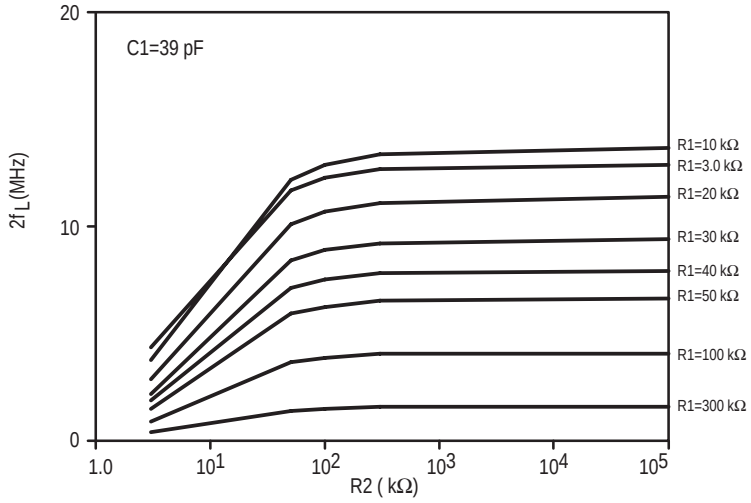


Figure 24. R2 versus Frequency Lock Range ($2f_L$)

APPLICATION INFORMATION

The following information is a guide for approximate values of R1, R2, and C1. Figures 19, 20, and 21 should be used as references as indicated below, also the values of R1, R2, and C1 should not violate the Maximum values indicated in the DC ELECTRICAL CHARACTERISTICS tables.

Phase Comparator 1		Phase Comparator 2		Phase Comparator 3	
$R_2 = \infty$	$R_2 \neq \infty$	$R_2 = \infty$	$R_2 \neq \infty$	$R_2 = \infty$	$R_2 \neq \infty$
• Given f0 • Use f0 with Figure 19 to determine R1 and C1. (see Figure 23 for characteristics of the VCO operation)	• Given f0 and fL • Calculate f_{min} f_{min} = f0–fL • Determine values of C1 and R2 from Figure 20. • Determine R1–C1 from Figure 21. • Calculate value of R1 from the value of C1 and the product of R1C1 from Figure 21. (see Figure 24 for characteristics of the VCO operation)	• Given f_{max} and f0 • Determine the value of R1 and C1 using Figure 19 and use Figure 21 to obtain 2fL and then use this to calculate f_{min}.	• Given f0 and fL • Calculate f_{min} f_{min} = f0–fL • Determine values of C1 and R2 from Figure 20. • Determine R1–C1 from Figure 21. • Calculate value of R1 from the value of C1 and the product of R1C1 from Figure 21. (see Figure 24 for characteristics of the VCO operation)	• Given f_{max} and f0 • Determine the value of R1 and C1 using Figure 19 and Figure 21 to obtain 2fL and then use this to calculate f_{min}.	• Given f0 and fL • Calculate f_{min}: f_{min} = f0–fL • Determine values of C1 and R2 from Figure 20. • Determine R1–C1 from Figure 21. • Calculate value of R1 from the value of C1 and the product of R1C1 from Figure 21. (see Figure 24 for characteristics of the VCO operation)

MC74HC4051A, MC74HC4052A, MC74HC4053A

Analog Multiplexers / Demultiplexers

High–Performance Silicon–Gate CMOS

The MC74HC4051A, MC74HC4052A and MC74HC4053A utilize silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The HC4051A, HC4052A and HC4053A are identical in pinout to the metal–gate MC14051AB, MC14052AB and MC14053AB. The Channel–Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel–Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors they are compatible with LSTTL outputs.

These devices have been designed so that the ON resistance (R_{on}) is more linear over input voltage than R_{on} of metal–gate CMOS analog switches.

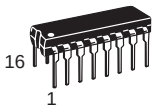
For a multiplexer/demultiplexer with injection current protection, see HC4851A and HC4852A.

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range ($V_{CC} – V_{EE}$) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range ($V_{CC} – GND$) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal–Gate Counterparts
- Low Noise
- In Compliance With the Requirements of JEDEC Standard No. 7A
- Chip Complexity: HC4051A — 184 FETs or 46 Equivalent Gates
  HC4052A — 168 FETs or 42 Equivalent Gates
  HC4053A — 156 FETs or 39 Equivalent Gates

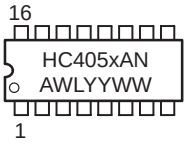
ON Semiconductor

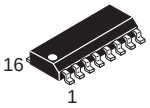
http://onsemi.com

MARKING DIAGRAMS

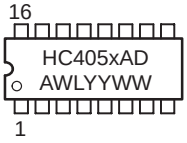


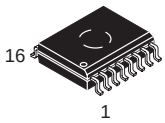
PDIP–16
N SUFFIX
CASE 648



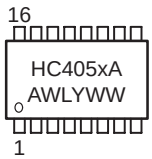


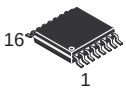
SO–16
D SUFFIX
CASE 751B



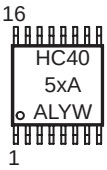


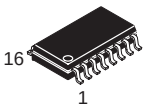
SO–16 WIDE
DW SUFFIX
CASE 751G



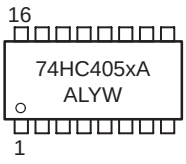


TSSOP–16
DT SUFFIX
CASE 948F





SOEIAJ–16
F SUFFIX
CASE 966

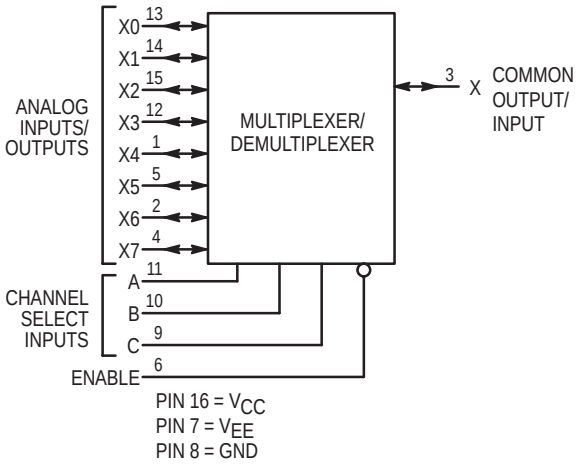


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 331 of this data sheet.

LOGIC DIAGRAM
MC74HC4051A
Single–Pole, 8–Position Plus Common Off

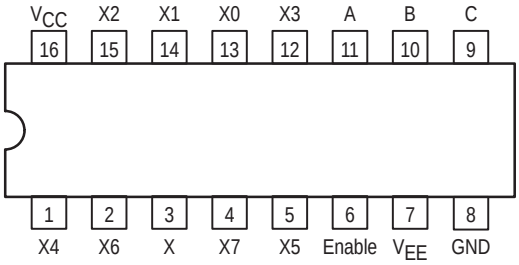


FUNCTION TABLE – MC74HC4051A

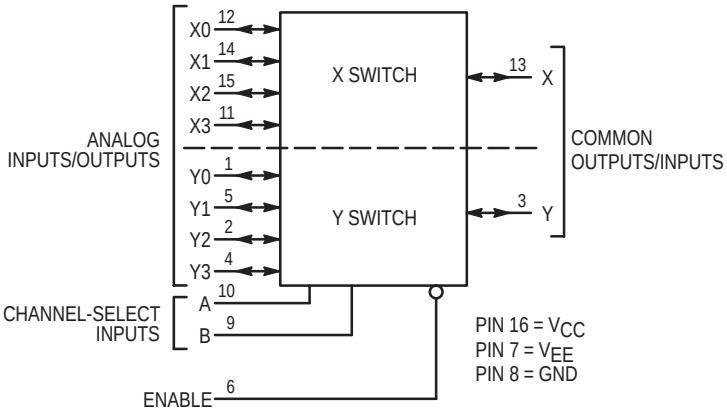
Control Inputs				
	Select			
Enable	C	B	A	ON Channels
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

X = Don't Care

Pinout: MC74HC4051A (Top View)



LOGIC DIAGRAM
MC74HC4052A
Double–Pole, 4–Position Plus Common Off

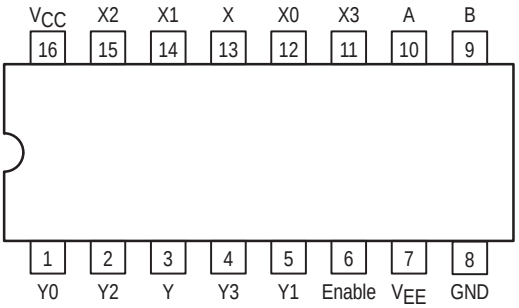


FUNCTION TABLE – MC74HC4052A

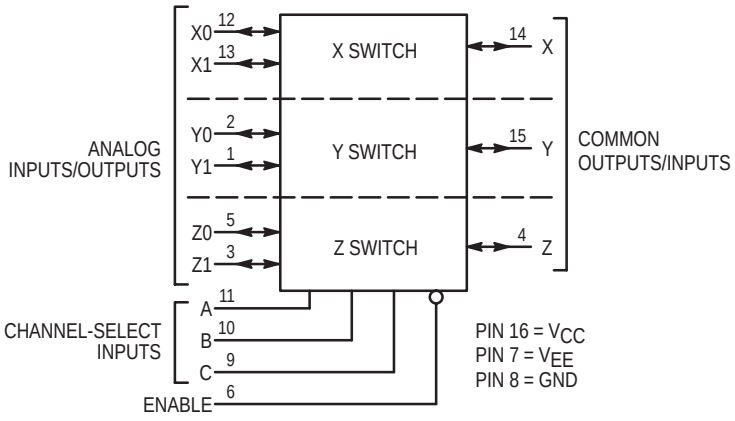
Control Inputs			
	Select		
Enable	B	A	ON Channels
L	L	L	Y0 X0
L	L	H	Y1 X1
L	H	L	Y2 X2
L	H	H	Y3 X3
H	X	X	NONE

X = Don't Care

Pinout: MC74HC4052A (Top View)



LOGIC DIAGRAM
MC74HC4053A
Triple Single–Pole, Double–Position Plus Common Off



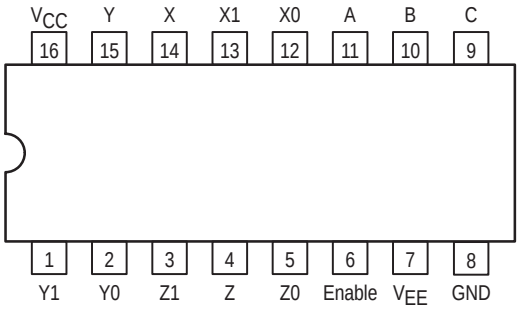
NOTE: This device allows independent control of each switch. Channel–Select Input A controls the X–Switch, Input B controls the Y–Switch and Input C controls the Z–Switch

FUNCTION TABLE – MC74HC4053A

Control Inputs						
	Select					
Enable	C	B	A	ON Channels		
L	L	L	L	Z0	Y0	X0
L	L	L	H	Z0	Y0	X1
L	L	H	L	Z0	Y1	X0
L	L	H	H	Z0	Y1	X1
L	H	L	L	Z1	Y0	X0
L	H	L	H	Z1	Y0	X1
L	H	H	L	Z1	Y1	X0
L	H	H	H	Z1	Y1	X1
H	X	X	X	NONE		

X = Don't Care

Pinout: MC74HC4053A (Top View)



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})	– 0.5 to + 7.0 – 0.5 to + 14.0	V
V_{EE}	Negative DC Supply Voltage (Referenced to GND)	– 7.0 to + 5.0	V
V_{IS}	Analog Input Voltage	V_{EE} – 0.5 to V_{CC} + 0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin	± 25	mA
P_D	Power Dissipation in Still Air, Plastic DIP† EIAJ/SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
EIAJ/SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	(Referenced to GND) (Referenced to V_{EE})	2.0 2.0	6.0 12.0	V
V_{EE}	Negative DC Supply Voltage, Output (Referenced to GND)		– 6.0	GND	V
V_{IS}	Analog Input Voltage		V_{EE}	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)		GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch			1.2	V
T_A	Operating Temperature Range, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise/Fall Time (Channel Select or Enable Inputs)	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

*For voltage drops across switch greater than 1.2V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND) V_{EE} = GND, Except Where Noted

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
I_{in}	Maximum Input Leakage Current, Channel–Select or Enable Inputs	V_{in} = V_{CC} or GND, V_{EE} = – 6.0 V	6.0	± 0.1	± 1.0	± 1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and V_{IS} = V_{CC} or GND; V_{EE} = GND V_{IO} = 0 V V_{EE} = – 6.0	 6.0 6.0	 1 4	 10 40	 20 80	µA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

DC CHARACTERISTICS — Analog Section

Symbol	Parameter	Condition	V_{CC}	V_{EE}	Guaranteed Limit			Unit
					–55 to 25°C	≤85°C	≤125°C	
R_{on}	Maximum "ON" Resistance	$V_{in} = V_{IL}$ or V_{IH}; $V_{IS} = V_{CC}$ to V_{EE}; $I_S \le 2.0$ mA (Figures 1, 2)	4.5 4.5 6.0	0.0 – 4.5 – 6.0	190 120 100	240 150 125	280 170 140	Ω
		$V_{in} = V_{IL}$ or V_{IH}; $V_{IS} = V_{CC}$ or V_{EE} (Endpoints); $I_S \le 2.0$ mA (Figures 1, 2)	4.5 4.5 6.0	0.0 – 4.5 – 6.0	150 100 80	190 125 100	230 140 115	
ΔR_{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{in} = V_{IL}$ or V_{IH}; V_{IS} = 1/2 ($V_{CC} - V_{EE}$); $I_S \le 2.0$ mA	4.5 4.5 6.0	0.0 – 4.5 – 6.0	30 12 10	35 15 12	40 18 14	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	$V_{in} = V_{IL}$ or V_{IH}; $V_{IO} = V_{CC} - V_{EE}$; Switch Off (Figure 3)	6.0	– 6.0	0.1	0.5	1.0	μA
	Maximum Off–Channel Leakage Current, Common Channel HC4051A HC4052A HC4053A	$V_{in} = V_{IL}$ or V_{IH}; $V_{IO} = V_{CC} - V_{EE}$; Switch Off (Figure 4)	6.0 6.0 6.0	– 6.0 – 6.0 – 6.0	0.2 0.1 0.1	2.0 1.0 1.0	4.0 2.0 2.0	
I_{on}	Maximum On–Channel Leakage Current, Channel–to–Channel HC4051A HC4052A HC4053A	$V_{in} = V_{IL}$ or V_{IH}; Switch–to–Switch = $V_{CC} - V_{EE}$; (Figure 5)	6.0 6.0 6.0	– 6.0 – 6.0 – 6.0	0.2 0.1 0.1	2.0 1.0 1.0	4.0 2.0 2.0	μA

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Channel–Select to Analog Output (Figure 9)	2.0 3.0 4.5 6.0	270 90 59 45	320 110 79 65	350 125 85 75	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.0 3.0 4.5 6.0	40 25 12 10	60 30 15 13	70 32 18 15	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0 3.0 4.5 6.0	160 70 48 39	200 95 63 55	220 110 76 63	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0 3.0 4.5 6.0	245 115 49 39	315 145 69 58	345 155 83 67	ns
C_{in}	Maximum Input Capacitance, Channel–Select or Enable Inputs		10	10	10	pF
$C_{I/O}$	Maximum Capacitance — Analog I/O		35	35	35	pF
	(All Switches Off) — Common O/I: HC4051A HC4052A HC4053A		130 80 50	130 80 50	130 80 50	
	Feedthrough		1.0	1.0	1.0	

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D)

Symbol	Parameter		Typical @ 25°C, V_{CC} = 5.0 V, V_{EE} = 0 V	Unit
C_{PD}	Power Dissipation Capacitance (Figure 13)*	HC4051A HC4052A HC4053A	45 80 45	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V_{CC} V	V_{EE} V	Limit* 25°C '51	Limit* 25°C '52	Limit* 25°C '53	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 6)	f_{in} = 1MHz Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{OS}; Increase f_{in} Frequency Until dB Meter Reads –3dB; R_L = 50Ω, C_L = 10pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	80 80 80	95 95 95	120 120 120	MHz
—	Off–Channel Feedthrough Isolation (Figure 7)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{IS} f_{in} = 10kHz, R_L = 600Ω, C_L = 50pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	–50 –50 –50			dB
		f_{in} = 1.0MHz, R_L = 50Ω, C_L = 10pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	–40 –40 –40			
—	Feedthrough Noise. Channel–Select Input to Common I/O (Figure 8)	V_{in} ≤ 1MHz Square Wave (t_r = t_f = 6ns); Adjust R_L at Setup so that I_S = 0A; Enable = GND R_L = 600Ω, C_L = 50pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	25 105 135			mV_{PP}
		R_L = 10kΩ, C_L = 10pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	35 145 190			
—	Crosstalk Between Any Two Switches (Figure 12) (Test does not apply to HC4051A)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{IS} f_{in} = 10kHz, R_L = 600Ω, C_L = 50pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	–50 –50 –50			dB
		f_{in} = 1.0MHz, R_L = 50Ω, C_L = 10pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	–60 –60 –60			
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1kHz, R_L = 10kΩ, C_L = 50pF $THD = THD_{measured} - THD_{source}$ V_{IS} = 4.0V_{PP} sine wave V_{IS} = 8.0V_{PP} sine wave V_{IS} = 11.0V_{PP} sine wave	2.25 4.50 6.00	–2.25 –4.50 –6.00	0.10 0.08 0.05			%

*Limits not tested. Determined by design and verified by qualification.

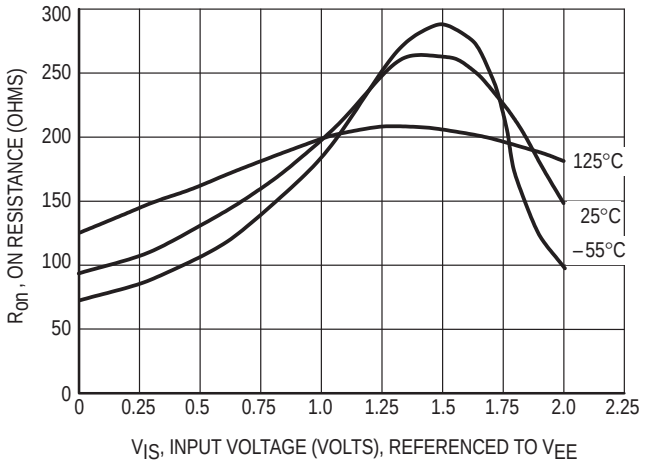


Figure 1a. Typical On Resistance, $V_{CC} - V_{EE}$ = 2.0 V

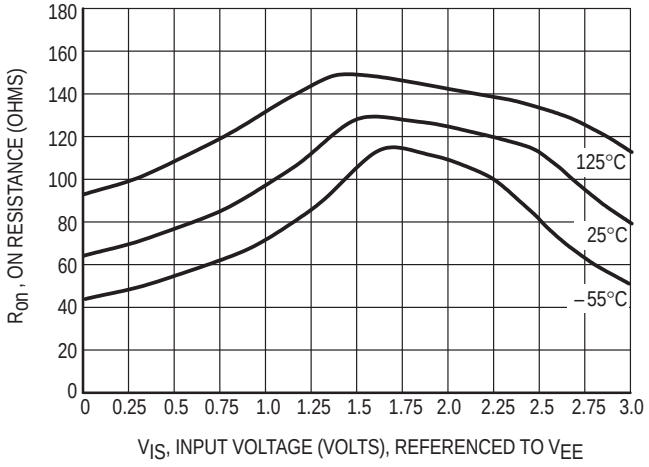


Figure 1b. Typical On Resistance, $V_{CC} - V_{EE}$ = 3.0 V

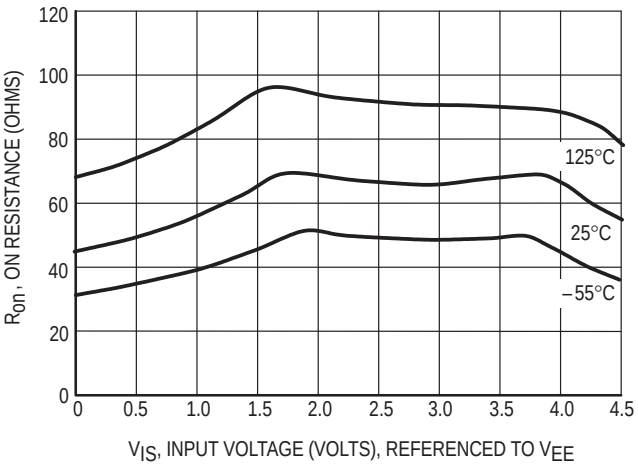


Figure 1c. Typical On Resistance, $V_{CC} - V_{EE}$ = 4.5 V

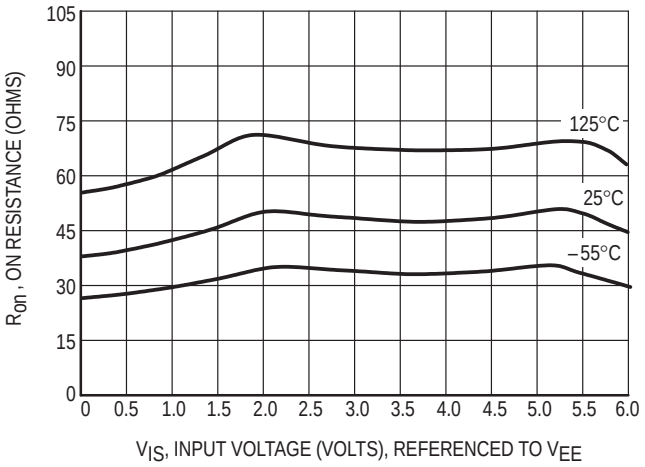


Figure 1d. Typical On Resistance, $V_{CC} - V_{EE}$ = 6.0 V

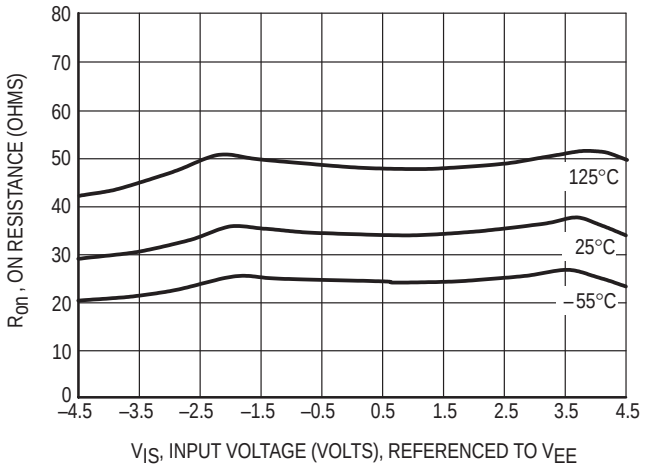


Figure 1e. Typical On Resistance, $V_{CC} - V_{EE}$ = 9.0 V

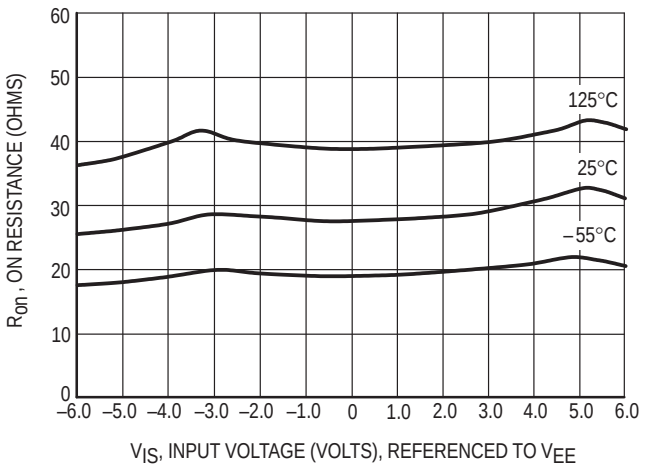


Figure 1f. Typical On Resistance, $V_{CC} - V_{EE}$ = 12.0 V

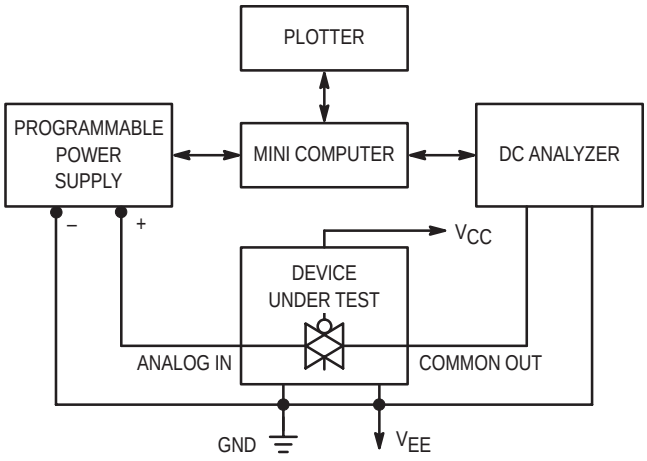


Figure 2. On Resistance Test Set–Up

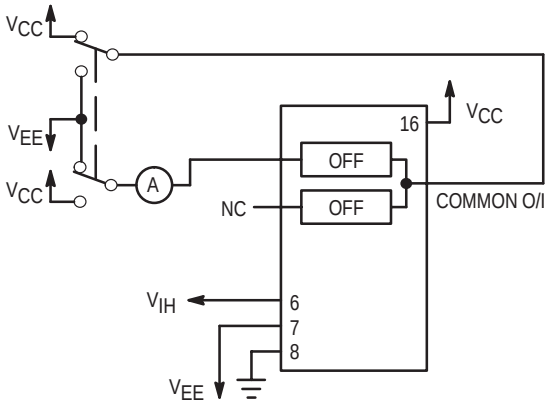


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

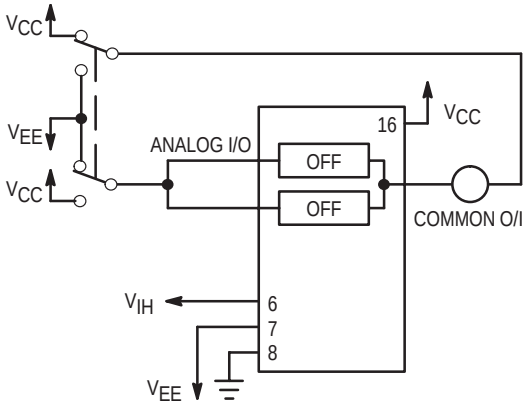


Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set–Up

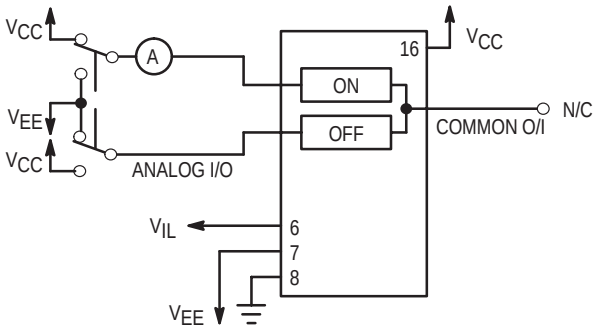


Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set–Up

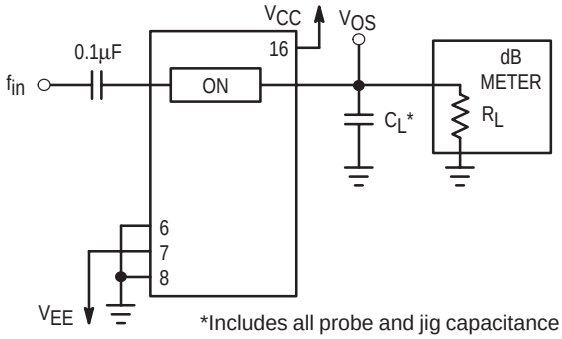


Figure 6. Maximum On Channel Bandwidth, Test Set–Up

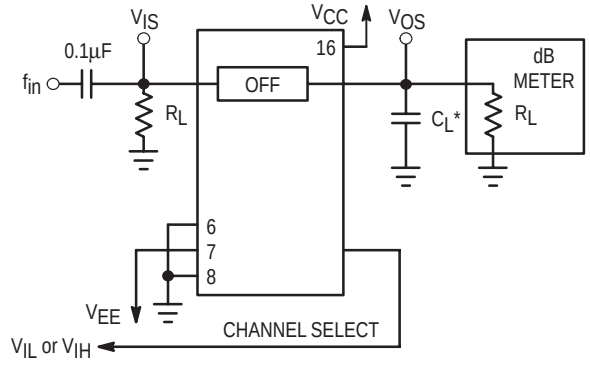


Figure 7. Off Channel Feedthrough Isolation, Test Set–Up

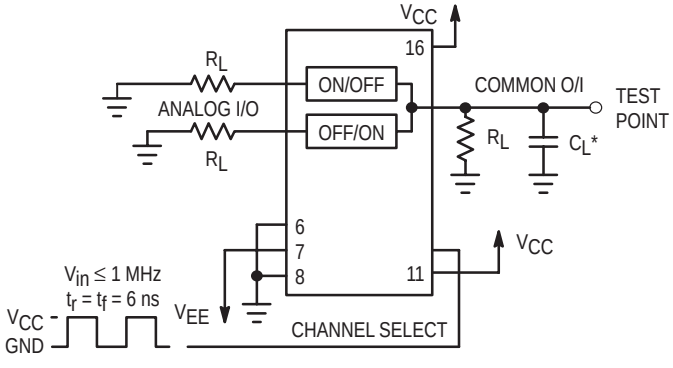


Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set–Up

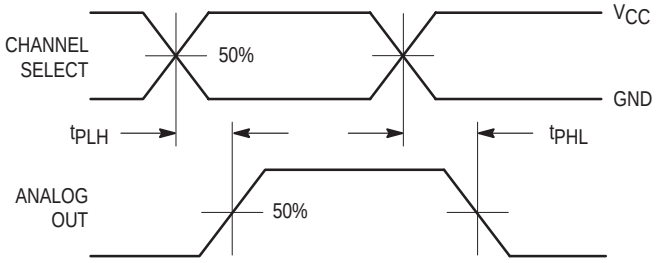
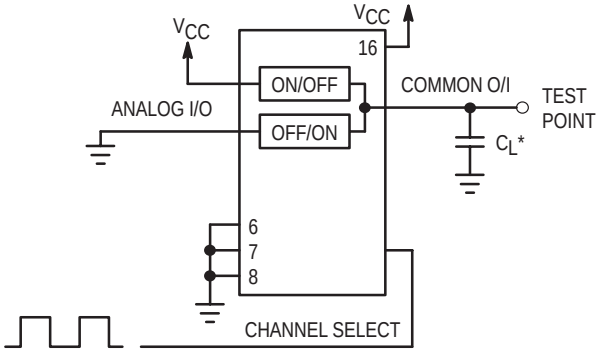


Figure 9a. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 9b. Propagation Delay, Test Set–Up Channel Select to Analog Out

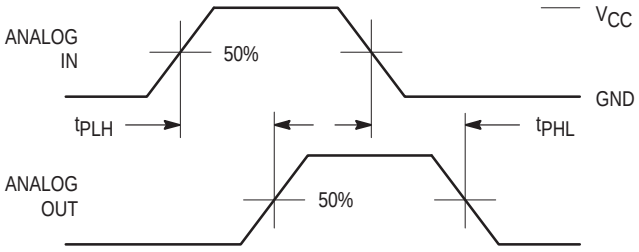
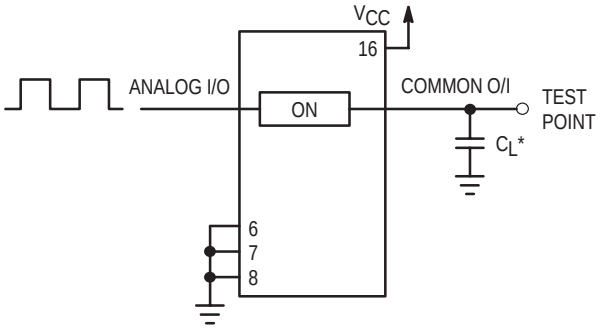


Figure 10a. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance

Figure 10b. Propagation Delay, Test Set–Up Analog In to Analog Out

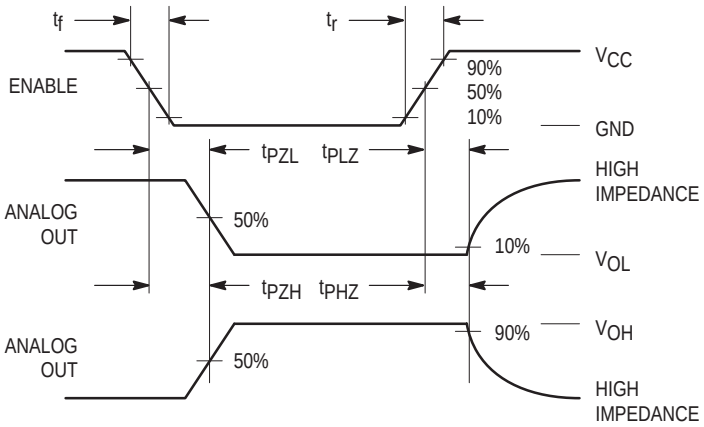


Figure 11a. Propagation Delays, Enable to Analog Out

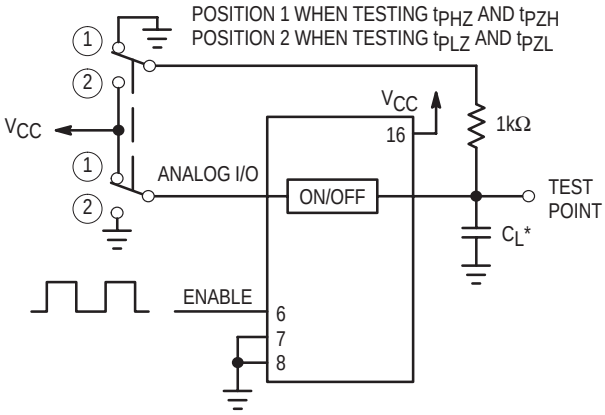


Figure 11b. Propagation Delay, Test Set–Up Enable to Analog Out

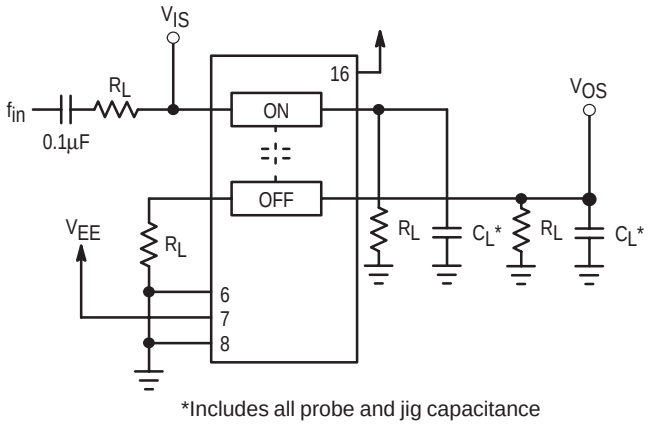


Figure 12. Crosstalk Between Any Two Switches, Test Set–Up

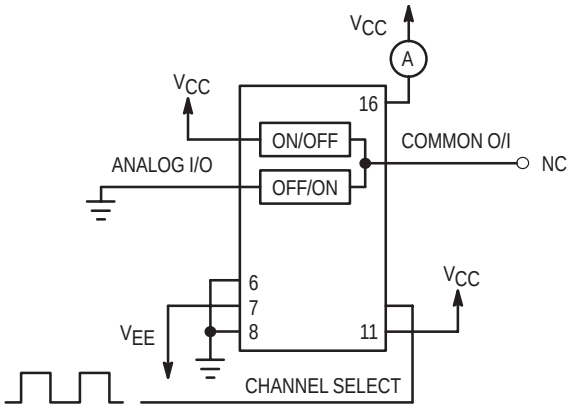


Figure 13. Power Dissipation Capacitance, Test Set–Up

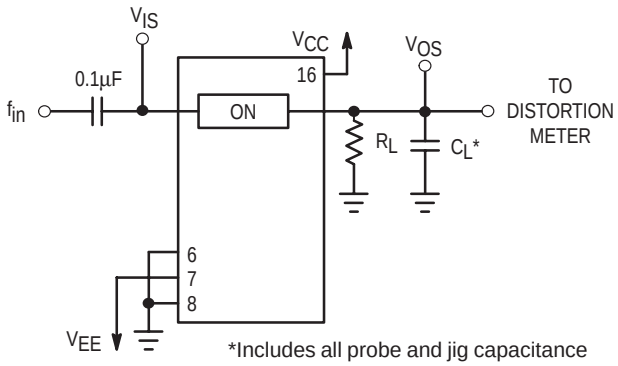


Figure 14a. Total Harmonic Distortion, Test Set–Up

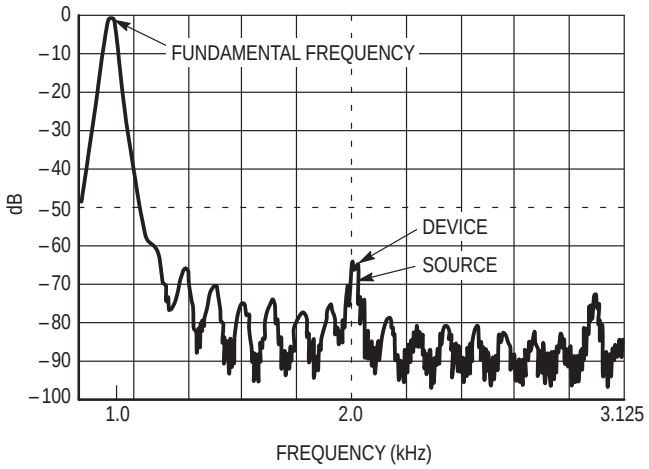


Figure 14b. Plot, Harmonic Distortion

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

V_{CC} = +5V = logic high
GND = 0V = logic low

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below V_{EE}. In this example, the difference between V_{CC} and V_{EE} is ten volts. Therefore, using the configuration of Figure 15, a maximum analog signal of ten volts peak–to–peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

V_{CC} – GND = 2 to 6 volts
V_{EE} – GND = 0 to –6 volts
V_{CC} – V_{EE} = 2 to 12 volts
and $V_{EE} \leq$ GND

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external Germanium or Schottky diodes (D_X) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

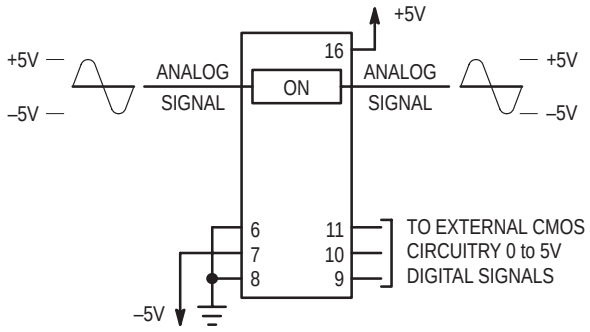


Figure 15. Application Example

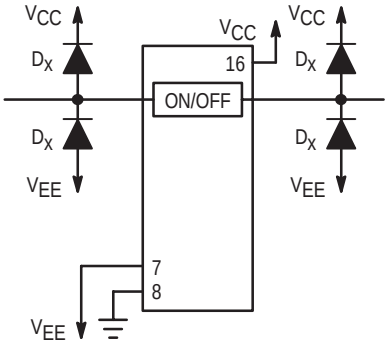
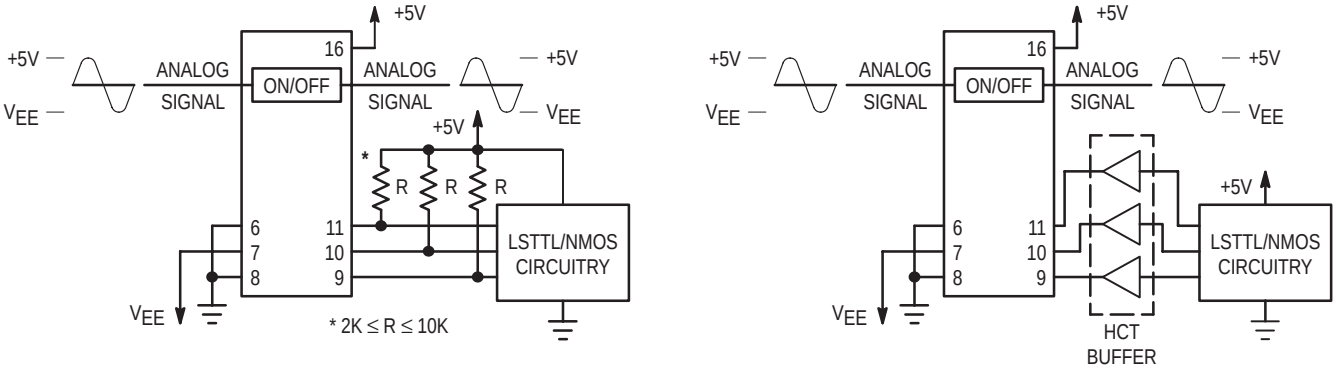


Figure 16. External Germanium or Schottky Clipping Diodes



a. Using Pull–Up Resistors

b. Using HCT Interface

Figure 17. Interfacing LSTTL/NMOS to CMOS Inputs

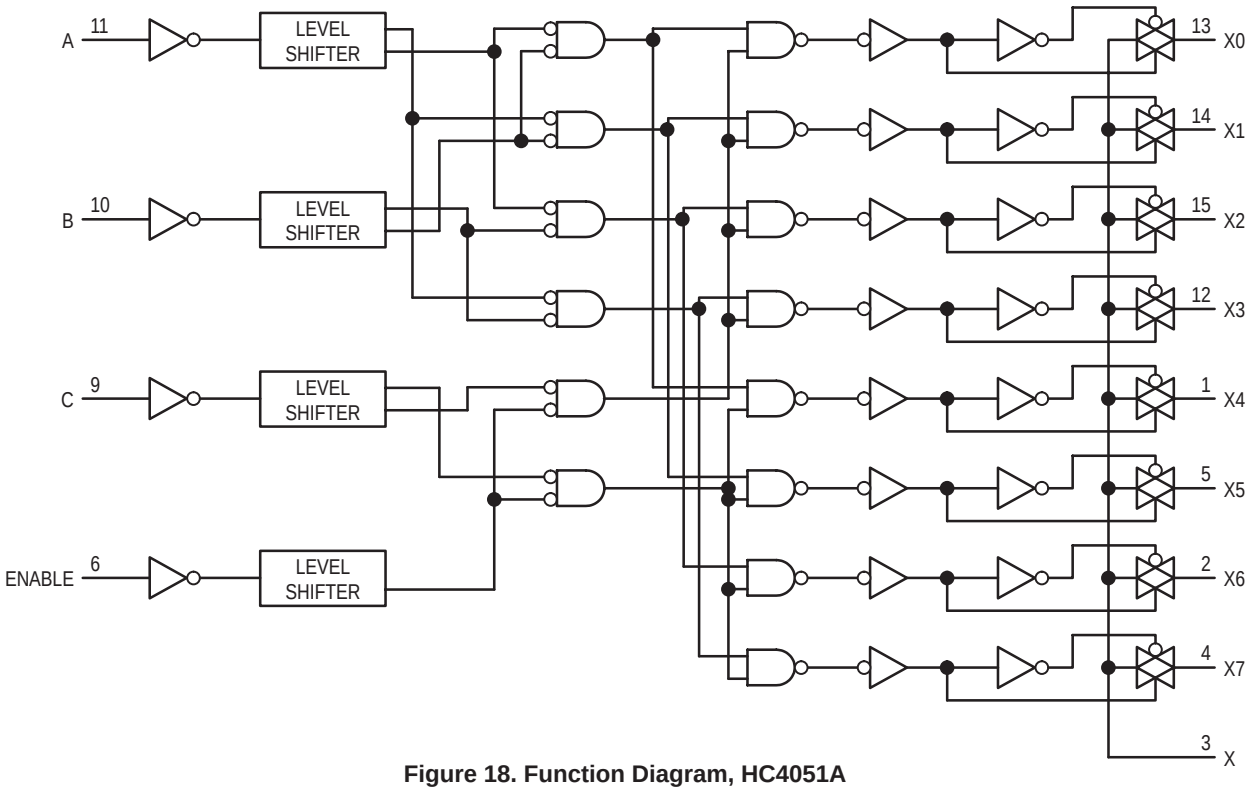


Figure 18. Function Diagram, HC4051A

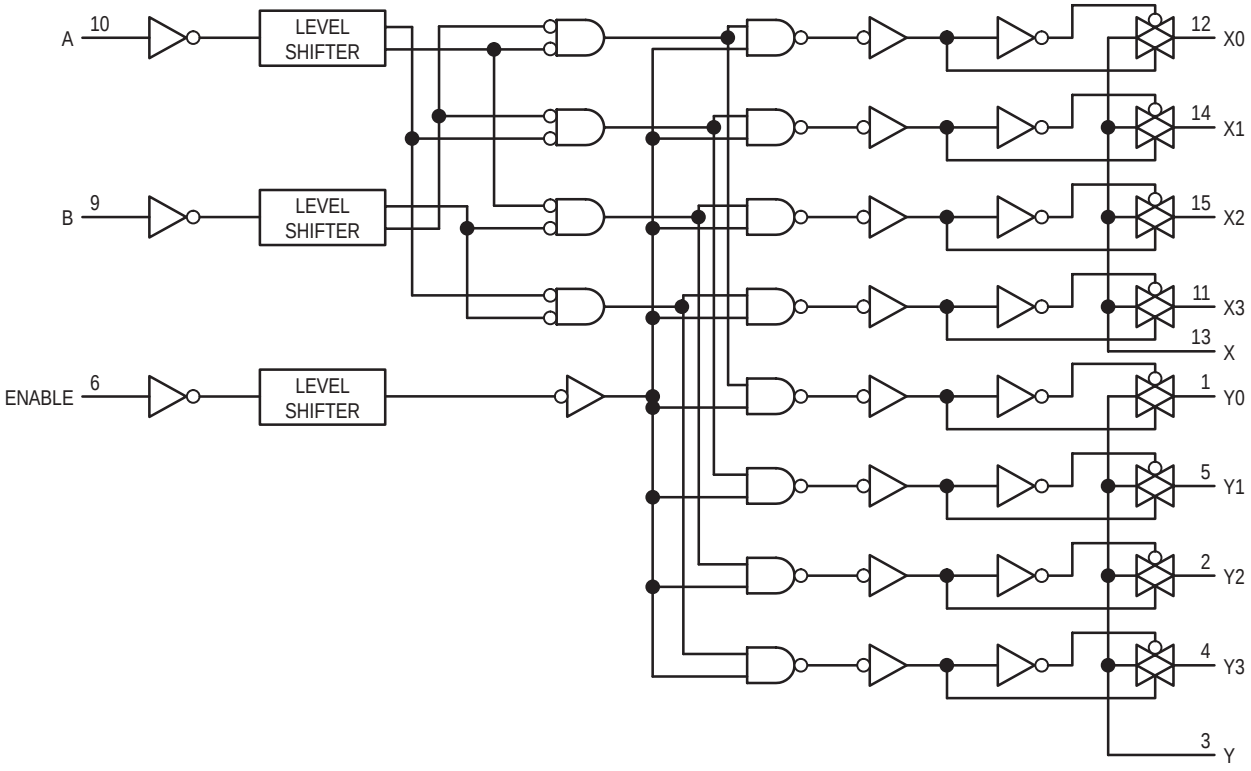


Figure 19. Function Diagram, HC4052A

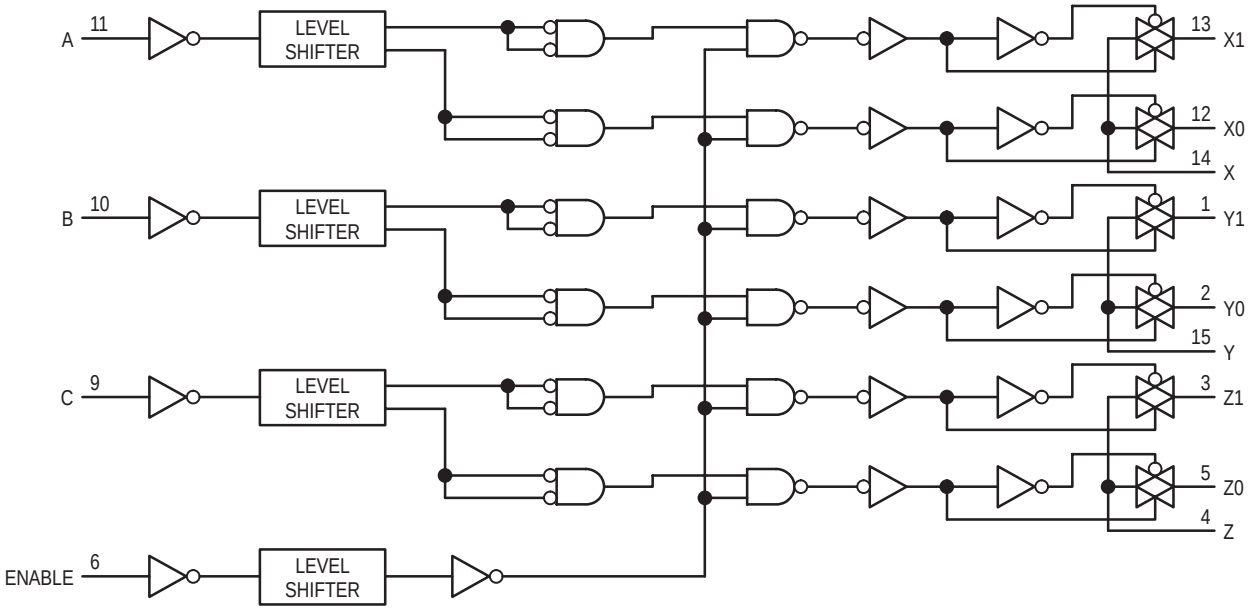


Figure 20. Function Diagram, HC4053A

ORDERING & SHIPPING INFORMATION

Device	Package	Shipping
MC74HC4051AN	PDIP–16	500 Units / Unit Pak
MC74HC4051AD	SOIC–16	48 Units / Rail
MC74HC4051ADR2	SOIC–16	2500 Units / Tape & Reel
MC74HC4051ADT	TSSOP–16	96 Units / Rail
MC74HC4051ADTR2	TSSOP–16	2500 Units / Tape & Reel
MC74HC4051ADW	SOIC WIDE	48 Units / Rail
MC74HC4051ADWR2	SOIC WIDE	1000 Units / Tape & Reel
MC74HC4051AF	SOEIAJ–16	See Note 1.
MC74HC4051AFEL	SOEIAJ–16	See Note 1.
MC74HC4052AN	PDIP–16	500 Units / Unit Pak
MC74HC4052AD	SOIC–16	48 Units / Rail
MC74HC4052ADR2	SOIC–16	2500 Units / Tape & Reel
MC74HC4052ADT	TSSOP–16	96 Units / Rail
MC74HC4052ADTR2	TSSOP–16	2500 Units / Tape & Reel
MC74HC4052ADW	SOIC WIDE	48 Units / Rail
MC74HC4052ADWR2	SOIC WIDE	1000 Units / Tape & Reel
MC74HC4052AF	SOEIAJ–16	See Note 1.
MC74HC4052AFEL	SOEIAJ–16	See Note 1.
MC74HC4053AN	PDIP–16	500 Units / Unit Pak
MC74HC4053AD	SOIC–16	48 Units / Rail
MC74HC4053ADR2	SOIC–16	2500 Units / Tape & Reel
MC74HC4053ADT	TSSOP–16	96 Units / Rail
MC74HC4053ADTR2	TSSOP–16	2500 Units / Tape & Reel
MC74HC4053ADW	SOIC WIDE	48 Units / Rail
MC74HC4053ADWR2	SOIC WIDE	1000 Units / Tape & Reel
MC74HC4053AF	SOEIAJ–16	See Note 1.
MC74HC4053AFEL	SOEIAJ–16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

MC74HC4060A

14-Stage Binary Ripple Counter With Oscillator

High–Performance Silicon–Gate CMOS

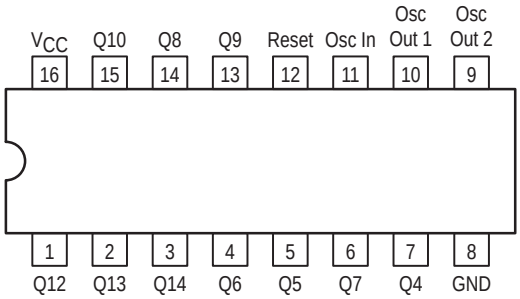
The MC74C4060A is identical in pinout to the standard CMOS MC14060B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of 14 master–slave flip–flops and an oscillator with a frequency that is controlled either by a crystal or by an RC circuit connected externally. The output of each flip–flop feeds the next and the frequency at each output is half of that of the preceding one. The state of the counter advances on the negative–going edge of the Osc In. The active–high Reset is asynchronous and disables the oscillator to allow very low power consumption during stand–by operation.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with Osc Out 2 of the HC4060A.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With JEDEC Standard No. 7A Requirements
- Chip Complexity: 390 FETs or 97.5 Equivalent Gates

Pinout: 16–Lead Plastic Package (Top View)



FUNCTION TABLE

Clock	Reset	Output State
⎍	L	No Change
⎎	L	Advance to Next State
X	H	All Outputs Are Low

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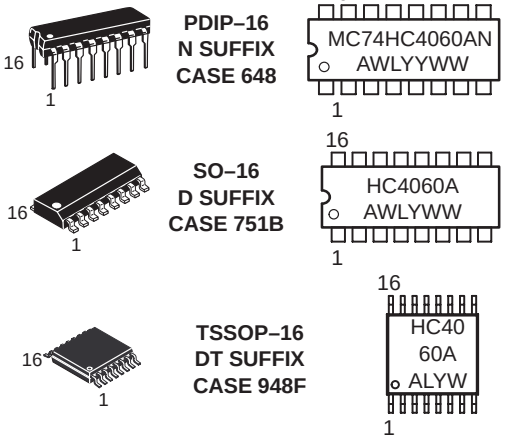
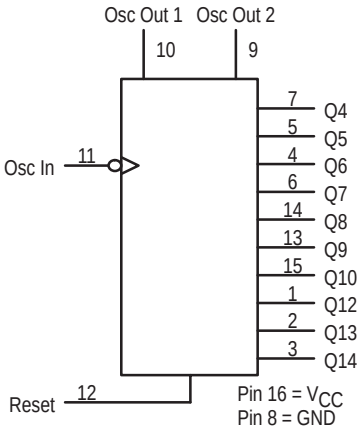
MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

LOGIC DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping
MC74HC4060AN	PDIP–16	2000 / Box
MC74HC4060AD	SOIC–16	48 / Rail
MC74HC4060ADR2	SOIC–16	2500 / Reel
MC74HC4060ADT	TSSOP–16	96 / Rail
MC74HC4060ADTR2	TSSOP–16	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.5*	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature Range, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise/Fall Time (Figure 1) V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

*The oscillator is guaranteed to function at 2.5 V minimum. However, parametrics are tested at 2.0 V by driving Pin 11 with an external clock source.

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit –55 to 25°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1V or V_{CC} –0.1V $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1V or V_{CC} – 0.1V $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
V_{OH}	Minimum High–Level Output Voltage (Q4–Q10, Q12–Q14)	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} =V_{IH} or V_{IL} $\|I_{out}\| \le 2.4mA$ $\|I_{out}\| \le 4.0mA$ $\|I_{out}\| \le 5.2mA$	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{OL}	Maximum Low–Level Output Voltage (Q4–Q10, Q12–Q14)	$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out}\rvert \le 20\mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out}\rvert \le 2.4mA$ $\lvert I_{out}\rvert \le 4.0mA$ $\lvert I_{out}\rvert \le 5.2mA$	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
V_{OH}	Minimum High–Level Output Voltage (Osc Out 1, Osc Out 2)	$V_{in} = V_{CC}$ or GND $\lvert I_{out}\rvert \le 20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{CC}$ or GND $\lvert I_{out}\rvert \le 0.7mA$ $\lvert I_{out}\rvert \le 1.0mA$ $\lvert I_{out}\rvert \le 1.3mA$	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage (Osc Out 1, Osc Out 2)	$V_{in} = V_{CC}$ or GND $\lvert I_{out}\rvert \le 20\mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{CC}$ or GND $\lvert I_{out}\rvert \le 0.7mA$ $\lvert I_{out}\rvert \le 1.0mA$ $\lvert I_{out}\rvert \le 1.3mA$	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0\mu A$	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 3.0 4.5 6.0	6.0 10 30 50	9.0 14 28 45	8.0 12 25 40	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Osc In to Q4* (Figures 1 and 4)	2.0 3.0 4.5 6.0	300 180 60 51	375 200 75 64	450 250 90 75	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Osc In to Q14* (Figures 1 and 4)	2.0 3.0 4.5 6.0	500 350 250 200	750 450 275 220	1000 600 300 250	ns
t_{PHL}	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 4)	2.0 3.0 4.5 6.0	195 75 39 33	245 100 49 42	300 125 61 53	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Qn to Qn+1 (Figures 3 and 4)	2.0 3.0 4.5 6.0	75 60 15 13	95 75 19 16	125 95 24 20	ns

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns) **– continued**

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
C_{in}	Maximum Input Capacitance		10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

* For T_A = 25°C and C_L = 50 pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:

V_{CC} = 2.0 V: t_P = [93.7 + 59.3 (n–1)] ns V_{CC} = 4.5 V: t_P = [30.25 + 14.6 (n–1)] ns

V_{CC} = 3.0 V: t_P = [61.5+ 34.4 (n–1)] ns V_{CC} = 6.0 V: t_P = [24.4 + 12 (n–1)] ns

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package)*	35	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	100	125	150	ns
		3.0	75	100	120	
		4.5	20	25	30	
		6.0	17	21	25	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	23	
		6.0	13	16	19	
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	23	
		6.0	13	16	19	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		3.0	800	800	800	
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

PIN DESCRIPTIONS

INPUTS

Osc In (Pin 11)

Negative–edge triggering clock input. A high–to–low transition on this input advances the state of the counter. Osc In may be driven by an external clock source.

Reset (Pin 12)

Active–high reset. A high level applied to this input asynchronously resets the counter to its zero state (forcing all Q outputs low) and disables the oscillator.

OUTPUTS

Q4—Q10, Q12–Q14 (Pins 7, 5, 4, 6, 13, 15, 1, 2, 3)

Active–high outputs. Each Qn output divides the Clock input frequency by 2^N. The user should note the Q1, Q2, Q3 and Q11 are not available as outputs.

Osc Out 1, Osc Out 2 (Pins 9, 10)

Oscillator outputs. These pins are used in conjunction with Osc In and the external components to form an oscillator. When Osc In is being driven with an external clock source, Osc Out 1 and Osc Out 2 must be left open circuited. With the crystal oscillator configuration in Figure 6, Osc Out 2 must be left open circuited.

SWITCHING WAVEFORMS

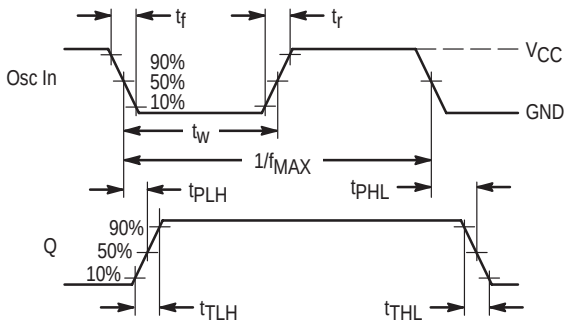


Figure 1.

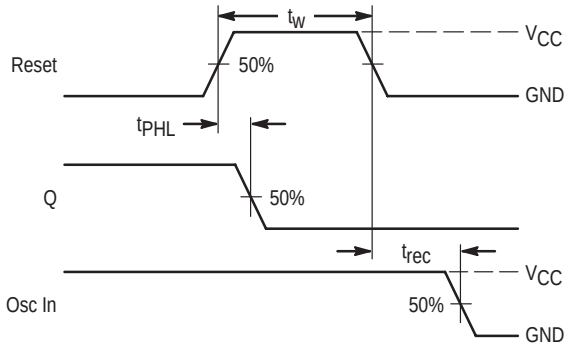


Figure 2.

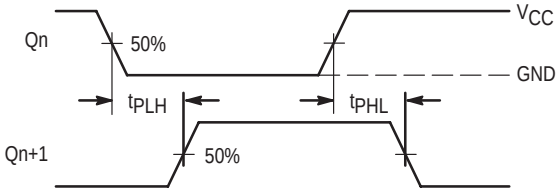
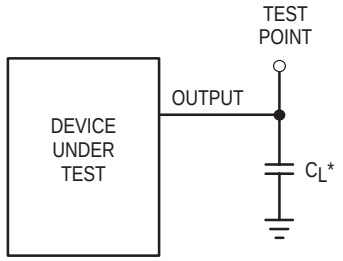


Figure 3.



*Includes all probe and jig capacitance

Figure 4. Test Circuit

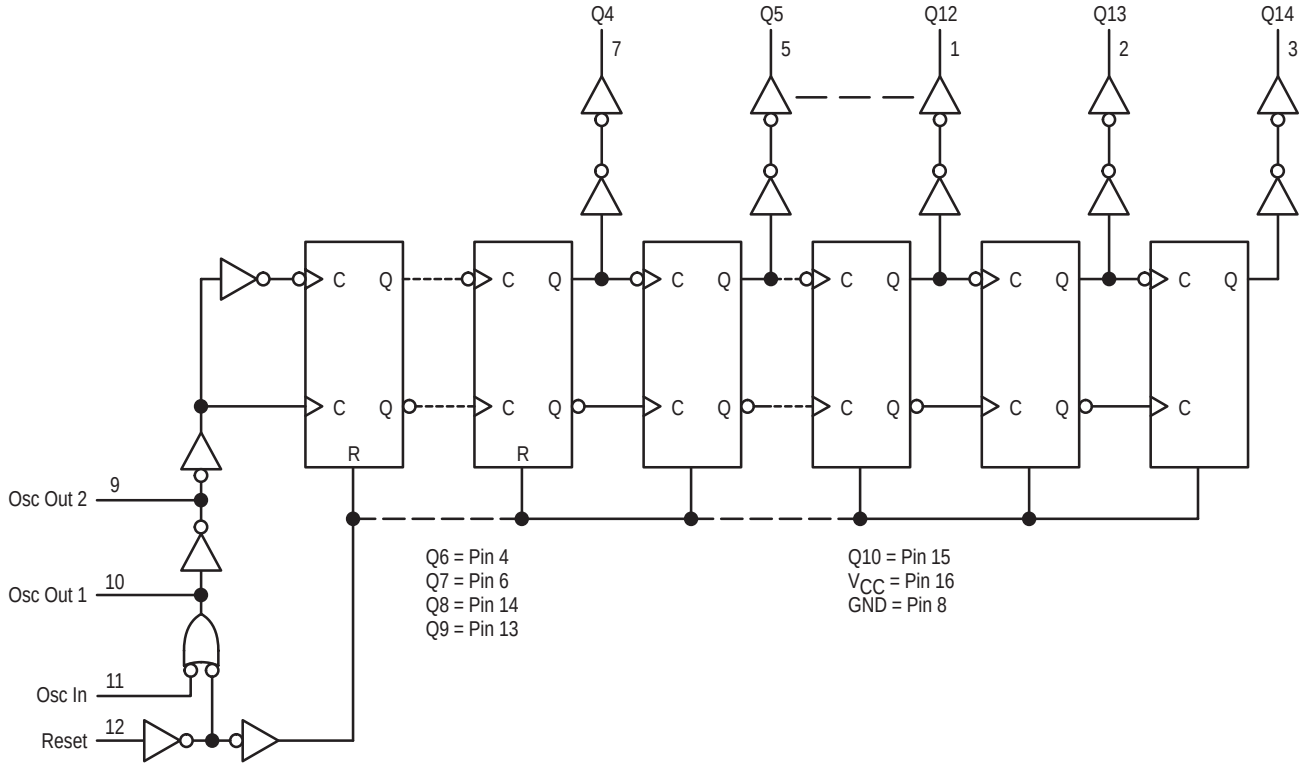
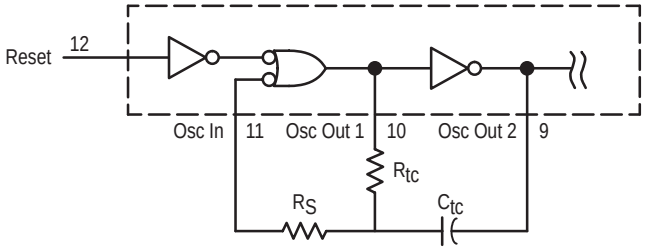


Figure 5. Expanded Logic Diagram



For $2.0V \le V_{CC} \le 6.0V$
$10R_{tc} > R_S > 2R_{tc}$
$400Hz \le f \le 400Khz$:

$$f \approx \frac{1}{3\ R_{tc}C_{tc}}$$ (f in Hz, R_{tc} in ohms, C_{tc} in farads)

The formula may vary for other frequencies.

Figure 6. Oscillator Circuit Using RC Configuration

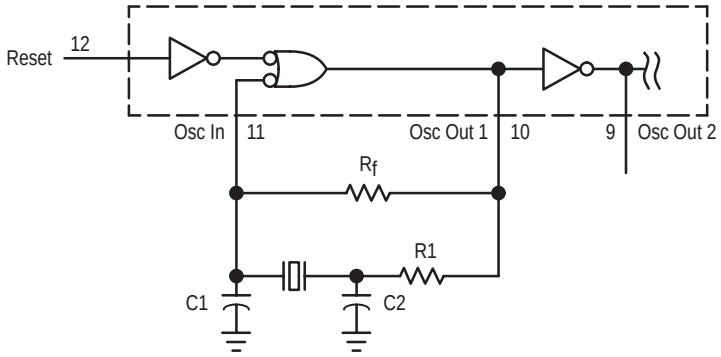
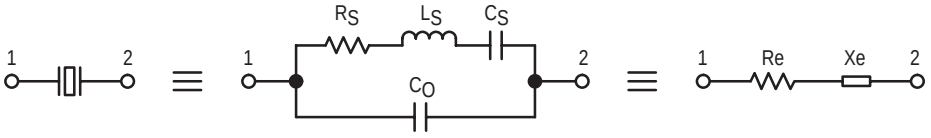


Figure 7. Pierce Crystal Oscillator Circuit

TABLE 1. CRYSTAL OSCILLATOR AMPLIFIER SPECIFICATIONS (T_A = 25°C; Input = Pin 11, Output = Pin 10)

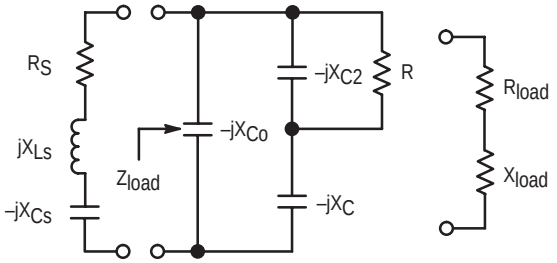
Type		Positive Reactance (Pierce)
Input Resistance, R_{in}		60MΩ Minimum
Output Impedance, Z_{out} (4.5V Supply)		200Ω (See Text)
Input Capacitance, C_{in}		5pF Typical
Output Capacitance, C_{out}		7pF Typical
Series Capacitance, C_a		5pF Typical
Open Loop Voltage Gain with Output at Full Swing, α	3Vdc Supply 4Vdc Supply 5Vdc Supply 6Vdc Supply	5.0 Expected Minimum 4.0 Expected Minimum 3.3 Expected Minimum 3.1 Expected Minimum

PIERCE CRYSTAL OSCILLATOR DESIGN



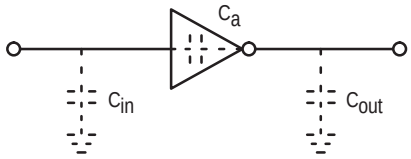
Value are supplied by crystal manufacturer (parallel resonant crystal).

Figure 8. Equivalent Crystal Networks



NOTE: C = C1 + C_{in} and R = R1 + R_{out}. C_o is considered as part of the load. C_a and R_f typically have minimal effect below 2MHz.

Figure 9. Series Equivalent Crystal Load



Values are listed in Table 1.

Figure 10. Parasitic Capacitances of the Amplifier

DESIGN PROCEDURES

The following procedure applies for oscillators operating below 2MHz where Z is a resistor R1. Above 2MHz, additional impedance elements should be considered: C_{out} and C_a of the amp, feedback resistor R_f, and amplifier phase shift error from 180°C.

Step 1: Calculate the equivalent series circuit of the crystal at the frequency of oscillation.

$$Z_e = \frac{-jX_{C_0}(R_S + jX_{L_S} - jX_{C_S})}{-jX_{C_0} + R_S + jX_{L_S} - jX_{C_S}} = R_e + jX_e$$

Reactance jX_e should be positive, indicating that the crystal is operating as an inductive reactance at the oscillation frequency. The maximum R_S for the crystal should be used in the equation.

Step 2: Determine β, the attenuation, of the feedback network. For a closed-loop gain of 2, $A_v\beta = 2, \beta = 2/A_v$ where A_v is the gain of the HC4060A amplifier.

Step 3: Determine the manufacturer's loading capacitance. For example: A manufacturer may specify an external load capacitance of 32pF at the required frequency.

Step 4: Determine the required Q of the system, and calculate R_{load}, For example, a manufacturer specifies a crystal Q of 100,000. In-circuit Q is arbitrarily set at 20% below crystal Q or 80,000. Then $R_{load} = (2\pi f_o L_S/Q) - R_S$ where L_S and R_S are crystal parameters.

Step 5: Simultaneously solve, using a computer,

$$\beta = \frac{X_C \cdot X_{C2}}{R \cdot R_e + X_{C2}\,(X_e - X_C)} \quad \text{(with feedback phase shift = 180°)} \qquad \text{(Eq 1)}$$

$$X_e = X_{C2} + X_C + \frac{R_e X_{C2}}{R} = X_{C_{load}} \quad \text{(where the loading capacitor is an external load, not including } C_o\text{)} \qquad \text{(Eq 2)}$$

$$R_{load} = \frac{RX_{C_0}X_{C2}\,[(X_C + X_{C2})(X_C + X_{C_0}) - X_C(X_C + X_{C_0} + X_{C2})]}{X^2_{C2}(X_C + X_{C_0})^2 + R^2(X_C + X_{C_0} + X_{C2})^2} \qquad \text{(Eq 3)}$$

Here $R = R_{out} + R1$. R_{out} is amp output resistance, R1 is Z. The C corresponding to X_C is given by $C = C1 + C_{in}$.

Alternately, pick a value for R1 (i.e, let $R1 = R_S$). Solve Equations 1 and 2 for C1 and C2. Use Equation 3 and the fact that $Q = 2\pi f_o L_S/(R_S + R_{load})$ to find in-circuit Q. If Q is not satisfactory pick another value for R1 and repeat the procedure.

CHOOSING R1

Power is dissipated in the effective series resistance of the crystal. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 limits the drive level.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at Osc Out 2 (Pin 9). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

SELECTING R_f

The feedback resistor, R_f, typically ranges up to 20MΩ. R_f determines the gain and bandwidth of the amplifier. Proper bandwidth insures oscillation at the correct frequency plus roll-off to minimize gain at undesirable frequencies, such as the first overtone. R_f must be large enough so as to not affect the phase of the feedback network in an appreciable manner.

ACKNOWLEDGEMENTS AND RECOMMENDED REFERENCES

The following publications were used in preparing this data sheet and are hereby acknowledged and recommended for reading:

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

D. Babin, "Designing Crystal Oscillators", Machine Design, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", Machine Design, April 25, 1985.

ALSO RECOMMENDED FOR READING:

E. Hafner, "The Piezoelectric Crystal Unit-Definitions and Method of Measurement", Proc. IEEE, Vol. 57, No. 2, Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", Electro-Technology, June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", Electronic Design, May, 1966.

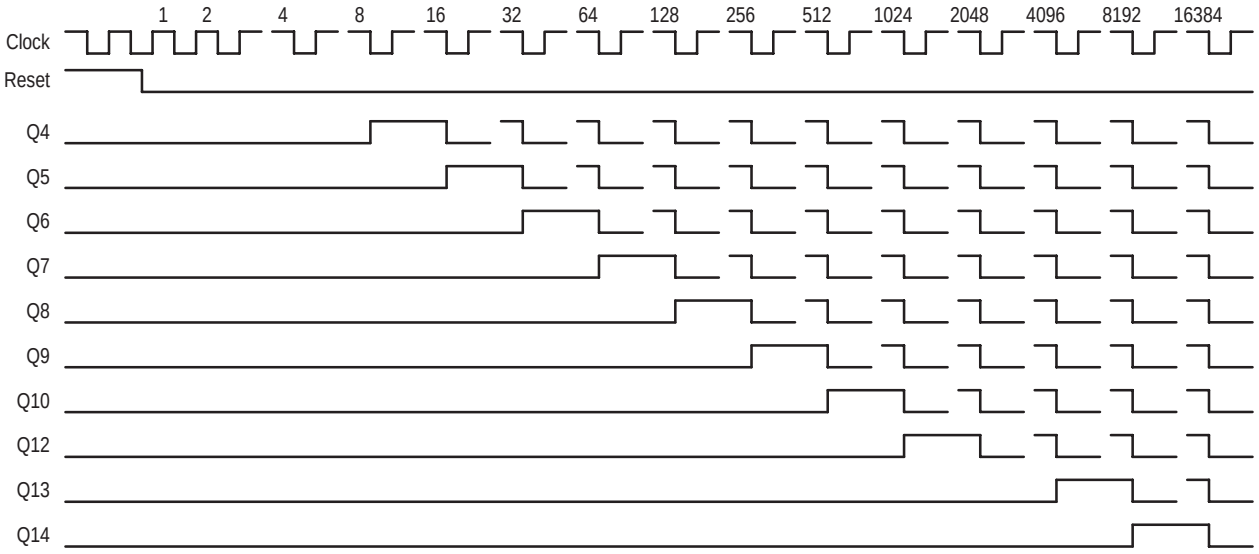


Figure 11. Timing Diagram

MC74HC4066A

Advance Information

Quad Analog Switch/ Multiplexer/Demultiplexer

High–Performance Silicon–Gate CMOS

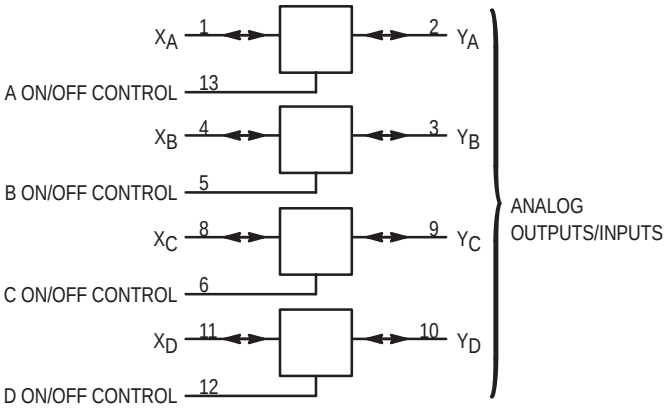
The MC74HC4066A utilizes silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF–channel leakage current. This bilateral switch/ multiplexer/demultiplexer controls analog and digital voltages that may vary across the full power–supply range (from V_{CC} to GND).

The HC4066A is identical in pinout to the metal–gate CMOS MC14016 and MC14066. Each device has four independent switches. The device has been designed so that the ON resistances (R_{ON}) are much more linear over input voltage than R_{ON} of metal–gate CMOS analog switches.

The ON/OFF control inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. For analog switches with voltage–level translators, see the HC4316A.

- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Wide Power–Supply Voltage Range (V_{CC} – GND) = 2.0 to 12.0 Volts
- Analog Input Voltage Range (V_{CC} – GND) = 2.0 to 12.0 Volts
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14016 or MC14066
- Low Noise
- Chip Complexity: 44 FETs or 11 Equivalent Gates

LOGIC DIAGRAM



ANALOG INPUTS/OUTPUTS = X_A, X_B, X_C, X_D
PIN 14 = V_{CC}
PIN 7 = GND

FUNCTION TABLE

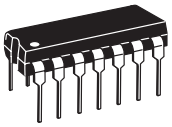
On/Off Control Input	State of Analog Switch
L	Off
H	On

This document contains information on a new product. Specifications and information herein are subject to change without notice.

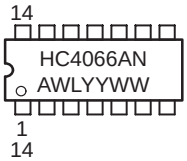
ON Semiconductor

http://onsemi.com

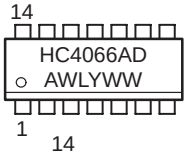
MARKING DIAGRAMS

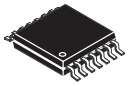


PDIP–14
N SUFFIX
CASE 646

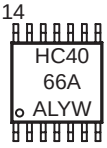


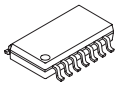
SOIC–14
D SUFFIX
CASE 751A



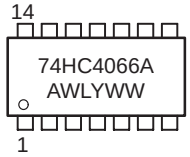


TSSOP–14
DT SUFFIX
CASE 948G



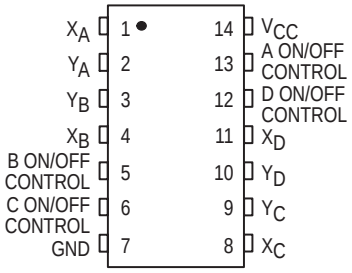


SOEIAJ–14
F SUFFIX
CASE 965



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HC4066AN	PDIP–14	2000 / Box
MC74HC4066AD	SOIC–14	55 / Rail
MC74HC4066ADR2	SOIC–14	2500 / Reel
MC74HC4066ADT	TSSOP–14	96 / Rail
MC74HC4066ADTR2	TSSOP–14	2500 / Reel
MC74HC4066AF	SOEIAJ–14	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	– 0.5 to + 14.0	V
V_{IS}	Analog Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current Into or Out of Any Pin	± 25	mA
P_D	Power Dissipation in Still Air, Plastic DIP† EIAJ/SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
EIAJ/SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	2.0	12.0	V
V_{IS}	Analog Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch	—	1.2	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time, ON/OFF Control Inputs (Figure 10)			ns
	V_{CC} = 2.0 V	0	1000	
	V_{CC} = 3.0 V	0	600	
	V_{CC} = 4.5 V	0	500	
	V_{CC} = 9.0 V	0	400	
	V_{CC} = 12.0 V	0	250	

*For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTIC Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit – 55 to 25°C	Guaranteed Limit ≤ 85°C	Guaranteed Limit ≤ 125°C	Unit
V_{IH}	Minimum High–Level Voltage ON/OFF Control Inputs	R_{on} = Per Spec	2.0 3.0 4.5 9.0 12.0	1.5 2.1 3.15 6.3 8.4	1.5 2.1 3.15 6.3 8.4	1.5 2.1 3.15 6.3 8.4	V
V_{IL}	Maximum Low–Level Voltage ON/OFF Control Inputs	R_{on} = Per Spec	2.0 3.0 4.5 9.0 12.0	0.5 0.9 1.35 2.7 3.6	0.5 0.9 1.35 2.7 3.6	0.5 0.9 1.35 2.7 3.6	V
I_{in}	Maximum Input Leakage Current ON/OFF Control Inputs	V_{in} = V_{CC} or GND	12.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND V_{IO} = 0 V	6.0 12.0	2 4	20 40	40 160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
R_{on}	Maximum "ON" Resistance	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ to GND $I_S \leq 2.0$ mA (Figures 1, 2)	2.0† 3.0† 4.5 9.0 12.0	— — 120 70 70	— — 160 85 85	— — 200 100 100	Ω
		$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ or GND (Endpoints) $I_S \leq 2.0$ mA (Figures 1, 2)	2.0 3.0 4.5 9.0 12.0	— — 70 50 30	— — 85 60 60	— — 100 80 80	
ΔR_{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{in} = V_{IH}$ V_{IS} = 1/2 (V_{CC} – GND) $I_S \leq 2.0$ mA	2.0 4.5 9.0 12.0	— 20 15 15	— 25 20 20	— 30 25 25	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	$V_{in} = V_{IL}$ $V_{IO} = V_{CC}$ or GND Switch Off (Figure 3)	12.0	0.1	0.5	1.0	μA
I_{on}	Maximum On–Channel Leakage Current, Any One Channel	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ or GND (Figure 4)	12.0	0.1	0.5	1.0	μA

†At supply voltage (V_{CC}) approaching 3 V the analog switch–on resistance becomes extremely non–linear. Therefore, for low–voltage operation, it is recommended that these devices only be used to control digital signals.

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, ON/OFF Control Inputs: $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figures 8 and 9)	2.0 3.0 4.5 9.0 12.0	40 30 5 5 5	50 40 7 7 7	60 50 8 8 8	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 11)	2.0 3.0 4.5 9.0 12.0	80 60 20 20 20	90 70 25 25 25	110 80 35 35 35	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 1 1)	2.0 3.0 4.5 9.0 12.0	80 45 20 20 20	90 50 25 25 25	100 60 30 30 30	ns
C	Maximum Capacitance — ON/OFF Control Input	—	10	10	10	pF
	Control Input = GND Analog I/O Feedthrough	— —	35 1.0	35 1.0	35 1.0	

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Switch) (Figure 13)*	15	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Test Conditions	V_{CC} V	Limit* 25°C 54/74HC	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 5)	f_{in} = 1 MHz Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{OS} Increase f_{in} Frequency Until dB Meter Reads – 3 dB R_L = 50 Ω, C_L = 10 pF	4.5 9.0 12.0	150 160 160	MHz
—	Off–Channel Feedthrough Isolation (Figure 6)	f_{in} ≡ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	4.5 9.0 12.0	– 50 – 50 – 50	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	4.5 9.0 12.0	– 40 – 40 – 40	
—	Feedthrough Noise, Control to Switch (Figure 7)	V_{in} ≤ 1 MHz Square Wave (t_r = t_f = 6 ns) Adjust R_L at Setup so that I_S = 0 A R_L = 600 Ω, C_L = 50 pF	4.5 9.0 12.0	60 130 200	mV_{PP}
		R_L = 10 kΩ, C_L = 10 pF	4.5 9.0 12.0	30 65 100	
—	Crosstalk Between Any Two Switches (Figure 12)	f_{in} ≡ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	4.5 9.0 12.0	– 70 – 70 – 70	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	4.5 9.0 12.0	– 80 – 80 – 80	
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1 kHz, R_L = 10 kΩ, C_L = 50 pF $THD = THD_{Measured} - THD_{Source}$ V_{IS} = 4.0 V_{PP} sine wave V_{IS} = 8.0 V_{PP} sine wave V_{IS} = 11.0 V_{PP} sine wave	 4.5 9.0 12.0	 0.10 0.06 0.04	%

*Guaranteed limits not tested. Determined by design and verified by qualification.

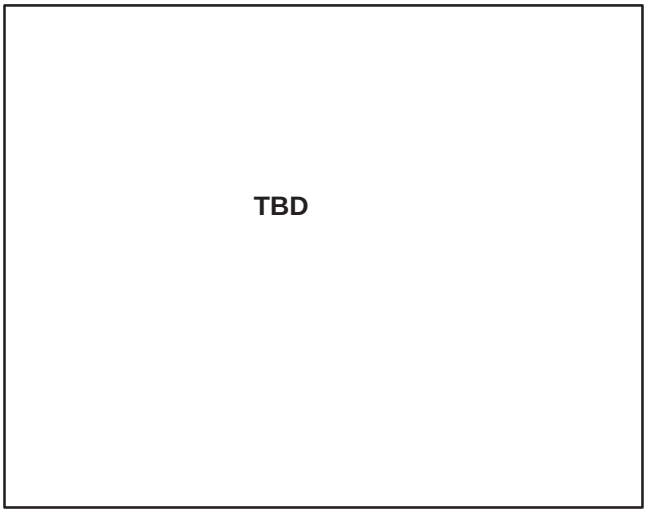


Figure 1a. Typical On Resistance, V_{CC} = 2.0 V

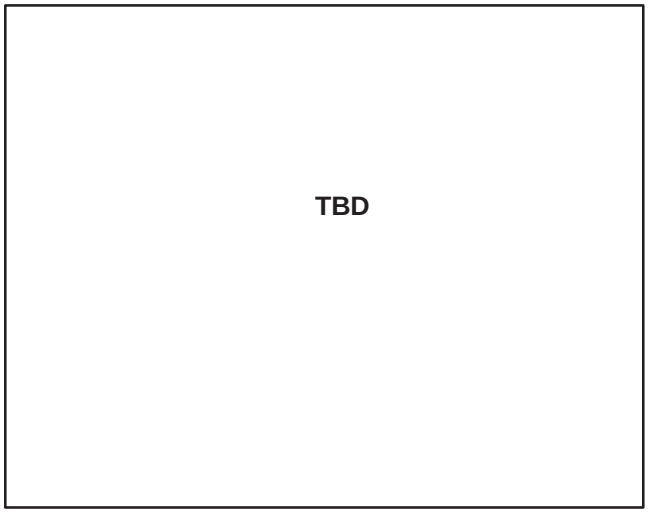


Figure 1b. Typical On Resistance, V_{CC} = 4.5 V

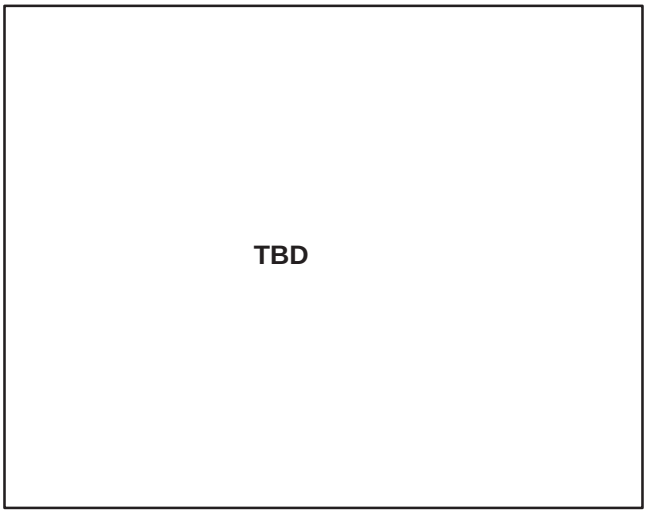


Figure 1c. Typical On Resistance, V_{CC} = 6.0 V

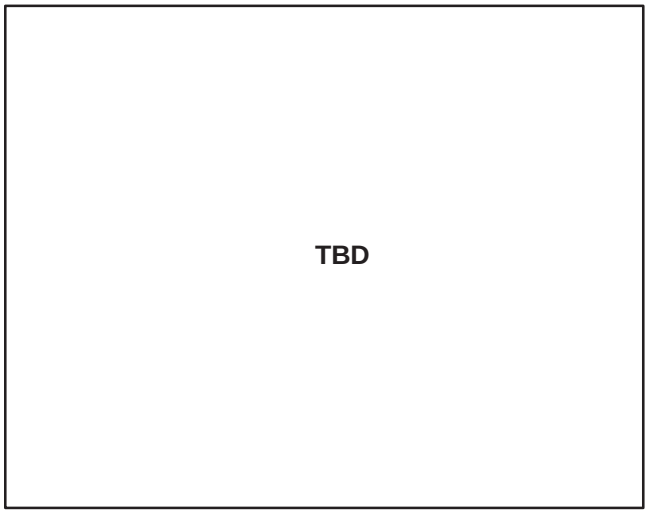


Figure 1d. Typical On Resistance, V_{CC} = 9.0 V

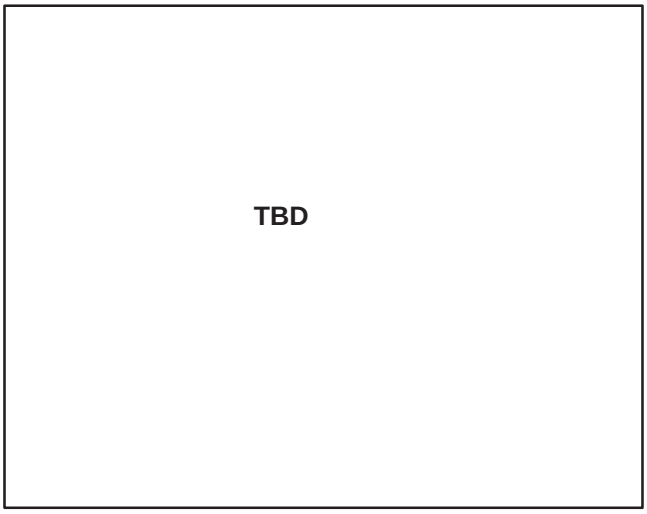


Figure 1e. Typical On Resistance, V_{CC} = 12 V

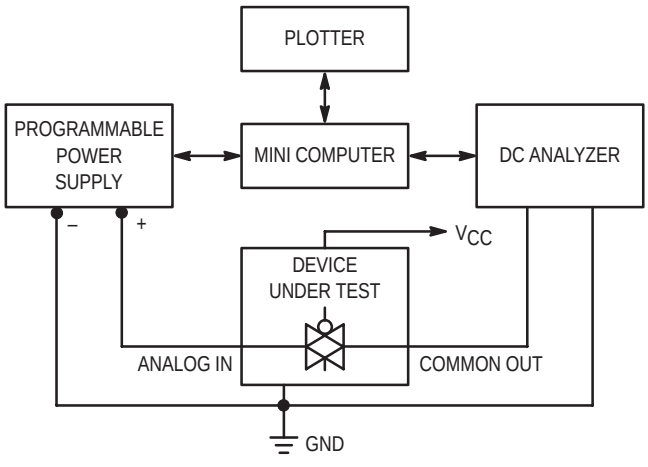


Figure 2. On Resistance Test Set–Up

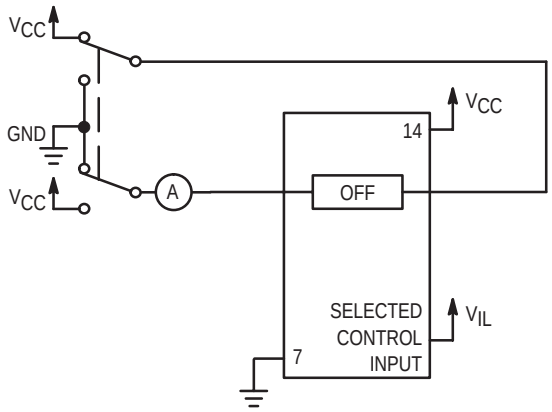


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

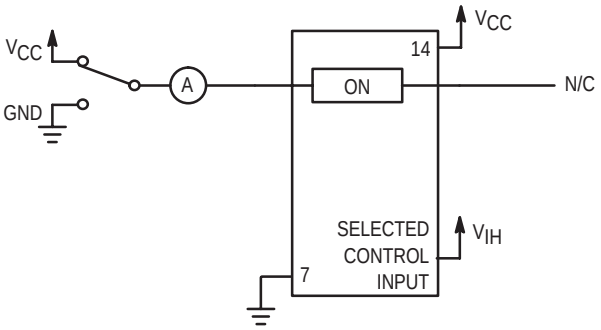
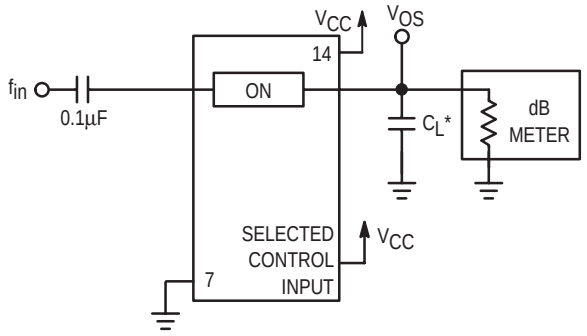
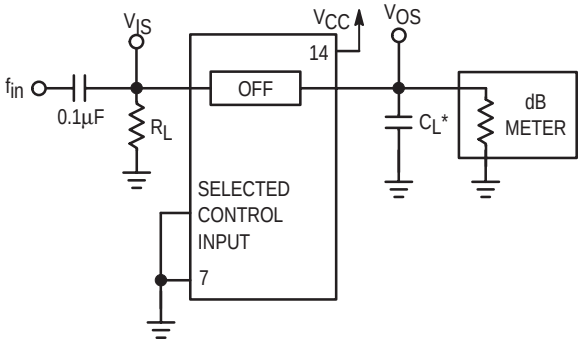


Figure 4. Maximum On Channel Leakage Current, Test Set–Up



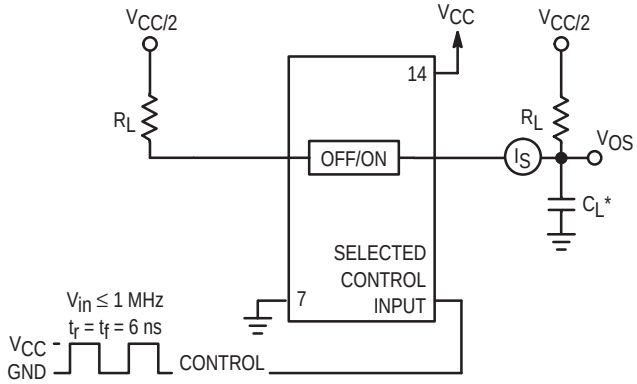
*Includes all probe and jig capacitance.

Figure 5. Maximum On–Channel Bandwidth Test Set–Up



*Includes all probe and jig capacitance.

Figure 6. Off–Channel Feedthrough Isolation, Test Set–Up



*Includes all probe and jig capacitance.

Figure 7. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set–Up

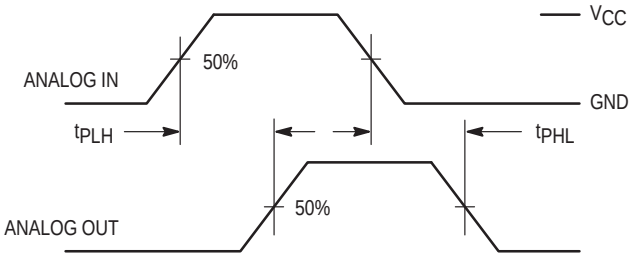
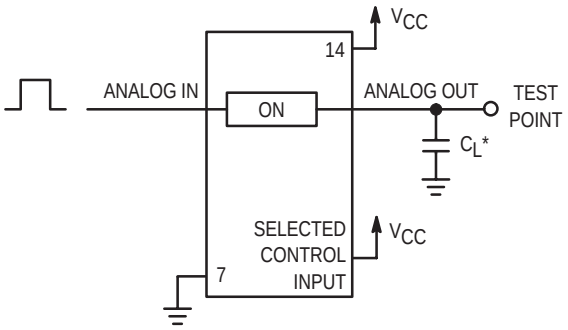


Figure 8. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance.

Figure 9. Propagation Delay Test Set–Up

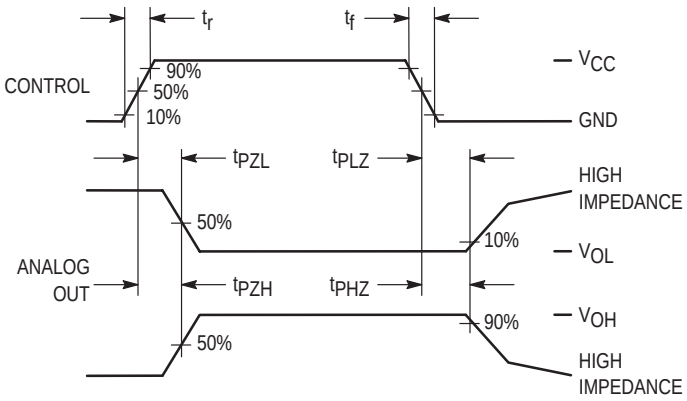
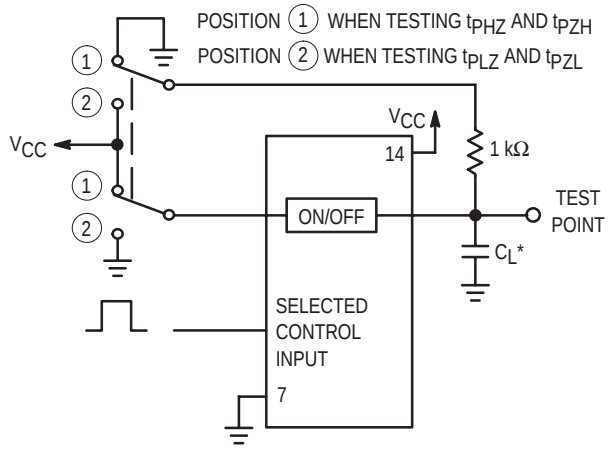
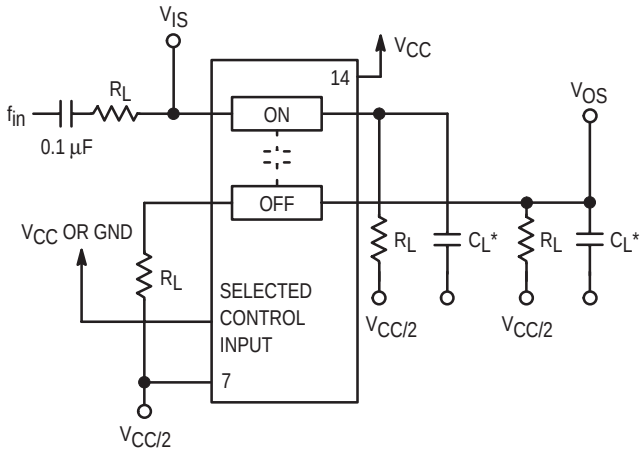


Figure 10. Propagation Delay, ON/OFF Control to Analog Out



*Includes all probe and jig capacitance.

Figure 11. Propagation Delay Test Set–Up



*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set–Up

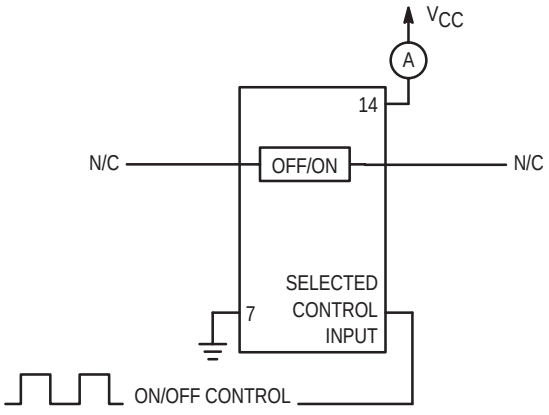
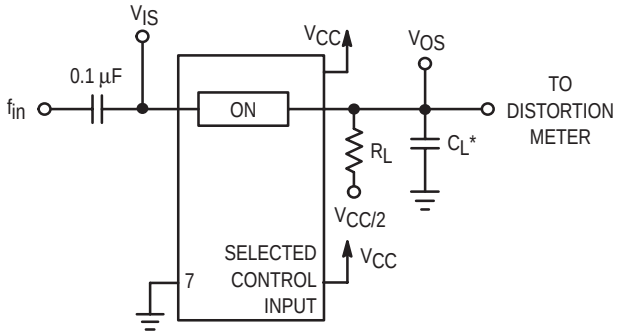


Figure 13. Power Dissipation Capacitance Test Set–Up



*Includes all probe and jig capacitance.

Figure 14. Total Harmonic Distortion, Test Set–Up

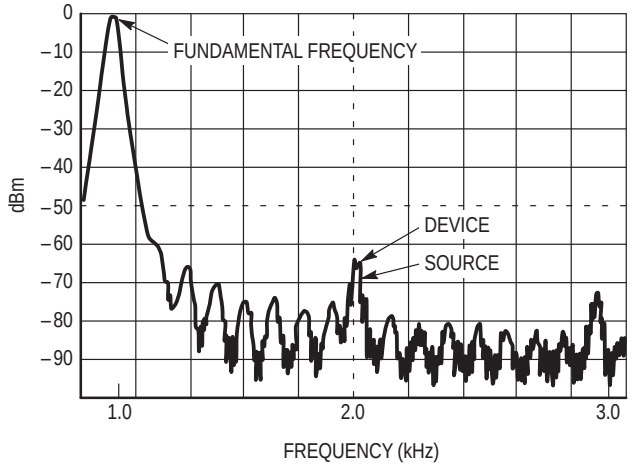


Figure 15. Plot, Harmonic Distortion

APPLICATION INFORMATION

The ON/OFF Control pins should be at V_{CC} or GND logic levels, V_{CC} being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to V_{CC} or GND through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked–up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages V_{CC} and GND. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below GND. In the example below, the difference between V_{CC} and GND is twelve volts. Therefore, using the configuration in Figure 16, a maximum analog signal of twelve volts peak–to–peak can be controlled.

When voltage transients above V_{CC} and/or below GND are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure 17. These diodes should be small signal, fast turn–on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the Dx diodes with Mosorbs (Mosorb™ is an acronym for high current surge protectors). Mosorbs are fast turn–on devices ideally suited for precise DC protection with no inherent wear out mechanism.

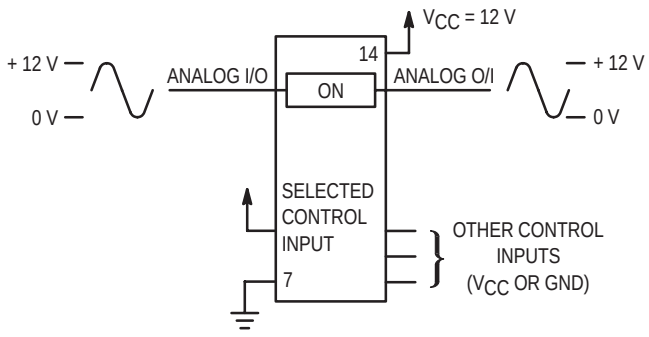


Figure 16. 12 V Application

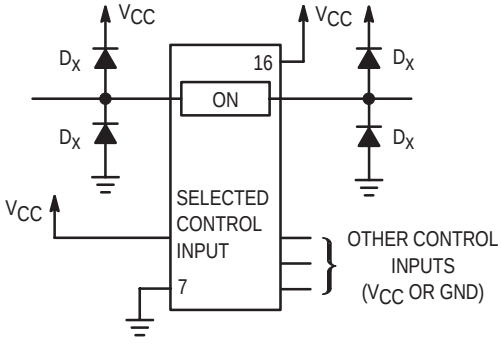
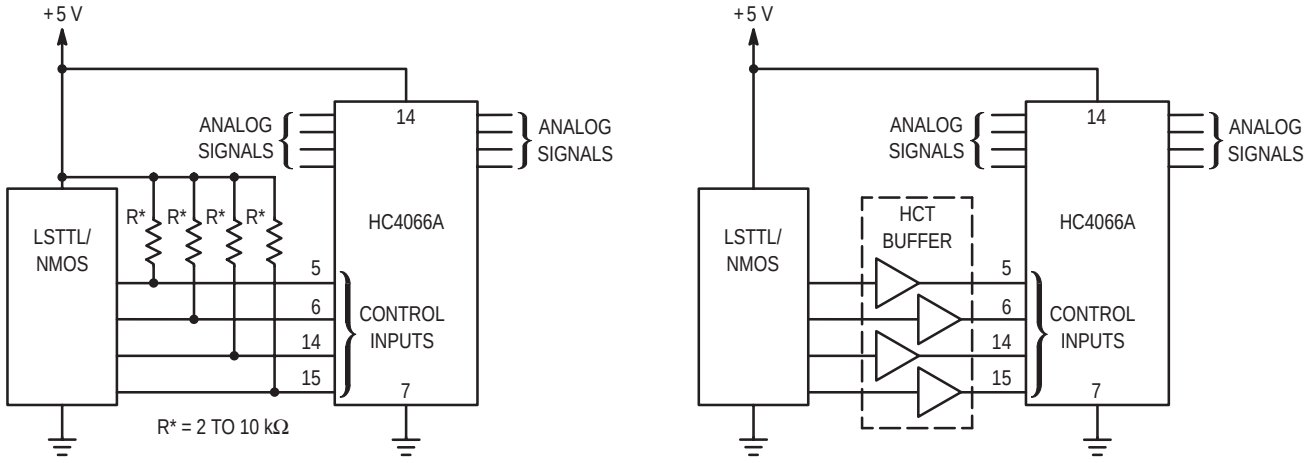


Figure 17. Transient Suppressor Application



a. Using Pull-Up Resistors **b. Using HCT Buffer**

Figure 18. LSTTL/NMOS to HCMOS Interface

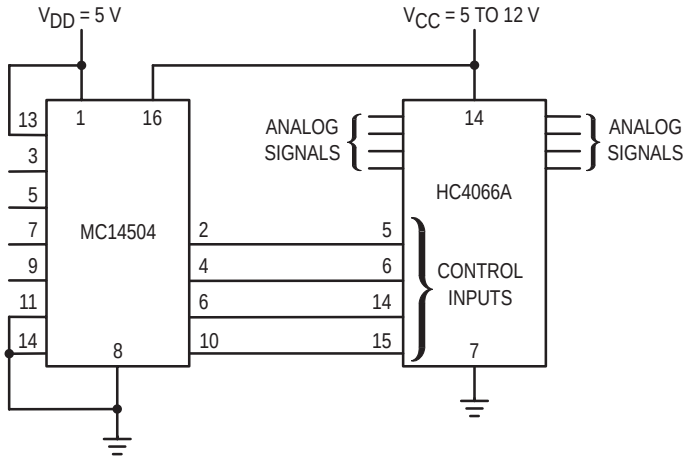


Figure 19. TTL/NMOS–to–CMOS Level Converter Analog Signal Peak–to–Peak Greater than 5 V (Also see HC4316A)

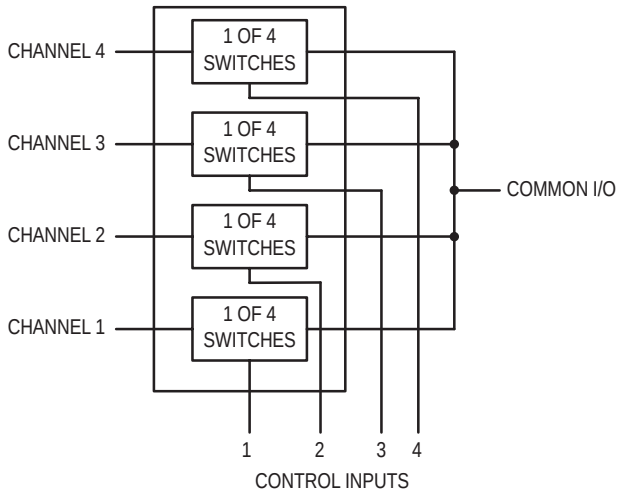


Figure 20. 4–Input Multiplexer

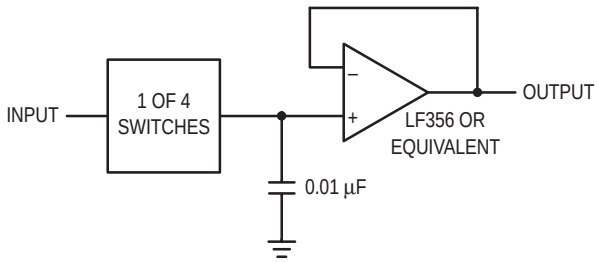


Figure 21. Sample/Hold Amplifier

MC74HC4316A

Product Preview

Quad Analog Switch/ Multiplexer/Demultiplexer with Separate Analog and Digital Power Supplies

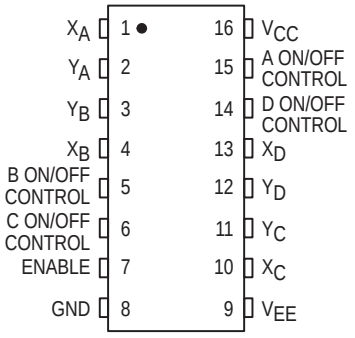
High–Performance Silicon–Gate CMOS

The MC74HC4316A utilizes silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF–channel leakage current. This bilateral switch/multiplexer/ demultiplexer controls analog and digital voltages that may vary across the full analog power–supply range (from V_{CC} to V_{EE}).

The HC4316A is similar in function to the metal–gate CMOS MC14016 and MC14066, and to the High–Speed CMOS HC4066A. Each device has four independent switches. The device control and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. The device has been designed so that the ON resistances (R_{ON}) are much more linear over input voltage than R_{ON} of metal–gate CMOS analog switches. Logic–level translators are provided so that the On/Off Control and Enable logic–level voltages need only be V_{CC} and GND, while the switch is passing signals ranging between V_{CC} and V_{EE}. When the Enable pin (active–low) is high, all four analog switches are turned off.

- Logic–Level Translator for On/Off Control and Enable Inputs
- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Diode Protection on All Inputs/Outputs
- Analog Power–Supply Voltage Range ($V_{CC} – V_{EE}$) = 2.0 to 12.0 Volts
- Digital (Control) Power–Supply Voltage Range (V_{CC} – GND) = 2.0 to 6.0 Volts, Independent of V_{EE}
- Improved Linearity of ON Resistance
- Chip Complexity: 66 FETs or 16.5 Equivalent Gates

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		State of Analog Switch
Enable	On/Off Control	
L	H	On
L	L	Off
H	X	Off

X = don't care

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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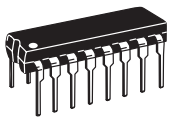
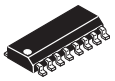
http://onsemi.com

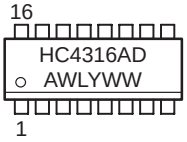
MARKING DIAGRAMS

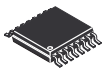


PDIP–16
P SUFFIX
CASE 648

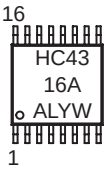


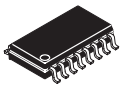
SOIC–16
D SUFFIX
CASE 751B



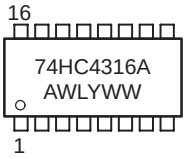


TSSOP–16
DT SUFFIX
CASE 948F





SOEIAJ–16
F SUFFIX
CASE 966



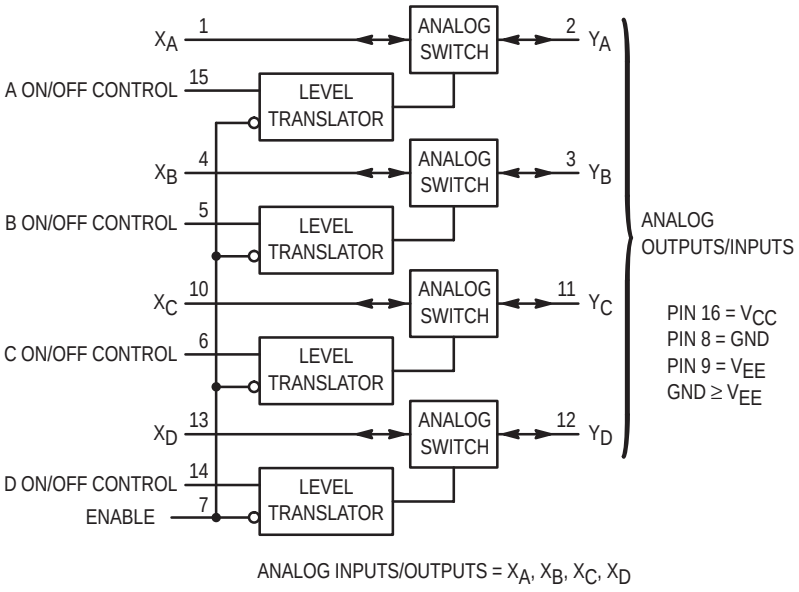
A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74HC4316AN	PDIP–16	2000 / Box
MC74HC4316AD	SOIC–16	48 / Rail
MC74HC4316ADR2	SOIC–16	2500 / Reel
MC74HC4316ADT	TSSOP–16	96 / Rail
MC74HC4316ADTR2	TSSOP–16	2500 / Reel
MC74HC4316AF	SOEIAJ–14	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

LOGIC DIAGRAM



ANALOG INPUTS/OUTPUTS = X_A, X_B, X_C, X_D

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Ref. to GND) (Ref. to V_{EE})	– 0.5 to + 7.0 – 0.5 to + 14.0	V
V_{EE}	Negative DC Supply Voltage (Ref. to GND)	– 7.0 to + 0.5	V
V_{IS}	Analog Input Voltage	V_{EE} – 0.5 to V_{CC} + 0.5	V
V_{in}	DC Input Voltage (Ref. to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current Into or Out of Any Pin	± 25	mA
P_D	Power Dissipation in Still Air Plastic DIP† EIAJ/SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
EIAJ/SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Ref. to GND)		2.0	6.0	V
V_{EE}	Negative DC Supply Voltage (Ref. to GND)		– 6.0	GND	V
V_{IS}	Analog Input Voltage		V_{EE}	V_{CC}	V
V_{in}	Digital Input Voltage (Ref. to GND)		GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		—	1.2	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Control or Enable Inputs) (Figure 10)	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

*For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND) V_{EE} = GND Except Where Noted

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Voltage, Control or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Voltage, Control or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
I_{in}	Maximum Input Leakage Current, Control or Enable Inputs	V_{in} = V_{CC} or GND V_{EE} = – 6.0 V	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND V_{IO} = 0 V V_{EE} = GND V_{EE} = – 6.0	 6.0 6.0	 2 4	 20 40	 40 160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to V_{EE})

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Guaranteed Limit			Unit
					– 55 to 25°C	≤ 85°C	≤ 125°C	
R_{on}	Maximum "ON" Resistance	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ to V_{EE} $I_S \leq 2.0$ mA (Figures 1, 2)	2.0* 4 5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	— 160 90 90	— 200 110 110	— 240 130 130	Ω
		$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ or V_{EE} (Endpoints) $I_S \leq 2.0$ mA (Figures 1, 2)	2.0 4.5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	— 90 70 70	— 115 90 90	— 140 105 105	
ΔR_{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{in} = V_{IH}$ $V_{IS} = 1/2\ (V_{CC} - V_{EE})$ $I_S \leq 2.0$ mA	2.0 4.5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	— 20 15 15	— 25 20 20	— 30 25 25	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	$V_{in} = V_{IL}$ $V_{IO} = V_{CC}$ or V_{EE} Switch Off (Figure 3)	6.0	– 6.0	0.1	0.5	1.0	μA
I_{on}	Maximum On–Channel Leakage Current, Any One Channel	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ or V_{EE} (Figure 4)	6.0	– 6.0	0.1	0.5	1.0	μA

*At supply voltage ($V_{CC} - V_{EE}$) approaching 2 V the analog switch–on resistance becomes extremely non–linear. Therefore, for low–voltage operation, it is recommended that these devices only be used to control digital signals.

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Control or Enable $t_r = t_f$ = 6 ns, V_{EE} = GND)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figures 8 and 9)	2.0 4.5 6.0	40 6 5	50 8 7	60 9 8	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Control or Enable to Analog Output (Figures 10 and 11)	2.0 4.5 6.0	130 40 30	160 50 40	200 60 50	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Control or Enable to Analog Output (Figures 10 and 11)	2.0 4.5 6.0	140 40 30	175 50 40	250 60 50	ns
C	Maximum Capacitance — ON/OFF Control and Enable Inputs	—	10	10	10	pF
	Control Input = GND					
	Analog I/O	—	35	35	35	
	Feedthrough	—	1.0	1.0	1.0	

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Switch) (Figure 13)*	15	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Limit* 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 5)	f_{in} = 1 MHz Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{OS} Increase f_{in} Frequency Until dB Meter Reads – 3 dB R_L = 50 Ω, C_L = 10 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	150 160 160	MHz
—	Off–Channel Feedthrough Isolation (Figure 6)	f_{in} ≡ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 50 – 50 – 50	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 40 – 40 – 40	
—	Feedthrough Noise, Control to Switch (Figure 7)	V_{in} ≤ 1 MHz Square Wave (t_r = t_f = 6 ns) Adjust R_L at Setup so that I_S = 0 A R_L = 600 Ω, C_L = 50 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	60 130 200	mV_{PP}
		R_L = 10 kΩ, C_L = 10 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	30 65 100	
—	Crosstalk Between Any Two Switches (Figure 12)	f_{in} ≡ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 70 – 70 – 70	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 80 – 80 – 80	
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1 kHz, R_L = 10 kΩ, C_L = 50 pF $THD = THD_{Measured} - THD_{Source}$ V_{IS} = 4.0 V_{PP} sine wave V_{IS} = 8.0 V_{PP} sine wave V_{IS} = 11.0 V_{PP} sine wave	 2.25 4.50 6.00	 – 2.25 – 4.50 – 6.00	 0.10 0.06 0.04	%

*Limits not tested. Determined by design and verified by qualification.

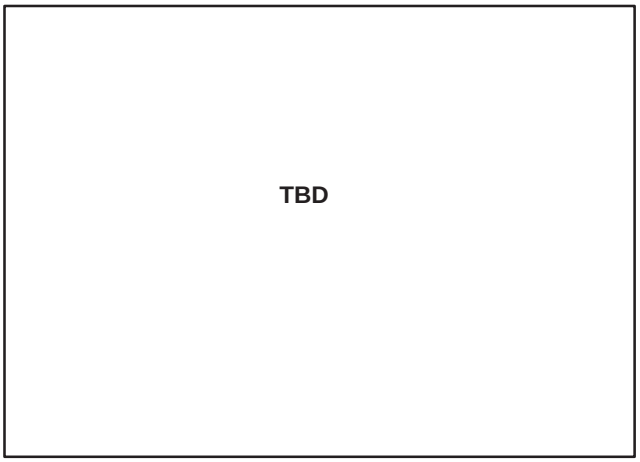


Figure 1a. Typical On Resistance,
$V_{CC} - V_{EE}$ = 2.0 V

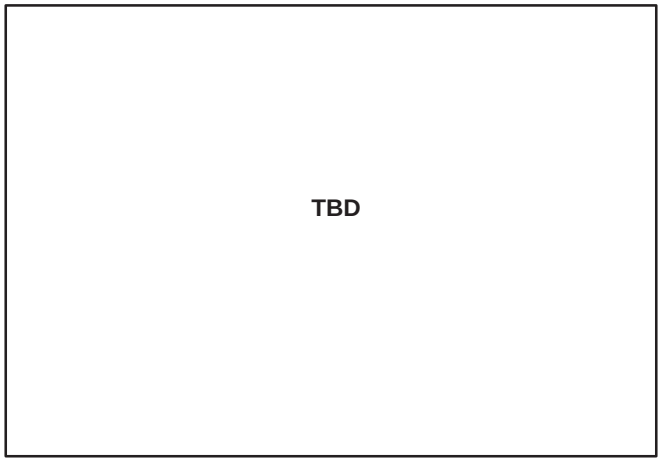


Figure 1b. Typical On Resistance,
$V_{CC} - V_{EE}$ = 4.5 V

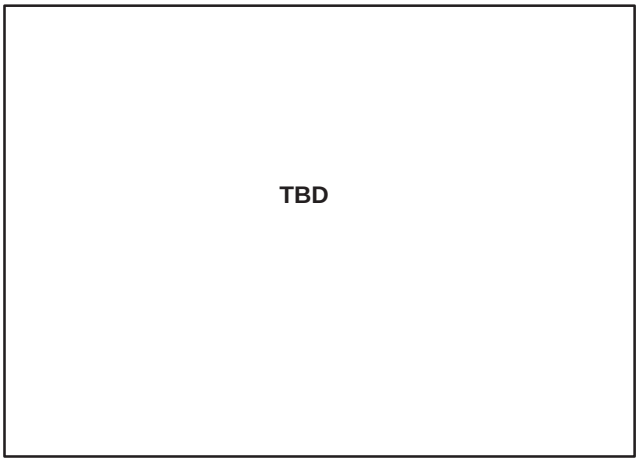


Figure 1c. Typical On Resistance,
$V_{CC} - V_{EE}$ = 6.0 V

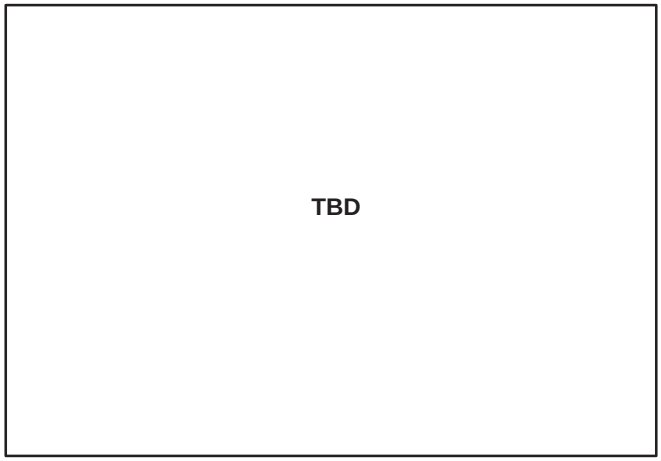


Figure 1d. Typical On Resistance,
$V_{CC} - V_{EE}$ = 9.0 V

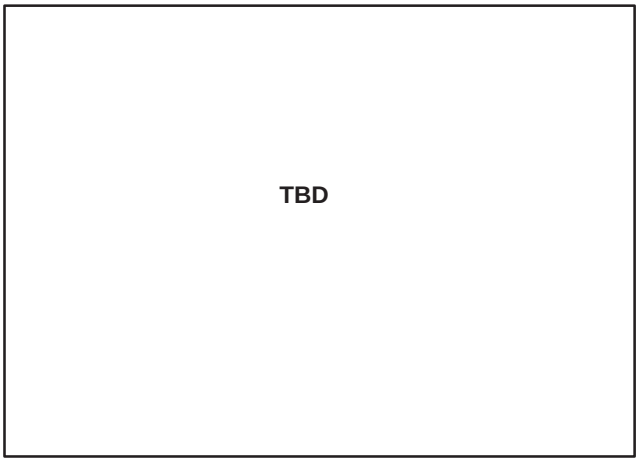


Figure 1e. Typical On Resistance,
$V_{CC} - V_{EE}$ = 12.0 V

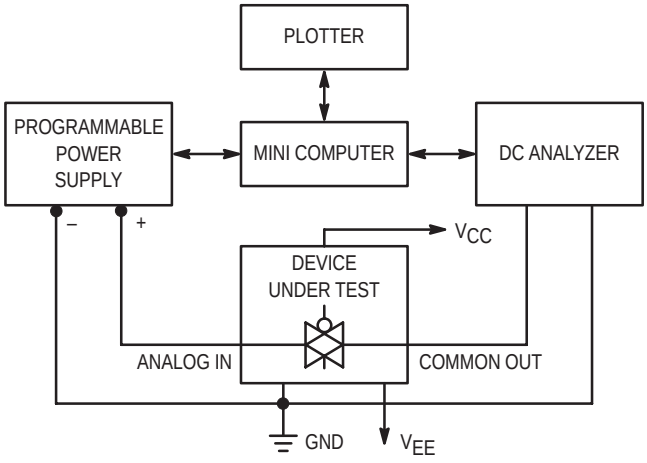


Figure 2. On Resistance Test Set–Up

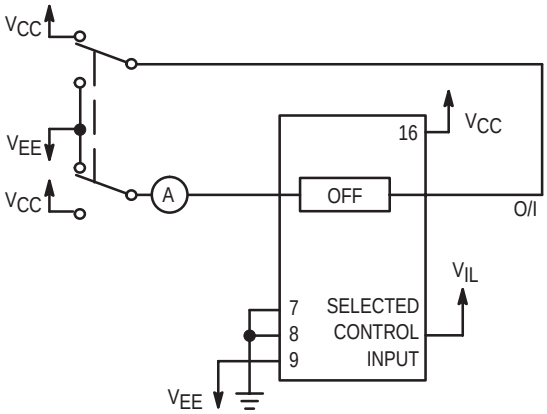


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

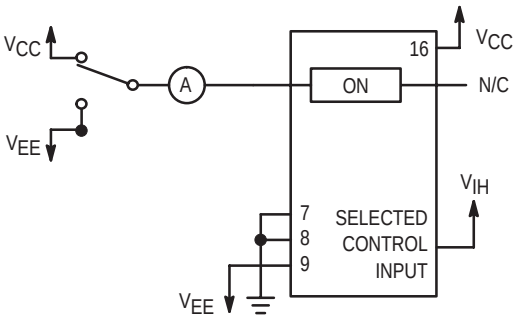
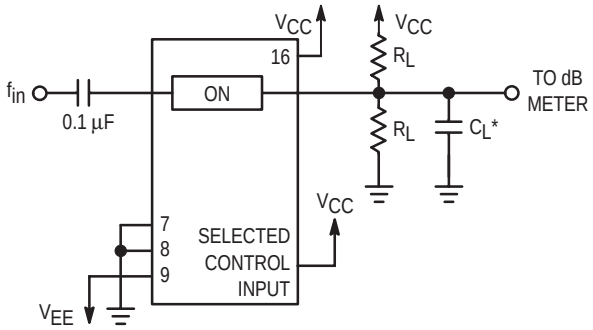
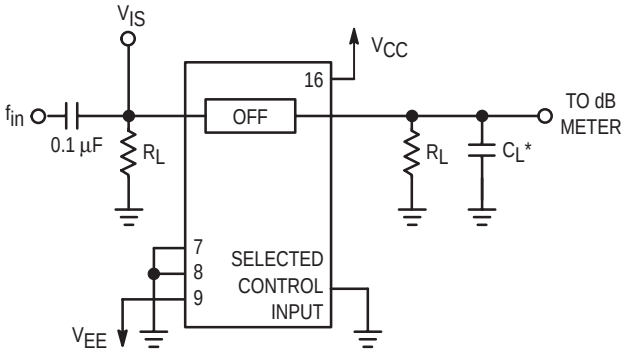


Figure 4. Maximum On Channel Leakage Current, Test Set–Up



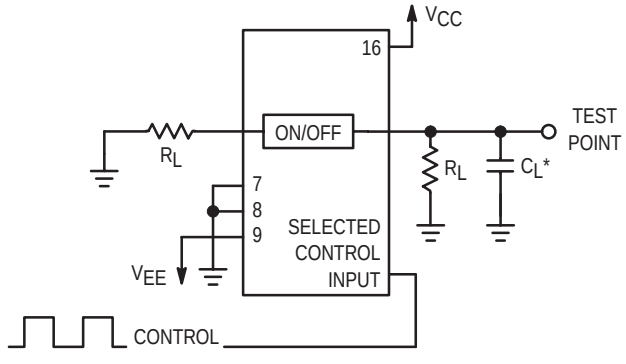
*Includes all probe and jig capacitance.

Figure 5. Maximum On–Channel Bandwidth Test Set–Up



*Includes all probe and jig capacitance.

Figure 6. Off–Channel Feedthrough Isolation, Test Set–Up



*Includes all probe and jig capacitance.

Figure 7. Feedthrough Noise, Control to Analog Out, Test Set–Up

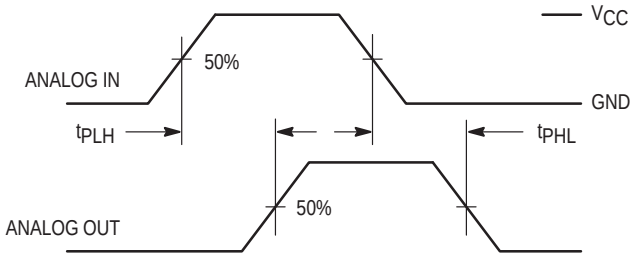
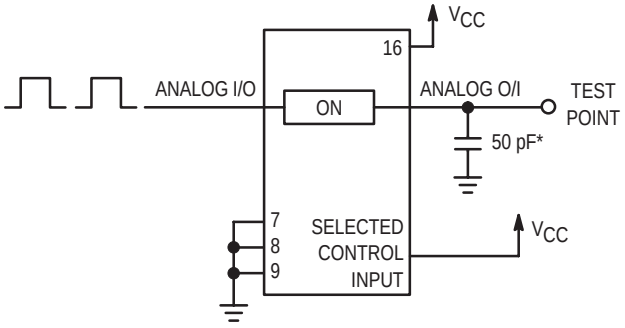


Figure 8. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance.

Figure 9. Propagation Delay Test Set–Up

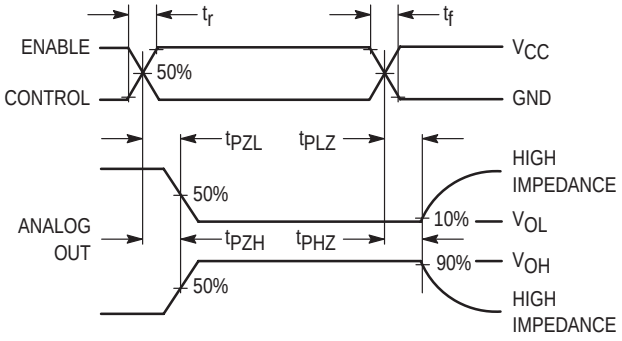
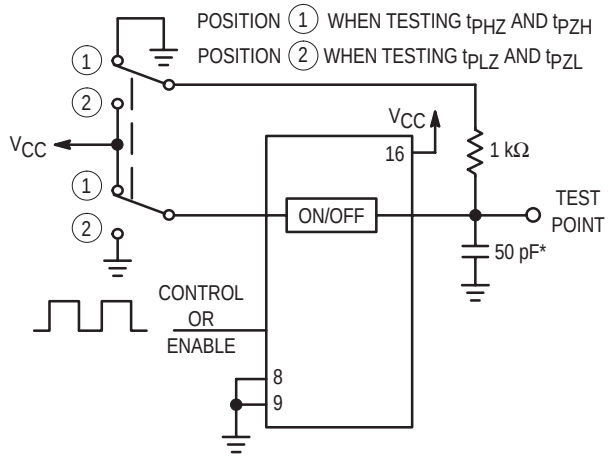
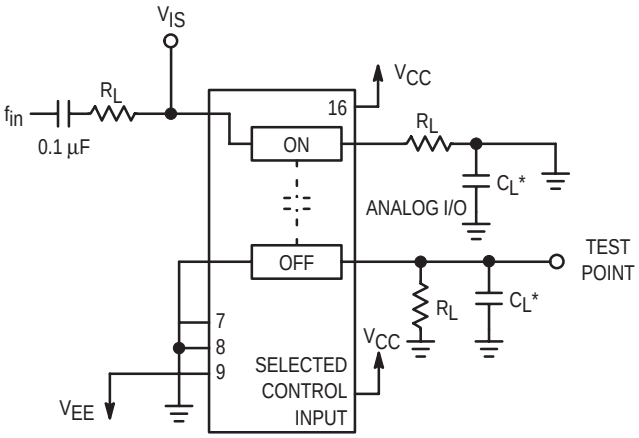


Figure 10. Propagation Delay, ON/OFF Control to Analog Out



*Includes all probe and jig capacitance.

Figure 11. Propagation Delay Test Set–Up



*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set–Up (Adjacent Channels Used)

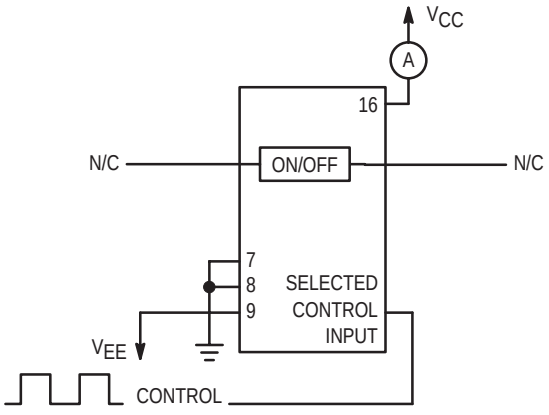
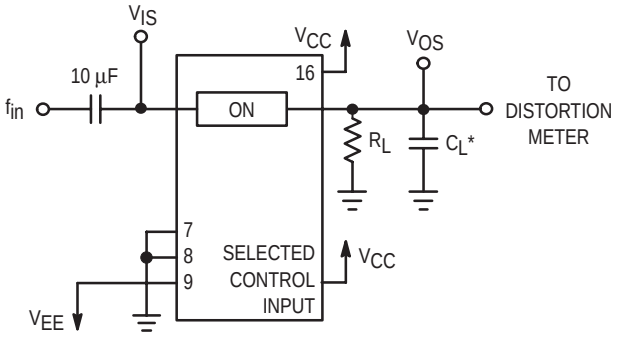


Figure 13. Power Dissipation Capacitance Test Set–Up



*Includes all probe and jig capacitance.

Figure 14. Total Harmonic Distortion, Test Set–Up

APPLICATIONS INFORMATION

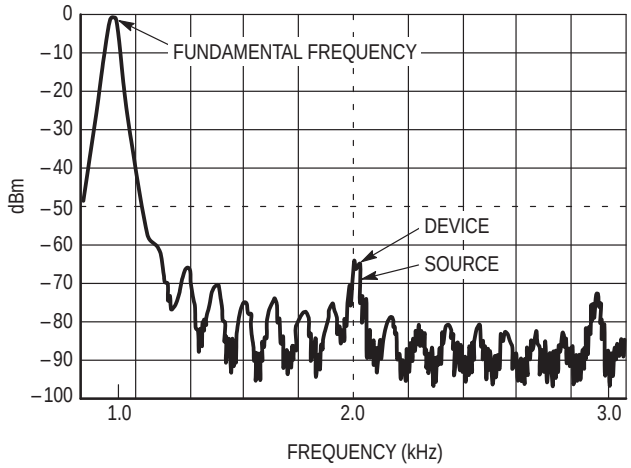


Figure 15. Plot, Harmonic Distortion

The Enable and Control pins should be at V_{CC} or GND logic levels, V_{CC} being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to V_{CC} or V_{EE} through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below V_{EE}. In the example below, the difference between V_{CC} and V_{EE} is twelve volts. Therefore, using the configuration in Figure 16, a maximum analog signal of twelve volts peak–to–peak can be controlled.

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure 17. These diodes should be small signal, fast turn–on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the Dx diodes with Mosorbs (Mosorb™ is an acronym for high current surge protectors). Mosorbs are fast turn–on devices ideally suited for precise dc protection with no inherent wear out mechanism.

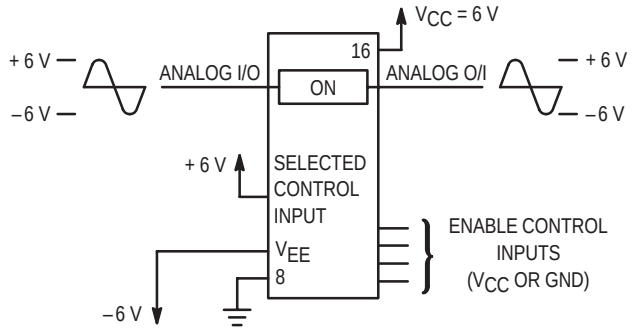


Figure 16.

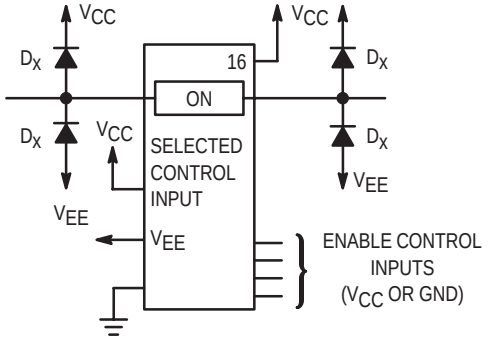
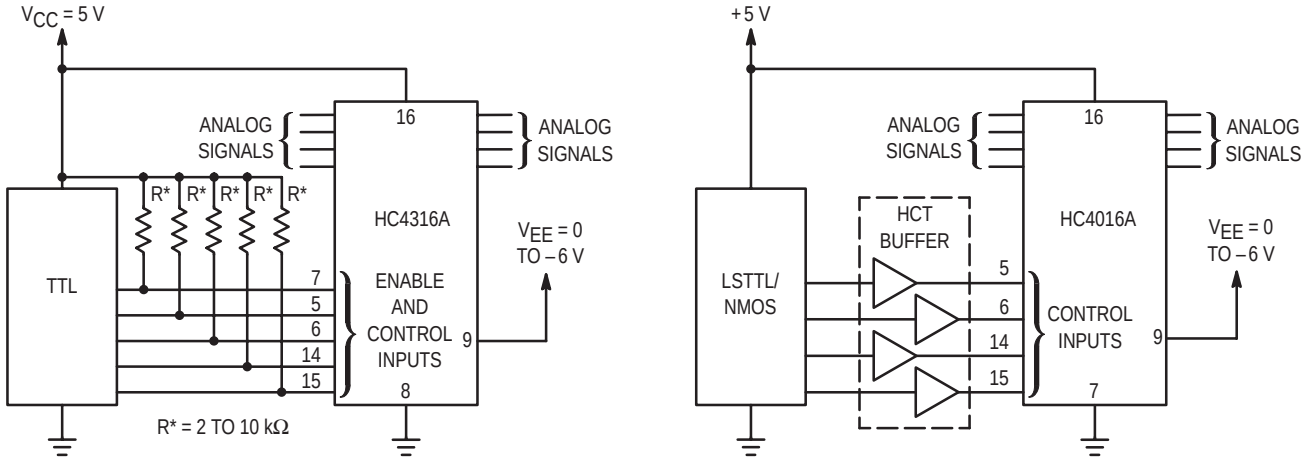


Figure 17. Transient Suppressor Application



a. Using Pull–Up Resistors **b. Using HCT Buffer**

Figure 18. LSTTL/NMOS to HCMOS Interface

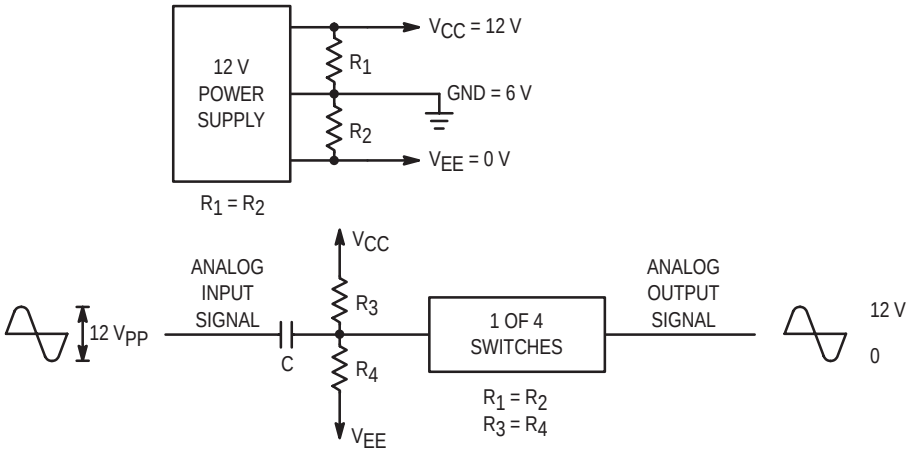


Figure 19. Switching a 0–to–12 V Signal Using a Single Power Supply (GND ≠ 0 V)

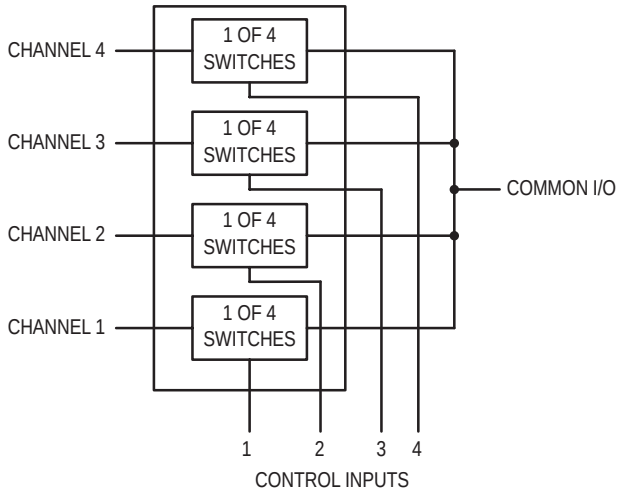


Figure 20. 4–Input Multiplexer

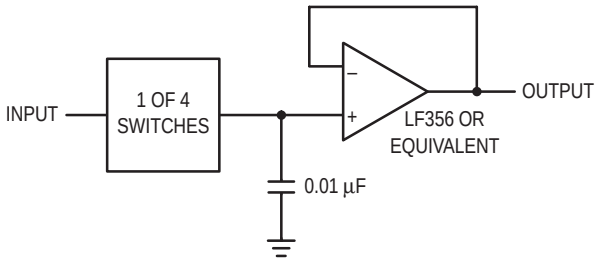


Figure 21. Sample/Hold Amplifier

MC74HC4538A

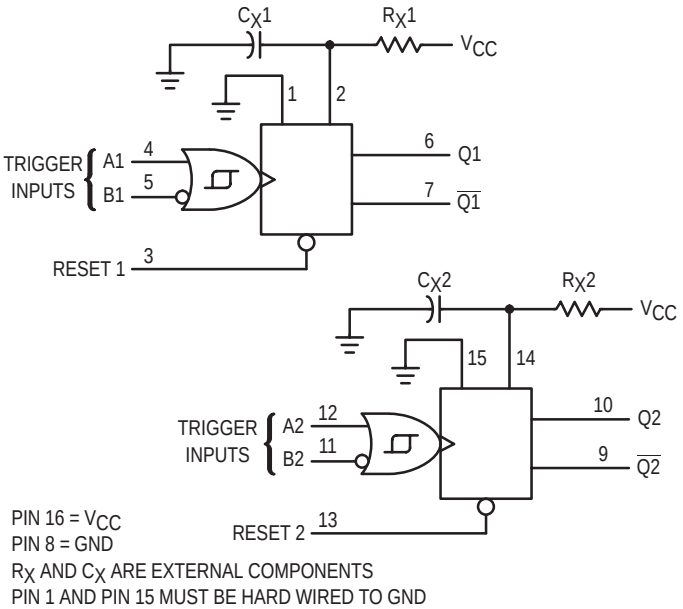
Dual Precision Monostable Multivibrator (Retriggerable, Resettable)

The MC74HC4538A is identical in pinout to the MC14538B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This dual monostable multivibrator may be triggered by either the positive or the negative edge of an input pulse, and produces a precision output pulse over a wide range of pulse widths. Because the device has conditioned trigger inputs, there are no trigger–input rise and fall time restrictions. The output pulse width is determined by the external timing components, R_X and C_X. The device has a reset function which forces the Q output low and the $\overline{Q}$ output high, regardless of the state of the output pulse circuitry.

- Unlimited Rise and Fall Times Allowed on the Trigger Inputs
- Output Pulse is Independent of the Trigger Pulse Width
- ± 10% Guaranteed Pulse Width Variation from Part to Part (Using the Same Test Jig)
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 3.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 145 FETs or 36 Equivalent Gates

LOGIC DIAGRAM



PIN 16 = V_{CC}
PIN 8 = GND
R_X AND C_X ARE EXTERNAL COMPONENTS
PIN 1 AND PIN 15 MUST BE HARD WIRED TO GND

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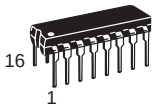
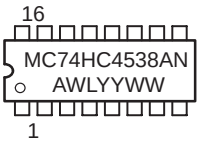
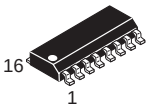
MARKING DIAGRAMS

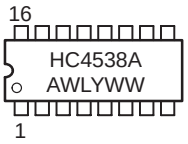


PDIP–16
N SUFFIX
CASE 648



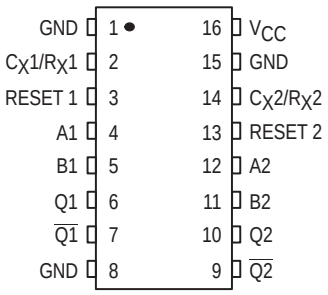


SO–16
D SUFFIX
CASE 751B



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs	
Reset	A	B	Q	$\overline{Q}$
H	↓	H	⊓	⊔
H	L	↘	⊓	⊔
H	X	L	Not Triggered	
H	H	X	Not Triggered	
H	L,H,↘	H	Not Triggered	
H	L	L,H,↓	Not Triggered	
L	X	X	L	H
↘ ↓	X	X	Not Triggered	

ORDERING INFORMATION

Device	Package	Shipping
MC74HC4538AN	PDIP–16	2000 / Box
MC74HC4538AD	SOIC–16	48 / Rail
MC74HC4538ADR2	SOIC–16	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 1.5 to V_{CC} + 1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	
I_{in}	DC Input Current, per Pin A, B, Reset C_X, R_X	± 20 ± 30	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0**	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time V_{CC} = 2.0 V (Figure 7) V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns
	A or B (Figure 5)	—	No Limit	
R_X	External Timing Resistor V_{CC} < 4.5 V V_{CC} ≥ 4.5 V	1.0 2.0	* *	kΩ
C_X	External Timing Capacitor	0	*	μF

* The maximum allowable values of R_X and C_X are a function of the leakage of capacitor C_X, the leakage of the HC4538A, and leakage due to board layout and surface resistance. For most applications, C_X/R_X should be limited to a maximum value of 10 μF/1.0 MΩ. Values of C_X > 1.0 μF may cause a problem during power down (see Power Down Considerations). Susceptibility to externally induced noise signals may occur for R_X > 1.0 MΩ.
** The HC4538A will function at 2.0 V but for optimum pulse width stability, V_{CC} should be above 3.0 V.
NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

DC CHARACTERISTICS FOR THE MC54/74HC4538A

Symbol	Parameter	Test Conditions	V_{CC} Volts	Guaranteed Limits						Unit
				– 55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	1.5 3.15 4.2		1.5 3.15 4.2		1.5 3.15 4.2		V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0		0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		1.9 4.4 5.9		V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq -4.0$ mA $\|I_{out}\| \leq -5.2$ mA	 4.5 6.0	 3.98 5.48		 3.84 5.34		 3.7 5.2		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0		0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	 4.5 6.0		 0.26 0.26		 0.33 0.33		 0.4 0.4	
I_{in}	Maximum Input Leakage Current (A, B, Reset)	V_{in} = V_{CC} or GND	6.0		± 0.1		± 1.0		± 1.0	μA
I_{in}	Maximum Input Leakage Current (R_X, C_X)	V_{in} = V_{CC} or GND	6.0		± 50		± 500		± 500	nA
I_{CC}	Maximum Quiescent Supply Current (per package) Standby State	V_{in} = V_{CC} or GND Q1 and Q2 = Low I_{out} = 0 μA	6.0		130		220		350	μA

I_{CC}	Maximum Supply Current (per package) Active State	V_{in} = V_{CC} or GND Q1 and Q2 = High I_{out} = 0 μA Pins 2 and 14 = 0.5 V_{CC}	6.0	25°C	400	– 45°C to 85°C	600	– 55°C to 125°C	800	μA

AC CHARACTERISTICS FOR THE MC54/74HC4538A (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} Volts	Guaranteed Limits						Unit
			– 55 to 25°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
t_{PLH}	Maximum Propagation Delay Input A or B to Q (Figures 6 and 8)	2.0 4.5 6.0		175 35 30		220 44 37		265 53 45	ns
t_{PHL}	Maximum Propagation Delay Input A or B to NQ (Figures 6 and 8)	2.0 4.5 6.0		195 39 33		245 49 42		295 59 50	ns
t_{PHL}	Maximum Propagation Delay Reset to Q (Figures 7 and 8)	2.0 4.5 6.0		175 35 30		220 44 37		265 53 45	ns
t_{PLH}	Maximum Propagation Delay Reset to NQ (Figures 7 and 8)	2.0 4.5 6.0		175 35 30		220 44 37		265 53 45	ns
t_{TLH} t_{THL}	Maximum Output Transition Time, Any Output (Figures 7 and 8)	2.0 4.5 6.0		75 15 13		95 19 16		110 22 19	ns
C_{in}	Maximum Input Capacitance (A. B, Reset) (C_X, R_X)	—		10 25		10 25		10 25	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Multivibrator)*	150	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING CHARACTERISTICS FOR THE MC54/74HC4538A (Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} Volts	Guaranteed Limits						Unit
			– 55 to 25°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
t_{rec}	Minimum Recovery Time, Inactive to A or B (Figure 7)	2.0 4.5 6.0	0 0 0		0 0 0		0 0 0		ns
t_w	Minimum Pulse Width, Input A or B (Figure 6)	2.0 4.5 6.0	60 12 10		75 15 13		90 18 15		ns
t_w	Minimum Pulse Width, Reset (Figure 7)	2.0 4.5 6.0	60 12 10		75 15 13		90 18 15		ns
t_r, t_f	Maximum Input Rise and Fall Times, Reset (Figure 7)	2.0 4.5 6.0		1000 500 400		1000 500 400		1000 500 400	ns
	A or B (Figure 7)	2.0 4.5 6.0	No Limit						

OUTPUT PULSE WIDTH CHARACTERISTICS (C_L = 50 pF)t

Symbol	Parameter	Conditions		Guaranteed Limits						Unit
				– 55 to 25°C		≤ 85°C		≤ 125°C		
		Timing Components	V_{CC} Volts	Min	Max	Min	Max	Min	Max	
τ	Output Pulse Width* (Figures 6 and 8)	R_X = 10 kΩ, C_X = 0.1 μF	5.0	0.63	0.77	0.6	0.8	0.59	0.81	ms
—	Pulse Width Match Between Circuits in the same Package	—	—	± 5.0						%
—	Pulse Width Match Variation (Part to Part)	—	—	± 10						%

*For output pulse widths greater than 100 μs, typically $\tau = kR_XC_X$, where the value of k may be found in Figure 1.

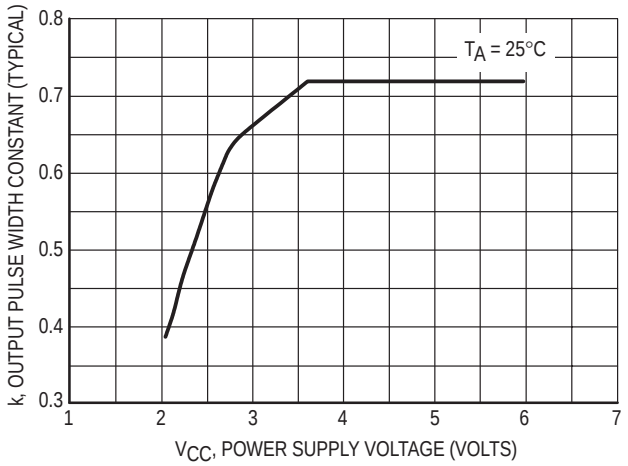


Figure 1. Typical Output Pulse Width Constant, k, versus Supply Voltage (For output pulse widths > 100 μs: $\tau = kR_XC_X$)

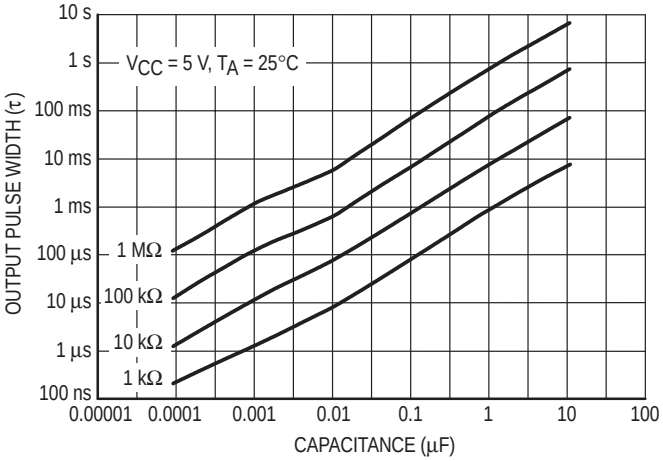


Figure 2. Output Pulse Width versus Timing Capacitance

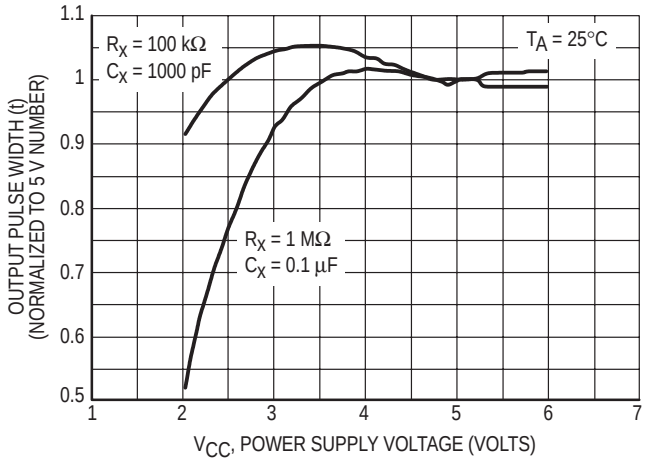


Figure 3. Normalized Output Pulse Width versus Power Supply Voltage

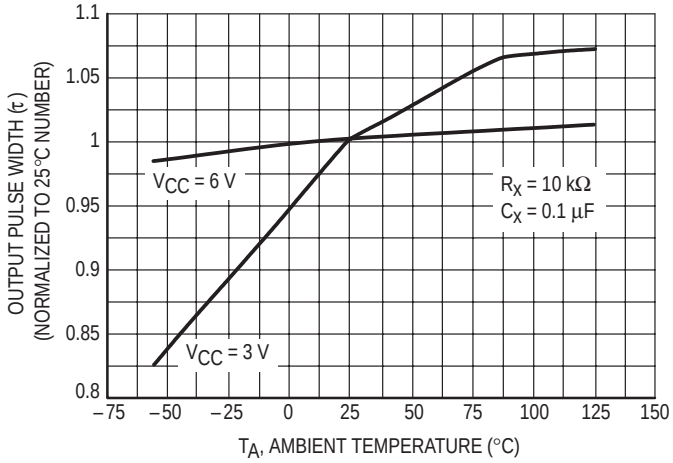


Figure 4. Normalized Output Pulse Width versus Power Supply Voltage

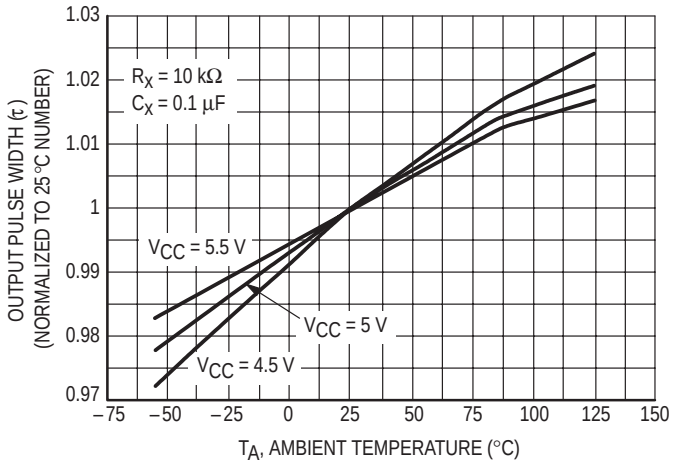


Figure 5. Normalized Output Pulse Width versus Power Supply Voltage

SWITCHING WAVEFORMS

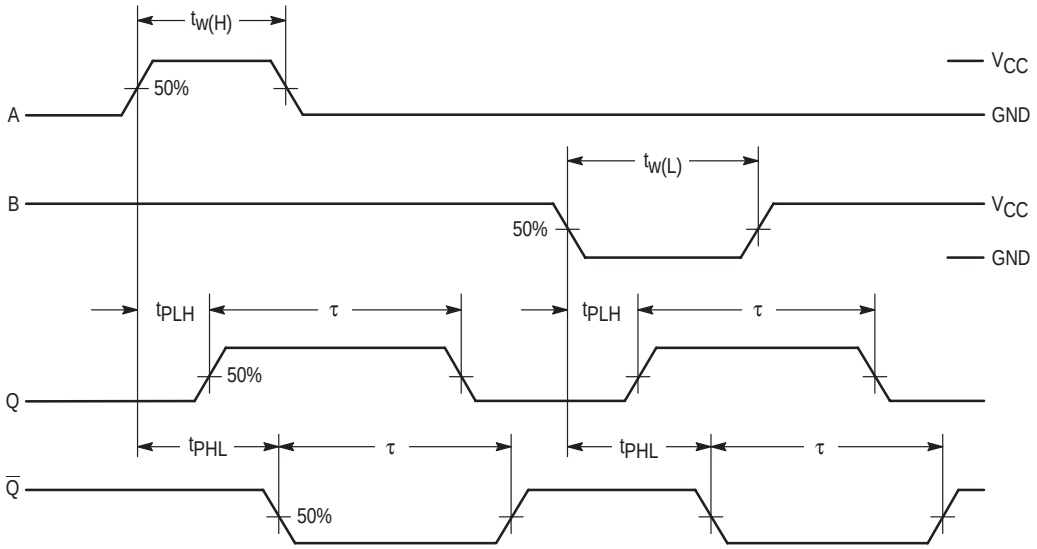


Figure 6.

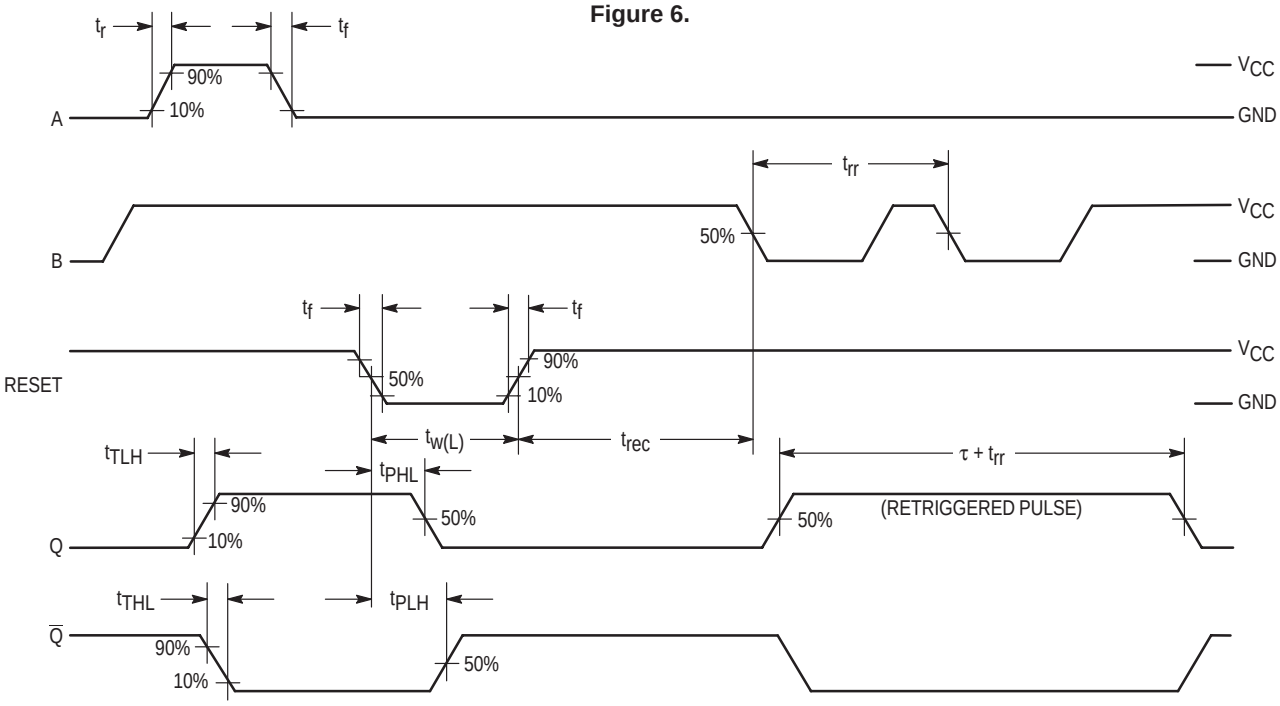
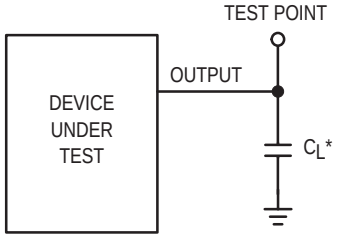


Figure 7.



*Includes all probe and jig capacitance

Figure 8. Test Circuit

PIN DESCRIPTIONS

INPUTS

A1, A2 (Pins 4, 12)

Positive–edge trigger inputs. A rising–edge signal on either of these pins triggers the corresponding multivibrator when there is a high level on the B1 or B2 input.

B1, B2 (Pins 5, 11)

Negative–edge trigger inputs. A falling–edge signal on either of these pins triggers the corresponding multivibrator when there is a low level on the A1 or A2 input.

Reset 1, Reset 2 (Pins 3, 13)

Reset inputs (active low). When a low level is applied to one of these pins, the Q output of the corresponding multivibrator is reset to a low level and the $\overline{Q}$ output is set to a high level.

C_X1/R_X1 and C_X2/R_X2 (Pins 2 and 14)

External timing components. These pins are tied to the common points of the external timing resistors and capacitors (see the Block Diagram). Polystyrene capacitors are recommended for optimum pulse width control. Electrolytic capacitors are not recommended due to high leakages associated with these type capacitors.

GND (Pins 1 and 15)

External ground. The external timing capacitors discharge to ground through these pins.

OUTPUTS

Q1, Q2 (Pins 6, 10)

Noninverted monostable outputs. These pins (normally low) pulse high when the multivibrator is triggered at either the A or the B input. The width of the pulse is determined by the external timing components, R_X and C_X.

$\overline{Q1}$, $\overline{Q2}$ (Pins 7, 9)

Inverted monostable outputs. These pins (normally high) pulse low when the multivibrator is triggered at either the A or the B input. These outputs are the inverse of Q1 and Q2.

LOGIC DETAIL
(1/2 THE DEVICE)

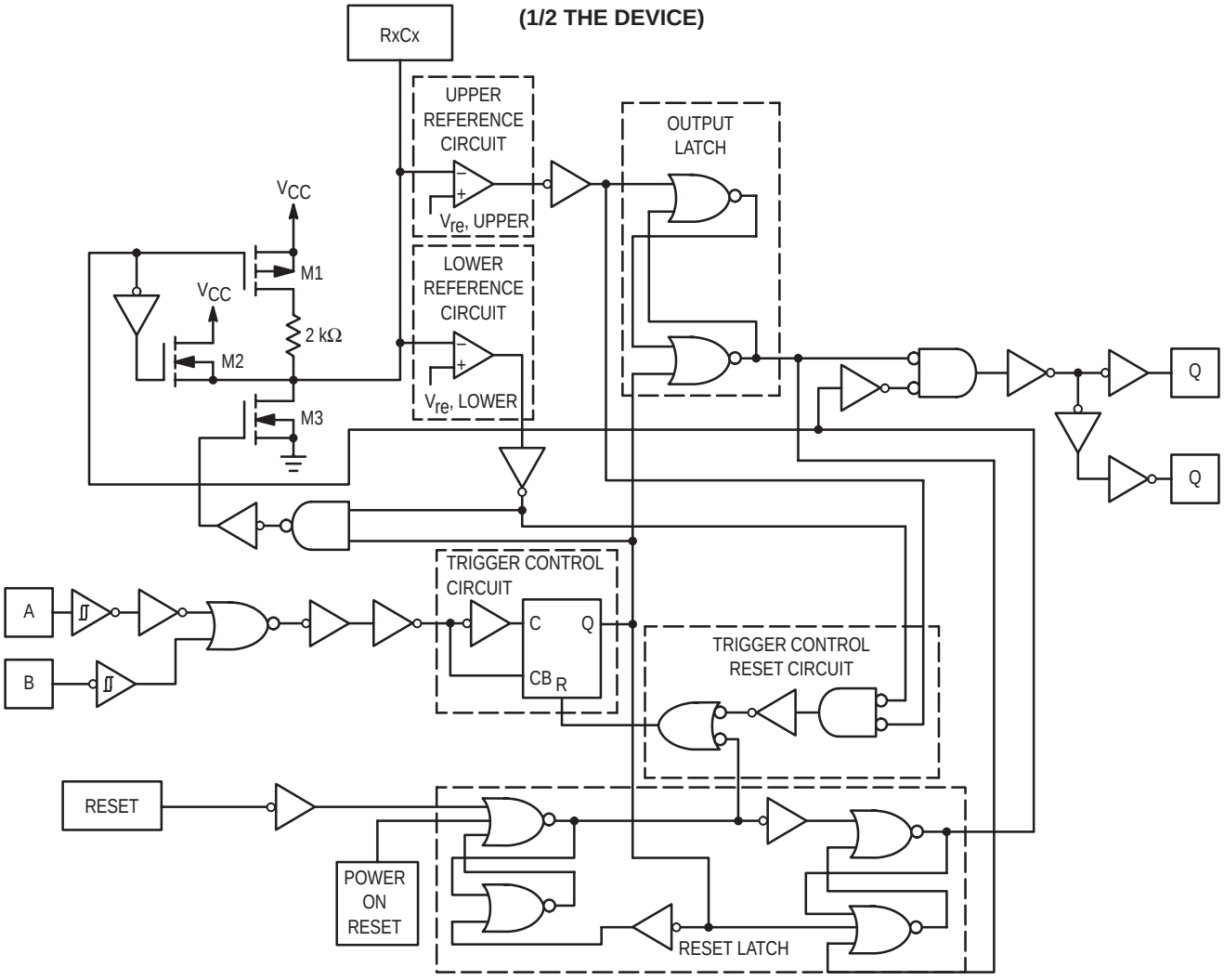


Figure 9.

CIRCUIT OPERATION

Figure 12 shows the HC4538A configured in the retriggerable mode. Briefly, the device operates as follows (refer to Figure 10): In the quiescent state, the external timing capacitor, C_X, is charged to V_{CC}. When a trigger occurs, the Q output goes high and C_X discharges quickly to the lower reference voltage (V_{ref} Lower $\approx$ 1/3 V_{CC}). C_X then charges, through R_X, back up to the upper reference voltage (V_{ref} Upper $\approx$ 2/3 V_{CC}), at which point the one–shot has timed out and the Q output goes low.

The following, more detailed description of the circuit operation refers to both the logic detail (Figure 9) and the timing diagram (Figure 10).

QUIESCENT STATE

In the quiescent state, before an input trigger appears, the output latch is high and the reset latch is high (#1 in Figure 10). Thus the Q output (pin 6 or 10) of the monostable multivibrator is low (#2, Figure 10).

The output of the trigger–control circuit is low (#3), and transistors M1, M2, and M3 are turned off. The external timing capacitor, C_X, is charged to V_{CC} (#4), and both the upper and lower reference circuit has a low output (#5).

In addition, the output of the trigger–control reset circuit is low.

TRIGGER OPERATION

The HC4538A is triggered by either a rising–edge signal at input A (#7) or a falling–edge signal at input B (#8), with the unused trigger input and the Reset input held at the voltage levels shown in the Function Table. Either trigger signal will cause the output of the trigger–control circuit to go high (#9).

The trigger–control circuit going high simultaneously initiates two events. First, the output latch goes low, thus taking the Q output of the HC4538A to a high state (#10). Second, transistor M3 is turned on, which allows the external timing capacitor, C_X, to rapidly discharge toward ground (#11). (Note that the voltage across C_X appears at the input of both the upper and lower reference circuit comparator).

When C_X discharges to the reference voltage of the lower reference circuit (#12), the outputs of both reference circuits will be high (#13). The trigger–control reset circuit goes high, resetting the trigger–control circuit flip–flop to a low state (#14). This turns transistor M3 off again, allowing C_X to begin to charge back up toward V_{CC}, with a time constant $t = R_X C_X$ (#15). Once the voltage across C_X charges to above the lower reference voltage, the lower reference circuit will go low allowing the monostable multivibrator to be retriggered.

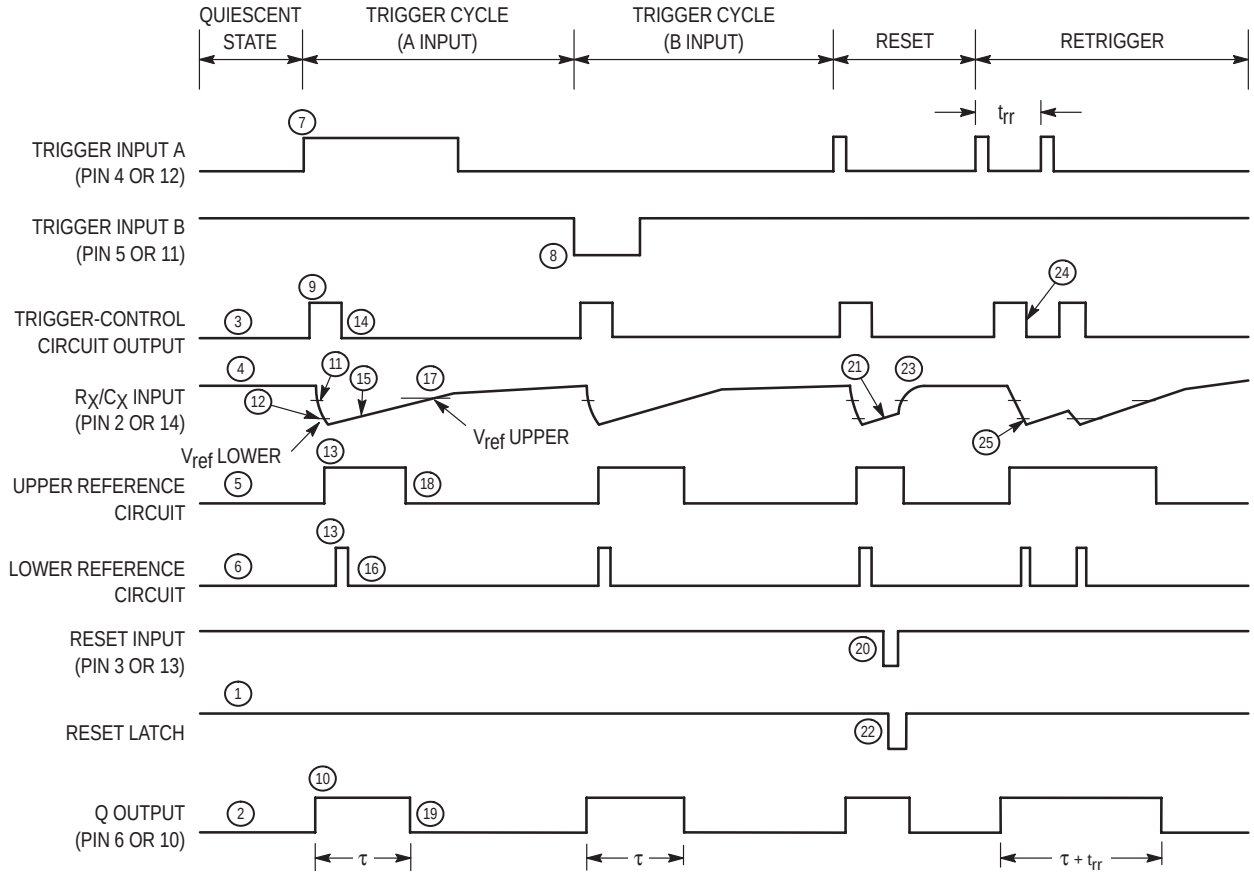


Figure 10. Timing Diagram

When C_X charges up to the reference voltage of the upper reference circuit (#17), the output of the upper reference circuit goes low (#18). This causes the output latch to toggle, taking the Q output of the HC4538A to a low state (#19), and completing the time–out cycle.

POWER–DOWN CONSIDERATIONS

Large values of C_X may cause problems when powering down the HC4538A because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from V_{CC} through the input protection diodes at pin 2 or pin 14. Current through the protection diodes must be limited to 30 mA; therefore, the turn–off time of the V_{CC} power supply must not be faster than $t = V_{CC} \bullet C_X/(30\ mA)$. For example, if V_{CC} = 5.0 V and C_X = 15 μF, the V_{CC} supply must turn off no faster than t = (5.0 V)•(15 μF)/30 mA = 2.5 ms. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of V_{CC} to zero volts occurs, the HC4538A may sustain damage. To avoid this possibility, use an external damping diode, D_X, connected as shown in Figure 11. Best results can be achieved if diode D_X is chosen to be a germanium or Schottky type diode able to withstand large current surges.

RESET AND POWER ON RESET OPERATION

A low voltage applied to the Reset pin always forces the Q output of the HC4538A to a low state.

The timing diagram illustrates the case in which reset occurs (#20) while C_X is charging up toward the reference voltage of the upper reference circuit (#21). When a reset occurs, the output of the reset latch goes low (#22), turning on transistor M1. Thus C_X is allowed to quickly charge up to V_{CC} (#23) to await the next trigger signal.

On power up of the HC4538A the power–on reset circuit will be high causing a reset condition. This will prevent the trigger–control circuit from accepting a trigger input during this state. The HC4538A's Q outputs are low and the $\overline{Q}$ not outputs are high.

RETRIGGER OPERATION

When used in the retriggerable mode (Figure 12), the HC4538A may be retriggered during timing out of the output pulse at any time after the trigger–control circuit flip–flop has been reset (#24), and the voltage across C_X is above the lower reference voltage. As long as the C_X voltage is below the lower reference voltage, the reset of the flip–flop is high, disabling any trigger pulse. This prevents M3 from turning on during this period resulting in an output pulse width that is predictable.

The amount of undershoot voltage on R_XC_X during the trigger mode is a function of loop delay, M3 conductivity, and V_{DD}. Minimum retrigger time, trr (Figure 7), is a function of 1) time to discharge R_XC_X from V_{DD} to lower reference voltage($T_{discharge}$);2)loopdelay(T_{delay});3)timetocharge R_XC_X from the undershoot voltage back to the lower reference voltage (T_{charge}).

Figure 13 shows the device configured in the non–retriggerable mode.

For additional information, please see Application Note (AN1558/D) titled *Characterization of Retrigger Time in the HC4538A Dual Precision Monstable Multivibrator.*

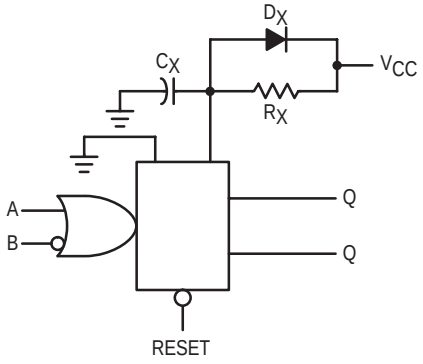


Figure 11. Discharge Protection During Power Down

TYPICAL APPLICATIONS

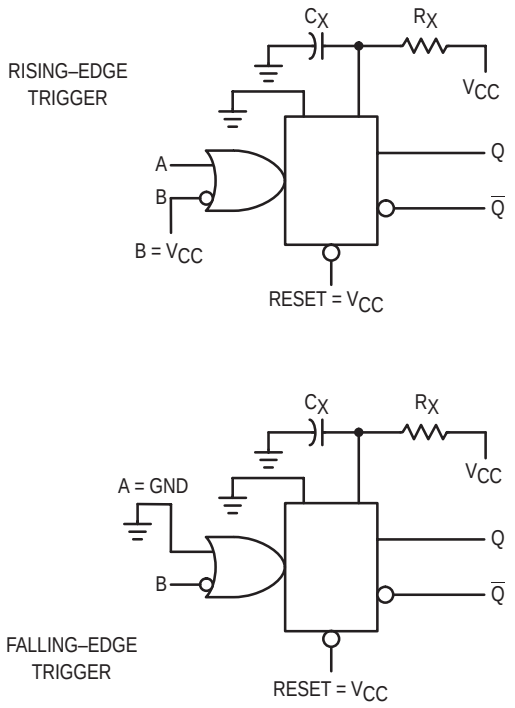


Figure 12. Retriggerable Monostable Circuitry

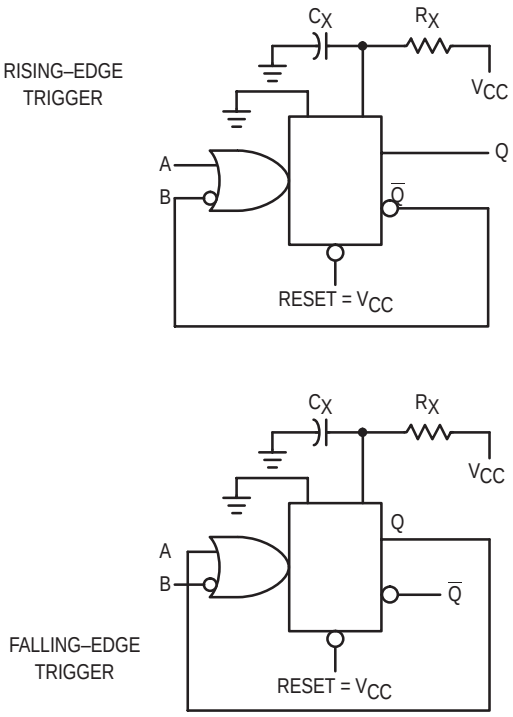


Figure 13. Non–retriggerable Monostable Circuitry

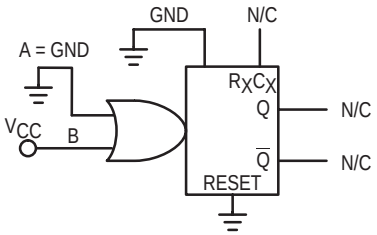
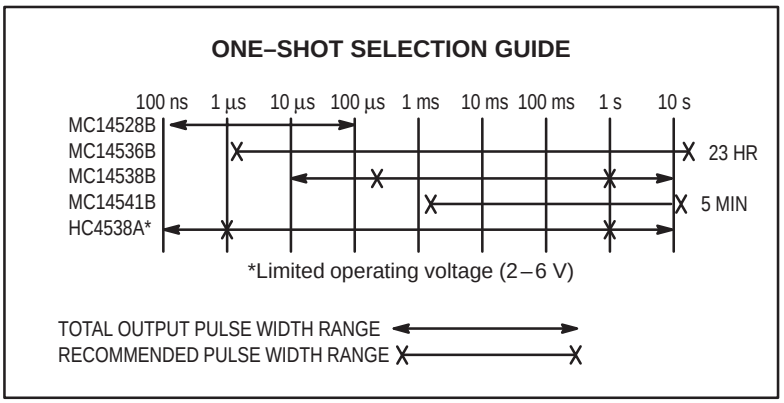


Figure 14. Connection of Unused Section



MC74HC4851A, MC74HC4852A

Analog Multiplexers/ Demultiplexers with Injection Current Effect Control

Automotive Customized

These devices are pin compatible to standard HC405x and MC1405xB analog mux/demux devices, but feature injection current effect control. This makes them especially suited for usage in automotive applications where voltages in excess of normal logic voltage are common.

The injection current effect control allows signals at disabled analog input channels to exceed the supply voltage range without affecting the signal of the enabled analog channel. This eliminates the need for external diode/ resistor networks typically used to keep the analog channel signals within the supply voltage range.

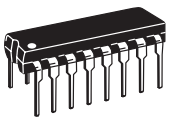
The devices utilize low power silicon gate CMOS technology. The Channel Select and Enable inputs are compatible with standard CMOS outputs.

- Injection Current Cross–Coupling Less than 1mV/mA (See Figure 9)
- Pin Compatible to HC405X and MC1405XB Devices
- Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- In Compliance With the Requirements of JEDEC Standard No. 7A
- Chip Complexity: 154 FETs or 36 Equivalent Gates

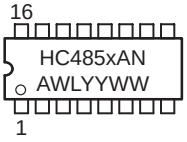
ON Semiconductor

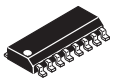
http://onsemi.com

MARKING DIAGRAMS

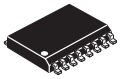


PDIP–16
N SUFFIX
CASE 648



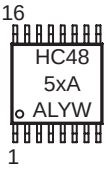


SOIC–16
D SUFFIX
CASE 751B



SOIC–16 WIDE
DW SUFFIX
CASE 751G

TSSOP–16
DT SUFFIX
CASE 948F



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 380 of this data sheet.

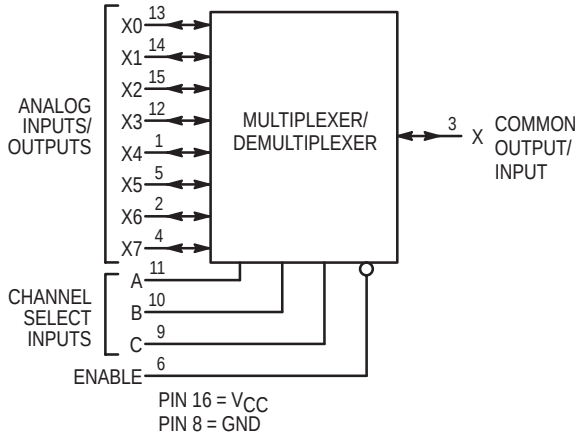


Figure 1. MC74HC4851A Logic Diagram
Single–Pole, 8–Position Plus Common Off

FUNCTION TABLE – MC74HC4851A

Control Inputs				
	Select			
Enable	C	B	A	ON Channels
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

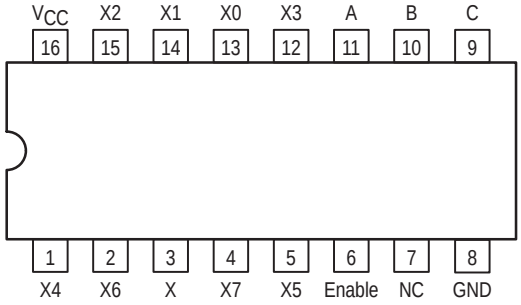


Figure 2. MC74HC4851A 16–Lead Pinout (Top View)

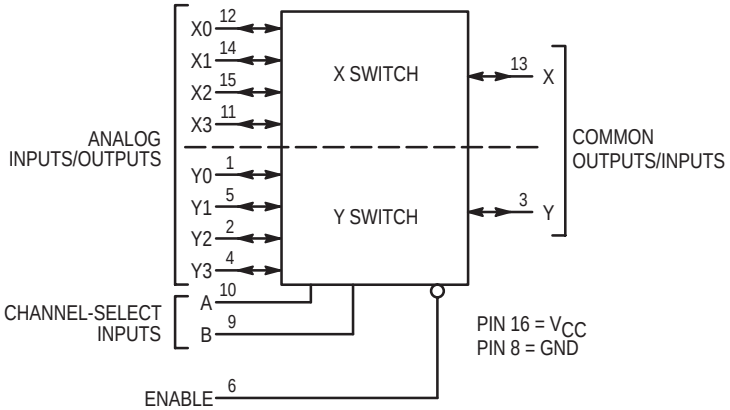


Figure 3. MC74HC4852A Logic Diagram
Double–Pole, 4–Position Plus Common Off

FUNCTION TABLE – MC74HC4852A

Control Inputs			
	Select		
Enable	B	A	ON Channels
L	L	L	Y0 X0
L	L	H	Y1 X1
L	H	L	Y2 X2
L	H	H	Y3 X3
H	X	X	NONE

X = Don't Care

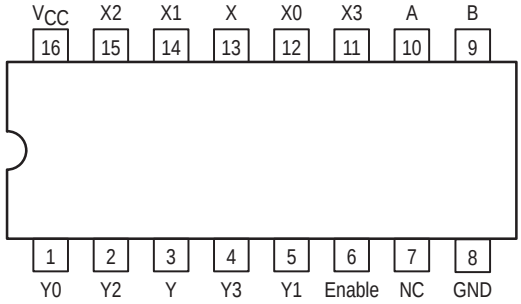


Figure 4. MC74HC4852A 16–Lead Pinout (Top View)

MAXIMUM RATINGS*

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage	(Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Any Pin)	(Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin		± 25	mA
P_D	Power Dissipation in Still Air,	Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature Range		– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package		260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	(Referenced to GND)	2.0	6.0	V
V_{in}	DC Input Voltage (Any Pin)	(Referenced to GND)	GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		0.0	1.2	V
T_A	Operating Temperature Range, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise/Fall Time (Channel Select or Enable Inputs)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

*For voltage drops across switch greater than 1.2V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND) V_{EE} = GND, Except Where Noted

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
I_{in}	Maximum Input Leakage Current on Digital Pins (Enable/A/B/C)	V_{in} = V_{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in(digital)}$ = V_{CC} or GND $V_{in(analog)}$ = GND	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

DC CHARACTERISTICS — Analog Section

Symbol	Parameter	Condition	V_{CC}	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
R_{on}	Maximum "ON" Resistance	V_{in} = V_{IL} or V_{IH}; V_{IS} = V_{CC} to GND; I_S ≤ 2.0 mA	2.0 3.0 4.5 6.0	1700 1100 550 400	1750 1200 650 500	1800 1300 750 600	Ω
ΔR_{on}	Delta "ON" Resistance	V_{in} = V_{IL} or V_{IH}; V_{IS} = V_{CC}/2 I_S ≤ 2.0 mA	2.0 3.0 4.5 6.0	300 160 80 60	400 200 100 80	500 240 120 100	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel Common Channel	V_{in} = V_{CC} or GND	6.0	 ±0.1 ±0.2	 ±0.5 ±2.0	 ±1.0 ±4.0	µA
I_{on}	Maximum On–Channel Leakage Channel–to–Channel	V_{in} = V_{CC} or GND	6.0	±0.2	±2.0	±4.0	µA

AC CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V_{CC}	–55 to 25°C	≤85°C	≤125°C	Unit
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Analog Input to Analog Output	2.0 3.0 4.5 6.0	160 80 40 30	180 90 45 35	200 100 50 40	ns
t_{PHL}, $t_{PHZ,PZH}$ t_{PLH}, $t_{PLZ,PZL}$	Maximum Propagation Delay, Enable or Channel–Select to Analog Output	2.0 3.0 4.5 6.0	260 160 80 60	280 180 90 70	300 200 100 80	ns
C_{in}	Maximum Input Capacitance Digital Pins (All Switches Off) Any Single Analog Pin (All Switches Off) Common Analog Pin		10 35 130	10 35 130	10 35 130	pF
C_{PD}	Power Dissipation Capacitance Typical	5.0	20			pF

INJECTION CURRENT COUPLING SPECIFICATIONS (V_{CC} = 5V, T_A = –55°C to +125°C)

Symbol	Parameter	Typ	Max	Unit	Condition
$V\Delta_{out}$	Maximum Shift of Output Voltage of Enabled Analog Channel	0.1 1.0 0.5 5.0	1.0 5.0 2.0 20	mV	I_{in}* ≤ 1mA, R_S ≤ 3,9kΩ I_{in}* ≤ 10mA, R_S ≤ 3,9kΩ I_{in}* ≤ 1mA, R_S ≤ 20kΩ I_{in}* ≤ 10mA, R_S ≤ 20kΩ

* I_{in} = Total current injected into all disabled channels.

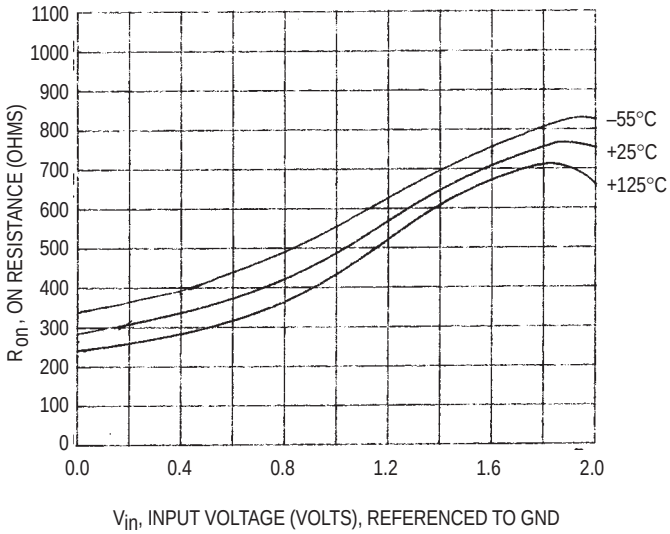


Figure 5. Typical On Resistance V_{CC} = 2V

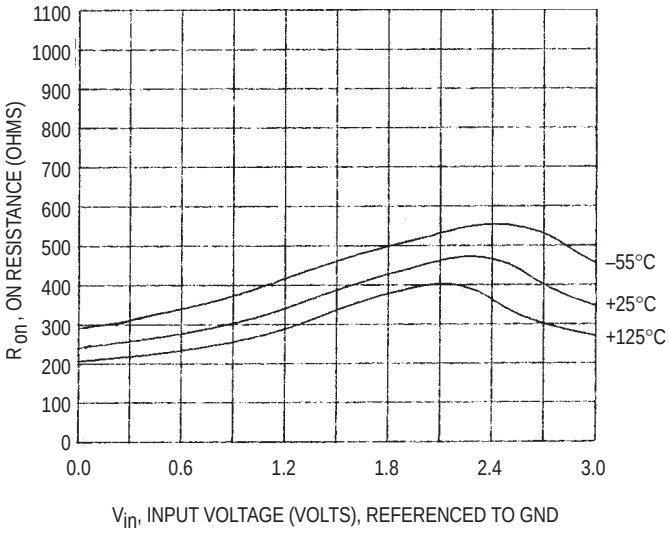


Figure 6. Typical On Resistance V_{CC} = 3V

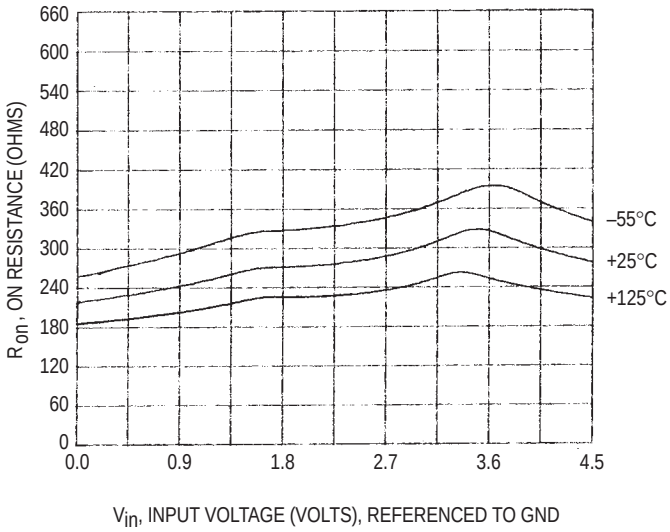


Figure 7. Typical On Resistance V_{CC} = 4.5V

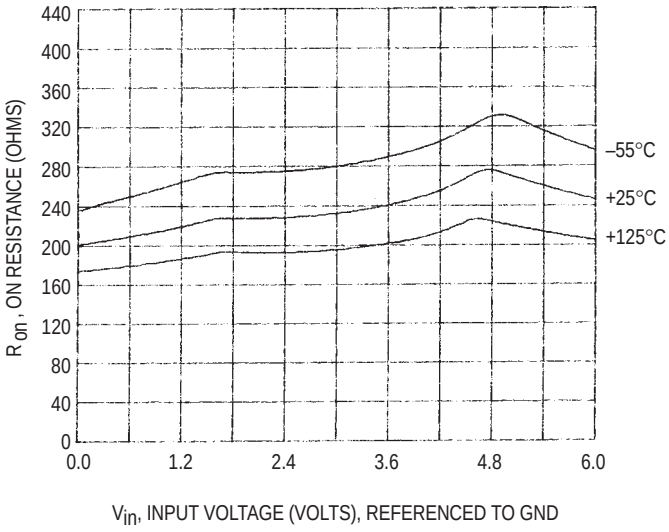


Figure 8. Typical On Resistance V_{CC} = 6V

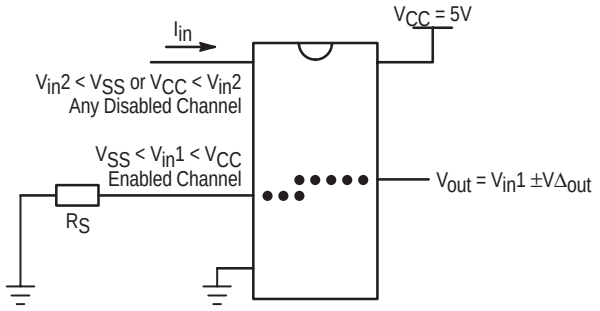


Figure 9. Injection Current Coupling Specification

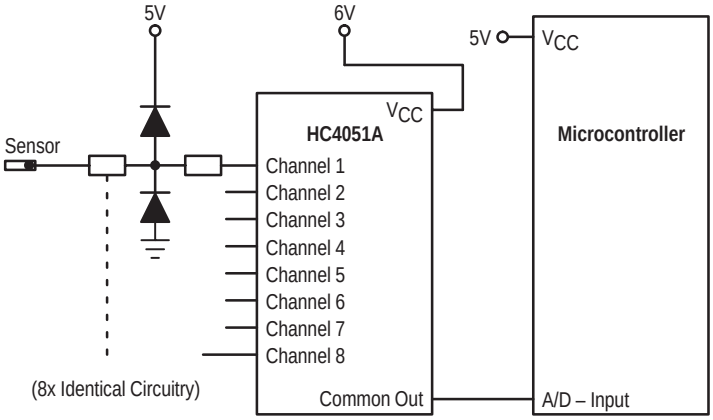


Figure 10. Actual Technology
Requires 32 passive components and one extra 6V regulator
to suppress injection current into a standard HC4051 multiplexer

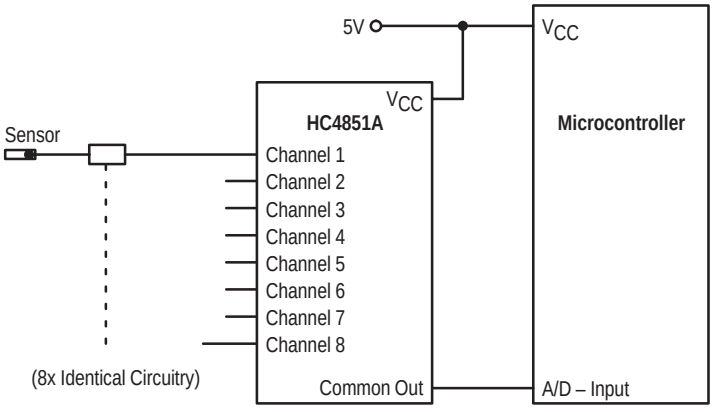


Figure 11. MC74HC4851A Solution
Solution by applying the HC4851A multiplexer

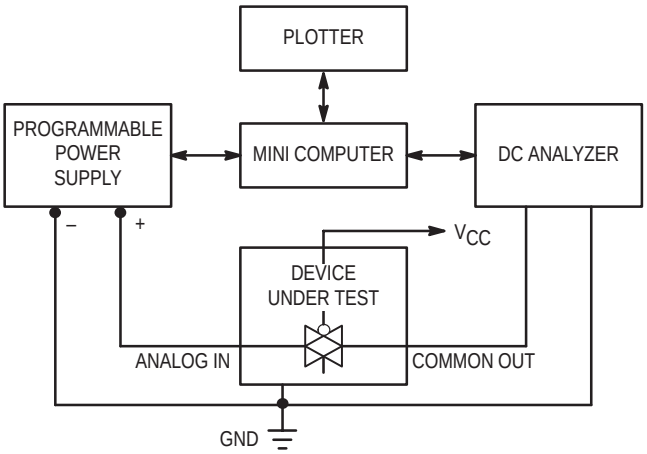


Figure 12. On Resistance Test Set–Up

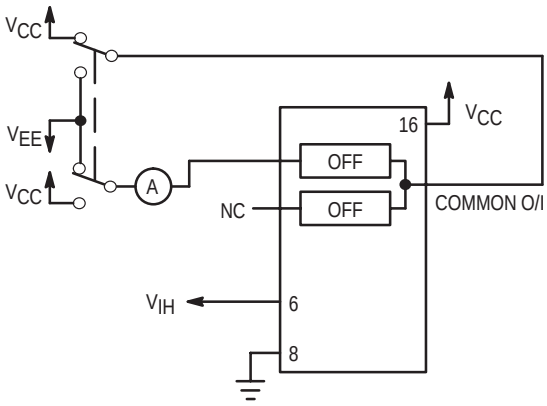


Figure 13. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

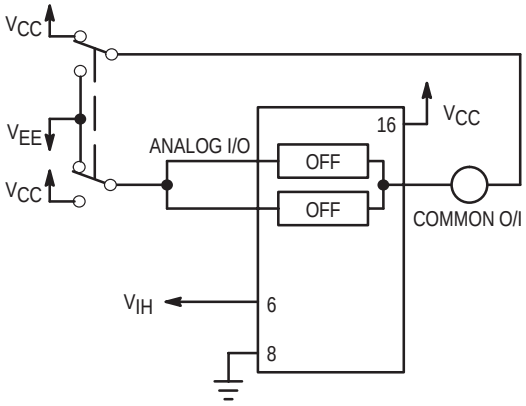


Figure 14. Maximum Off Channel Leakage Current, Common Channel, Test Set–Up

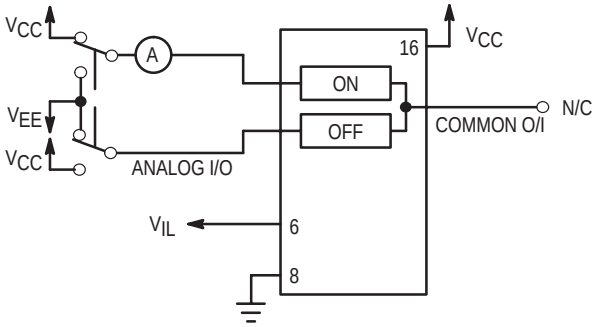


Figure 15. Maximum On Channel Leakage Current, Channel to Channel, Test Set–Up

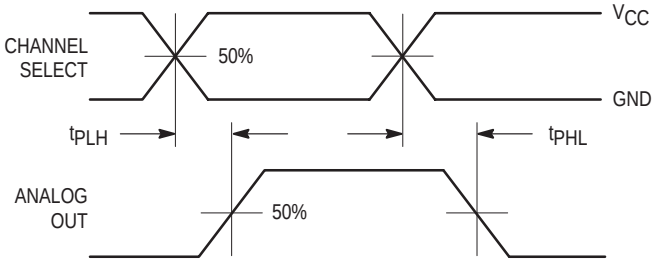
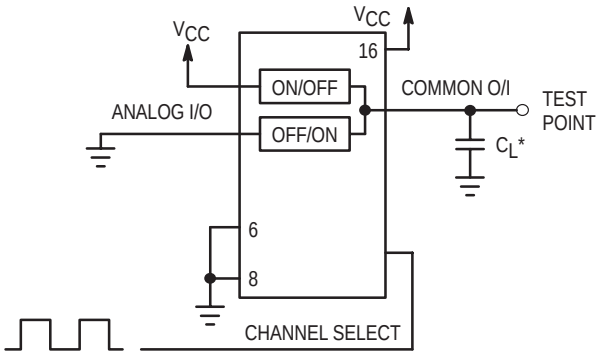


Figure 16. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 17. Propagation Delay, Test Set–Up Channel Select to Analog Out

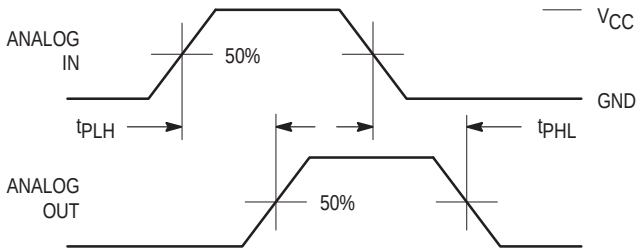
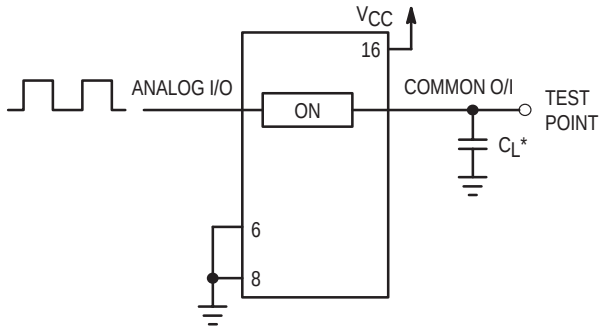


Figure 18. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance

Figure 19. Propagation Delay, Test Set–Up Analog In to Analog Out

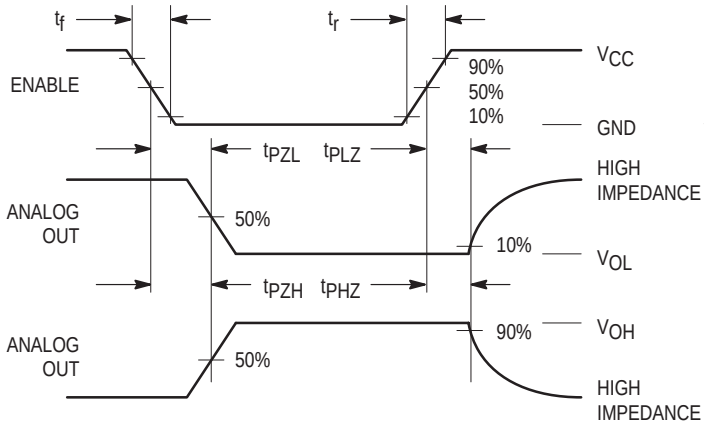


Figure 20. Propagation Delays, Enable to Analog Out

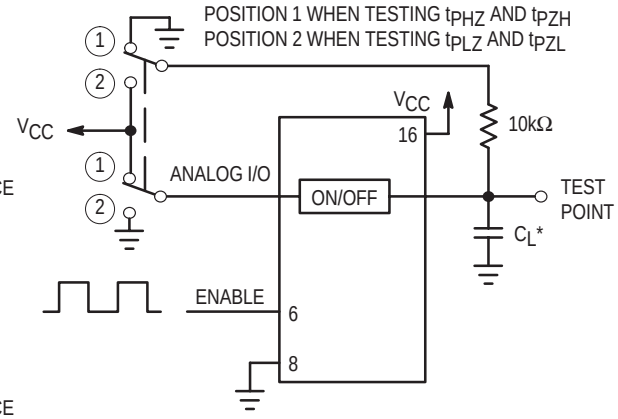


Figure 21. Propagation Delay, Test Set–Up Enable to Analog Out

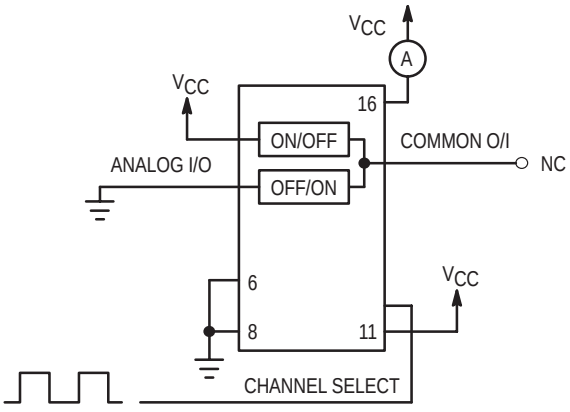


Figure 22. Power Dissipation Capacitance, Test Set–Up

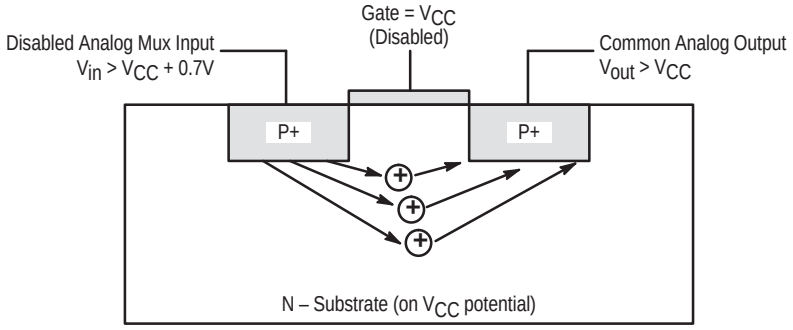


Figure 23. Diagram of Bipolar Coupling Mechanism
Appears if V_{in} exceeds V_{CC}, driving injection current into the substrate

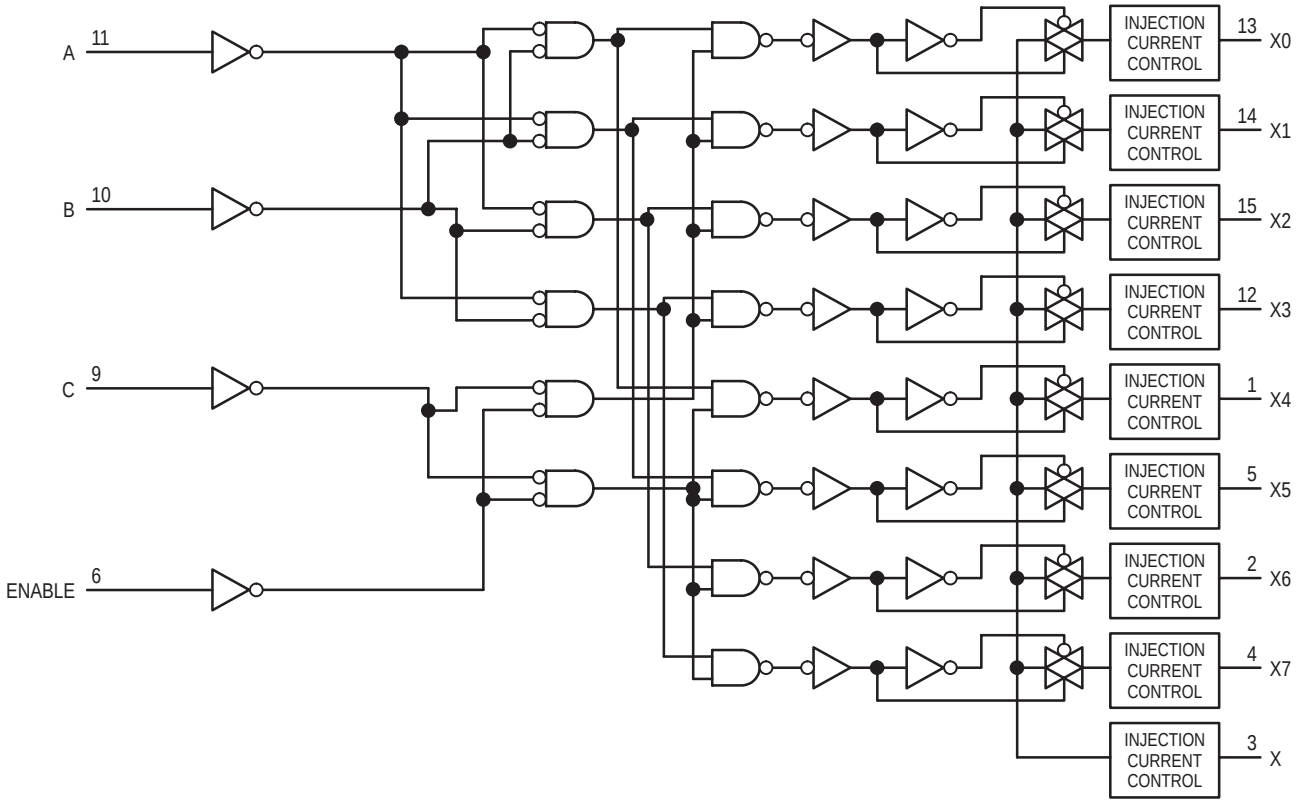


Figure 24. Function Diagram, HC4851A

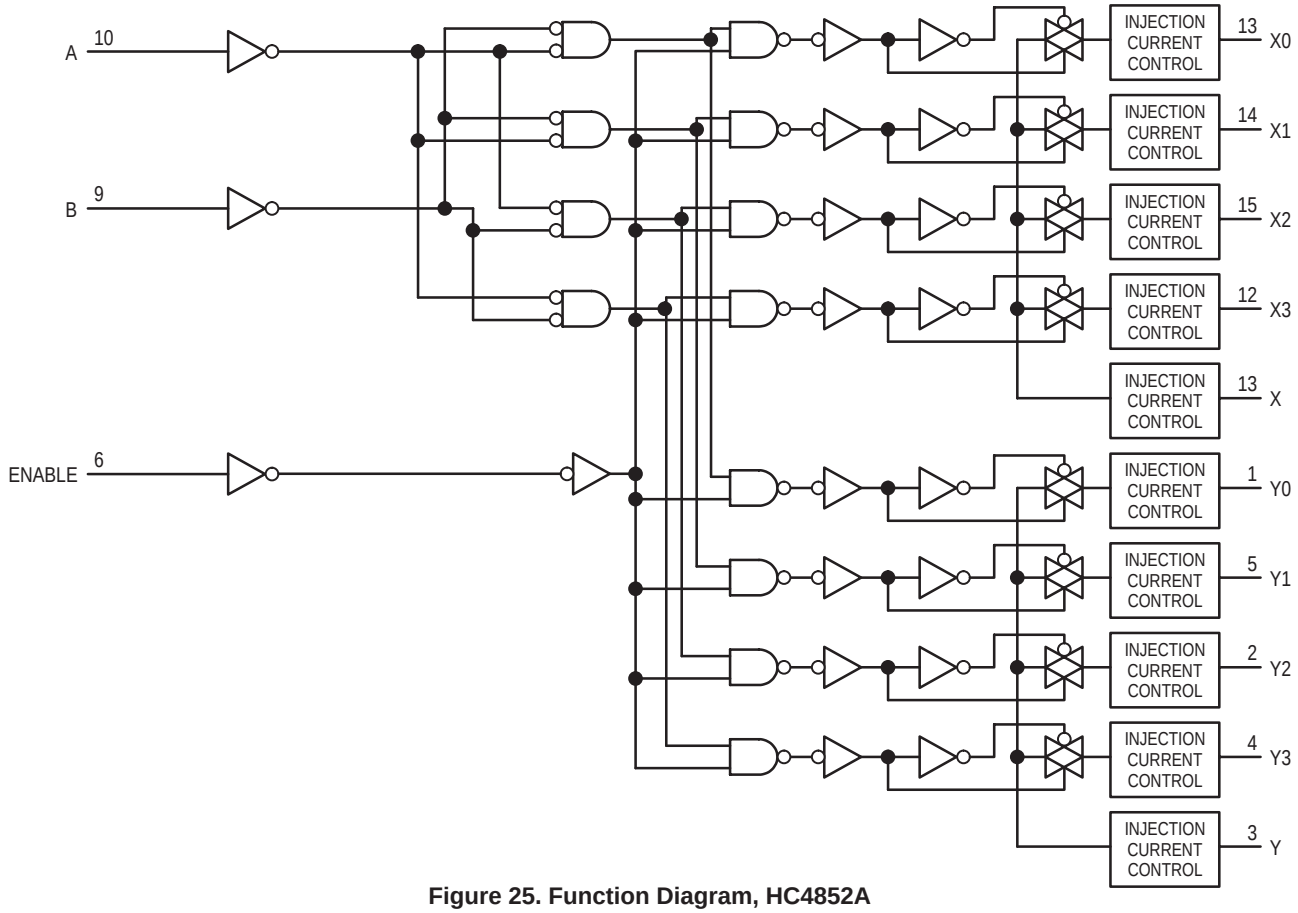


Figure 25. Function Diagram, HC4852A

ORDERING & SHIPPING INFORMATION

Device	Package	Shipping
MC74HC4851AN	PDIP–16	500 Units / Unit Pak
MC74HC4851AD	SOIC–16	48 Units / Rail
MC74HC4851ADR2	SOIC–16	2500 Units / Tape & Reel
MC74HC4851ADW	SOIC–16 WIDE	48 Units / Rail
MC74HC4851ADWR2	SOIC–16 WIDE	1000 Units / Tape & Reel
MC74HC4851ADT	TSSOP–16	96 Units / Rail
MC74HC4851ADTR2	TSSOP–16	2500 Units / Tape & Reel
MC74HC4852AN	PDIP–16	500 Units / Unit Pak
MC74HC4852AD	SOIC–16	48 Units / Rail
MC74HC4852ADR2	SOIC–16	2500 Units / Tape & Reel
MC74HC4852ADW	SOIC–16 WIDE	48 Units / Rail
MC74HC4852ADWR2	SOIC–16 WIDE	1000 Units / Tape & Reel
MC74HC4852ADT	TSSOP–16	96 Units / Rail
MC74HC4852ADTR2	TSSOP–16	2500 Units / Tape & Reel

CHAPTER 4
Application Notes

Configuring and Applying the MC74HC4046A Phase-Locked Loop

A versatile device for 0.1 to 16MHz frequency synchronization

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APPLICATION NOTE

Abstract

The MC74HC4046A (hereafter designated HC4046A) phase–locked loop contains three phase comparators, a voltage–controlled oscillator (VCO) and an output amplifier. The user of this document should have a copy of the HC4046A data sheet in ON Semiconductor Data Book DL129 available for details of device operation and operating specifications. The user should also be aware that the following information is useful for approximating a design **but**, because of process, layout and other variables, there can be substantial deviation between theory and actual results. Therefore, **it is highly recommended that prototypes be built and checked before committing a design to production**.

Typical applications for the HC4046A usually involve a configuration such as shown in Figure 1.

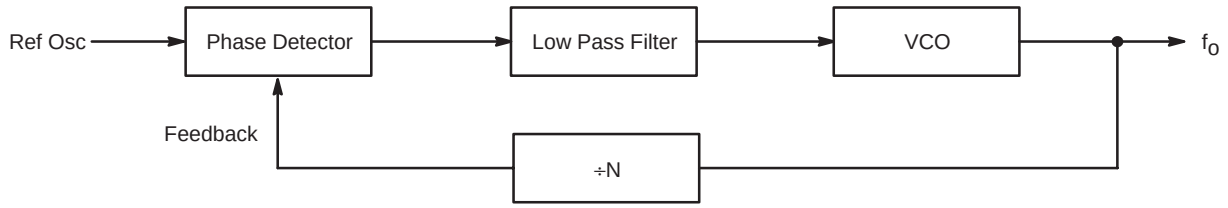

Figure 1. Typical Phase–Locked Loop

VCO/OUTPUT FREQUENCY

The output frequency, F_O, is calculated as a function of the Ref Osc input and the ÷N feedback counter:

$$F_O = \text{Ref Osc} * N \quad (1)$$

The ability of the loop to emulate the above formula makes it ideal for multiplying an input frequency by any number up to the maximum of the VCO. The HC4046A VCO frequency is controlled by the equation:

$$\text{VCO freq} = f(I * C) \quad (2)$$

where I is controlled by the external resistors R_1 and R_2 and C by external capacitor C_{ext} .

Frequency of oscillation is calculated by starting with the familiar equation:

$$I = c\frac{dV}{dt} \quad (3)$$

and reworking it to obtain a formula that incorporates all the detail to fit the HC4046A. First, the charge time of the device for half–cycle time is obtained as follows:

$$dt = dV\frac{C}{I} \quad \text{and} \quad F_O = \frac{1}{2dt}$$

$$\text{or,} \quad F_O = \frac{\frac{1}{2CdV}}{I} = \frac{I}{2CdV} \quad (4)$$

where I and dV must be obtained for the HC4046A.

There are two components that comprise the I charge for the HC4046A VCO, I_1 and I_2. I_1 is the current that sets the frequency associated with the VCO input and is a function of R_1, VCO_{in}, and an internal current mirror that is ratioed at 120/5 ≈ 24, resulting in the equation:

$$I_1 = \frac{VCO_{in}}{R_1}\left(\frac{120}{5}\right) \quad (5)$$

I_2 is set by R_2 and adds a constant current to limit the F_o min of the VCO and is a function of V_{dd}, R_2, and an internal current mirror of ratio 23/5, resulting in the equation:

$$I_2 = \left(\frac{2V_{dd}}{3R_2}\right)\left(\frac{23}{5}\right) \quad (6)$$

The dV of Equation (4) is determined by design to be ≈ 1/3 V_{dd}. Substituting this and $I = I_1 + I_2$ into Equation (4) results in:

$$F_o = \frac{\frac{VCO_{in}}{R_1}\left(\frac{120}{5}\right) + \left(\frac{2V_{dd}}{3R_2}\right)\left(\frac{23}{5}\right)}{2C_{ext}\frac{V_{dd}}{3}}$$

$$= \frac{\frac{VCO_{in}}{R_1}(24) + \left(\frac{2V_{dd}}{3R_2}\right)(4.6)}{2C_{ext}\frac{V_{dd}}{3}}$$

$$= \frac{\frac{3VCO_{in}}{R_1}(24) + \frac{2V_{dd}}{R_2}(4.6)}{2C_{ext}\ V_{dd}} \quad (7)$$

It was found by experiment that when the C_{ext} potential reaches threshold (at $V_{dd}/3$), the inversion of the charging voltage of C_{ext} is forced below ground due to charge coupling. Therefore, the dV is not just $V_{dd}/3$ as expected and the charging time must start at a point below ground which affects t and thus, F_o. An undershoot voltage must be added to the equation for better accuracy in calculating t and F_o. This modifies Equation (7) as follows:

$$F_o = \frac{\frac{3VCO_{in}}{R_1}(24) + \frac{2V_{dd}}{R_2}(4.6)}{2C_{ext}\ (V_{dd} + 3 * undershoot)}$$

$$= \frac{\frac{3VCO_{in}(I_{constant\ ratio})}{R_1} + \frac{9.2(V_{dd})}{R_2}}{2C_{ext}\ (V_{dd} + 3 * undershoot)} \quad (8)$$

Equation (8) now contains all the factors to calculate an F_o for the HC4046A VCO.

It was determined by experiment that the undershoot of the charging waveform is a function of C_{ext} and an on–chip parasitic diode that clamps it at a maximum of –0.7V. The size of the C_{ext} capacitor limits the voltage and was found to be near zero volts for $C_{stray} \approx 17pF \le C_{ext} \le 30pF$; the voltage increases at 6 mV/pF for a $30pF \le C_{ext} \le 150pF$ range of C_{ext}. The on–chip diode then takes over and limits the voltage to –0.7V.

It was also found that the $I_{constant\ ratio}$ is a function of R_1 and increases as R_1 becomes larger. The change is attributed to saturation of the current mirror at lower value resistances, and to voltage divider problems at higher value resistances combined with the resistance of the small FET in the current mirror. Experimental data shows that $I_{constant\ ratio}$ follows Table 1 somewhat. The ratio goes to 25 somewhere between 9.1KΩ and 51KΩ, and for those limits, 25 should give reasonable results. In addition, these numbers seem to hold for a range of V_{dd} of $3.0V \le V_{dd} \le 6V$.

1. $I_{constant\ ratio}$ versus R_1

R_1 (KΩ)	$I_{constant\ ratio}$
3.0	13.5
5.1	17.5
9.1	21.5
12	23.0
15	24.0
30	26.5
40	27.0
51	28.5
110	29.0
300	31.0

The VCO calculation [Equation (8)] becomes a bit more accurate by adjusting the VCO_{in} and $I_{constant\ ratio}$. For example, with R_1 = 300K, $R_2 = \infty$, C_{ext} = 0.1μF, VCO_{in} = 1.0V, V_{dd} = 4.5V, and $I_{constant\ ratio}$ = 31, Equation (8) yields:

$$F_o = \frac{\frac{(3)(1)(31)}{300K}}{2(0.1 * 10^{-6})(4.5 + 2.1)}$$

$$= 235Hz$$

For comparison, from Chart 14D in the HC4046A data sheet, the F_o based on measurements is approximately 270 Hz. Thus, the calculated and measured values are not too far apart taking into consideration such variables as process variation, temperature, and breadboard inaccuracies. The C_{stray} of a PCB layout will affect results if the C_{ext} is not ≫ C_{stray}. So for $C_{ext} \le 1000pF$, adding C_{stray} to the C_{ext} fixed capacitance will result in better accuracy.

The gain of a VCO is calculated by knowing f_{max} at VCO_{in} max and f_{min} at VCO_{in}min and calculating the following equation:

$$VCO\ gain = \frac{f\,max - f\,min}{VCO_{in}\,max - VCO_{in}\,min} \quad (9)$$

$$= \Delta freq/volt$$

The gain of the VCO is needed to calculate a suitable loop filter for a PLL system.

F_o is determined by VCO_{in} and is clamped as a function of a % of V_{dd}. The clamp voltage generally follows the slope of 4%/V for V_{dd} changes from $3.5V \le V_{dd} \le 6V$, starting at 56% at V_{dd} = 3.5V and going to 66% at V_{dd} = 6V. Knowing this limit point allows picking a VCO_{in} max point a few hundred mV below it and keeps F_o in the linear range of operation. It also best to pick a VCO_{in} min point at a level of a few hundred mV above 0V for the same reason given above.

As an example, for a C_{ext} = 1100pF, R_1 = 9.1K, $R_2 = \infty$, V_{dd} = 5.0V, and VCO_{in} min = 0.25V, VCO_{in} max can be determined and a gain calculated as follows. VCO_{in} limit = (4%/V)(1.5V) + 56% = (62%)(V_{dd}) = 3.1V. So, for sake of linearity, choose VCO_{in} = 2.5V. Using Equation (8), VCO_{in} min and VCO_{in} max can be used to calculate F_o min and F_o max as follows:

$$F_o\ min = \frac{\frac{(3)(0.25)(21.5)}{9.1K}}{2(1100 * 10^{-12})(5 + 2.1)} = 113.4KHz$$

$$F_o\ max = \frac{\frac{(3)(2.5)(21.5)}{9.1K}}{2(1100 * 10^{-12})(5 + 2.1)} = 1.3MHz$$

Then, using Equation (9), the VCO gain is:

$$VCO\ gain = \frac{1.3 * 10^6 – 0.11 * 10^6}{2.5 – 0.25} = 528.9KHz/V$$

This gain factor will be known as K_{VCO} in the loop filter equations.

R_2 is used in applications where a minimum output frequency is desired when VCO_{in} is 0V. It is calculated at VCO_{in} = 0V causing Equation (8) to become:

$$F_o = \frac{9.2\ (V_{dd})}{2C\ (R_2)\ (V_{dd} + 3 * undershoot)}$$

The additional I_2 current is a constant that adds to total charge current for C_{ext} and increases the VCO_{in} versus F_o curve by a theoretical constant amount. In reality, the amount of increase actually decreases at a slight rate as VCO_{in} increases. The decrease is slight and the use of Equation (8) will give adequate accuracy for most applications.

The F_{max} of the HC4046A VCO was determined to be about 16MHz. Beyond 16MHz, the output logic swing tends to reduce and is therefore somewhat useless for driving a CMOS input. The VCO will operate at ≈ 28MHz but the output has a V_{OL}≈ 2.0V and a V_{OH}≈ 4.5V at V_{dd} = 5.0V.

The following table was generated to make calculation of R_1 and C_{ext} a function of F_o with V_{dd} = 5V, VCO_{in} = 1V, and room temperature. Use of the table allows a rough estimate of $(R_1)(C_{ext})$ for a given F_o. The final values can be adjusted by use of Equation (8), Table 1 for $I_{constant\ ratio}$, rules for undershoot voltage, V_{dd} variations, and VCO_{in} variations. The example below shows a typical calculation.

2. $(R_1)(C_{ext})$ versus F_o

R_1 (Ω)	C_{ext} (pF)	$(R_1)(C_{ext})$
3.0K ≤ R_1 ≤ 9.0K	0 ≤ C_{ext} ≤ 30 30 ≤ C_{ext} ≤ 150 150 ≤ C_{ext} ≤ ∞	5.40/F_o 4.15/F_o 3.80/F_o
9.1K ≤ R_1 ≤ 50K	0 ≤ C_{ext} ≤ 30 30 ≤ C_{ext} ≤ 150 150 ≤ C_{ext} ≤ ∞	7.50/F_o 5.77/F_o 5.28/F_o
50K ≤ R_1 ≤ 900K	0 ≤ C_{ext} ≤ 30 30 ≤ C_{ext} ≤ 150 150 ≤ C_{ext} ≤ ∞	9.00/F_o 6.92/F_o 6.34/F_o

Assume a desired value of F_o of 1MHz. From 2, choose an R_1 range of 9.1K ≤ R_1 ≤ 50K and a C_{ext} range of > 150pF; this condition leads to $(R_1)(C_{ext}) = 5.28/F_o$. Thus,

$$(R_1)\ (C_{ext}) = \frac{5.28}{1 * 10^6} = 5.28 * 10^{-6}$$

Now choose a C_{ext} of 200pF. Then, from above result,

$$R_1 = \frac{5.28 * 10^{-6}}{200 * 10^{-12}} = 26K$$

This appears reasonable and there are standard values for C_{ext} = 200pF and R_1 = 27K. Using these values, Equation (8) can be adjusted according to the desired F_o min, F_o max, and F_o center.

LOW PASS FILTER DESIGN

The design of low pass filters is well known and the intent here is to simply show some typical examples. Reference should be made to the HC4046A Data Sheet and to Application Note AN535/D — “Phase–Locked Loop Fundamentals” (available through ON Semiconductor Literature Distribution).

Some simple types of low pass filters are shown in Figure 2 and Figure 3.

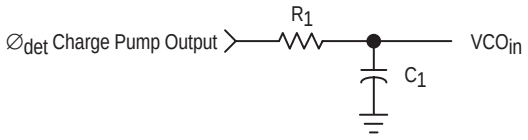

Figure 2. Simple Low Pass Filter A

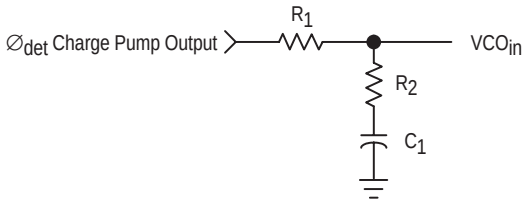

Figure 3. Simple Low Pass Filter B

The equations for calculating loop natural frequency (w_n) and damping factor (d) are as follows:

For Filter A (Figure 2):

$$w_n = \sqrt{\frac{K_{\varnothing}K_{VCO}}{NC_1R_1}}$$

$$d = \frac{0.5w_n}{K_{\varnothing}K_{VCO}}$$

where $K_{\varnothing}$ = phase detector gain, K_{VCO} = VCO gain, and N = divide counter.

For Filter B (Figure 3):

$$w_n = \sqrt{\frac{K_{\varnothing}K_{VCO}}{NC_1(R_1 + R_2)}}$$

$$d = 0.5w_n(R_2C_1 + \frac{N}{K_{\varnothing}K_{VCO}}) \qquad (10)$$

Figure 4 shows an active filter using an op amp from Application Note AN535/D.

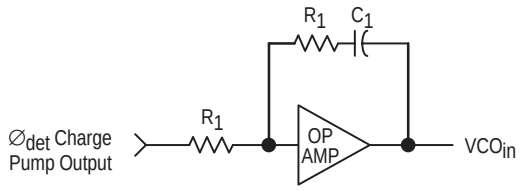

Figure 4. Op Amp Filter

For Figure 4, the equations become:

$$w_n = \sqrt{\frac{K_\varnothing K_{VCO}}{NC_1R_1}} \qquad (11)$$

$$d = \frac{K_\varnothing K_{VCO} R_2}{2w_n N R_1} \qquad (12)$$

$$= \frac{w_n C_1 R_2}{2}, \text{where Op Amp gain is large}$$

From the above equations, it is possible to design a suitable filter to meet the needs of many PLL applications. The inclusion of R_2 in the equations for Figure 3 and Figure 4 permits the capability to change w_n and d separately while Figure 2 equations do not. Normally, a design is easier if w_n and d can be chosen independently. Both factors affect the loop acquisition time and stability. A good starting value for d is 0.707 and $F_{ref}/10$ for w_n.

Manipulation of the equations allows calculation of R_1, R_2, and C_1 from the other measured, calculated, or picked parameters. For example,

$$R_1 + R_2 = \frac{K_\varnothing K_{VCO}}{NC_1 w_n^2} \qquad (13)$$

$$R_2 = \frac{2d}{C_1 w_n} - \frac{N}{C_1(K_\varnothing K_{VCO})} \qquad (14)$$

$$C_1 = \frac{K_\varnothing K_{VCO}}{N w_n^2 (R_1 + R_2)}, \text{ or alternatively,}$$

$$C_1 = \frac{2d}{R_2 w_n} - \frac{N}{R_2(K_\varnothing K_{VCO})}$$

Usually, C_1, w_n, and d are picked and the remaining parameters calculated.

DESIGN EXAMPLE

The goal is to design a phase–locked loop that has an F_{ref} of 100KHz, an output F_o of 1MHz center frequency, and the ability to move from 200KHz to 2MHz in 100KHz steps.

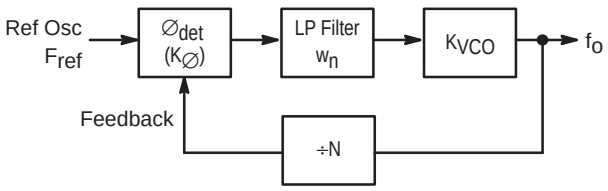

Figure 5. Parametized PLL

To determine N, use equation (1) for F_o min = 200KHz, and F_o max = 2MHz resulting in the following:

N min = 200/100 = 2, and

N max = 2000/100 = 20

The results so far indicate the following starting parameters:

A. A VCO with a 10:1 range is required

B. $w_n = F_{ref}/10 = 10KHz$

C. d = 0.707

D. $R_2 = \infty$

E. $V_{dd} = 5.0V$

The F_o center frequency ≈

$$\frac{F_{max} + F_{min}}{2} = \frac{2.0 + 0.2}{2} = 1.1MHz$$

Recalling that the clamp voltage % at V_{dd} = 5V is about 62, then F_{max} VCO_{in} limit = (0.62)(5) = 3.1V, but as described earlier, this needs to be reduced by a factor to bring it into linearity (≈ 350mV) so the final F_{max} VCO_{in} limit = 2.75V.

For the F_{min} VCO_{in} limit pick 0.25V. This results in a center frequency VCO_{in} of:

$$\text{Center freq } VCO_{in} = \frac{2.75 - 0.25}{2} = 1.25V$$

From 2, for picked values of $9.1K \le R_1 \le 50K$ and $30 \le C_{ext} \le 150$, obtain an estimate for $(R_1)(C_{ext})$ of $5.77/F_o$. Thus, at the F_o center frequency,

$$(R_1)(C_{ext}) = \frac{5.77}{1.1 * 10^6} = 5.245 * 10^{-6}$$

Now, a reasonable starting point is established for setting the values of the loop filter and the VCO range. Choosing R_1 = 9.1K, C_{ext} becomes

$$C_{ext} = \frac{5.245 * 10^{-6}}{9.1K} = 576pF \text{ WHOOPS!}$$

This value, 576pF, is outside of the original picked range for C_{ext}; therefore, we need to go back and pick a larger value of R_1, e.g., 42K should be sufficient. Then C_{ext} becomes

$$C_{ext} = \frac{5.245 * 10^{-6}}{42K} = 125pF$$

and now both R_1 and C_{ext} are within selected ranges.

Now calculate F_{max} and F_{min} using Equation (8) with R_1 = 42kΩ, $R_2 = \infty$, V_{dd} = 5.0V, $I_{constant\ ratio}$ = 27 (from 1. and R_1 = 42kΩ), $V_{undershoot}$ = 0.57V (calculated from 6pF/mV (125pF–30pF) = 0.57V), VCO_{in} min = 0.25V, and VCO_{in} max = 2.75V:

$$F_o\,min = \frac{\frac{(3)(0.25)(27)}{42K} + \frac{(9.2)(5.0)}{\infty}}{(2)(125 * 10^{-12}f)\ [5.0V + 3(0.57V)]}$$

$$= \frac{20.25}{70.455 * 10^{-6}} = 287.4KHz$$

$$F_o\,max\frac{\frac{(3)(2.75)(27)}{42K} + \frac{(9.2)(5.0)}{\infty}}{(2)(125 * 10^{-12}f)\ [5.0V + 3(0.57V)]}$$

$$= \frac{222.75}{70.455 * 10^{-6}} = 3.16MHz$$

F_{max} is > the required 2.0MHz, but the F_{min} is not low enough for required application. It is necessary to adjust either C_{ext} or R_1 to achieve required specification of 0.2 to 2.0MHz F_o. Since R_1 = 42kΩ is a standard resistor value, try adjusting C_{ext} to a higher value, such as 175pF. Because C_{ext} is now > 150pF, the $V_{undershoot}$ must be adjusted to 0.7V, as per earlier explanation:

So,

$$F_o\,min = \frac{\frac{(3)(0.25)(27)}{42K} + \frac{(9.2)(5.0)}{\infty}}{(2)(175 * 10^{-12}f)\ [5.0V + 3(0.7V)]}$$

$$= \frac{20.25}{104.37 * 10^{-6}} = 194.02KHz$$

and

$$F_o\,max\frac{\frac{(3)(2.75)(27)}{42K} + \frac{(9.2)(5.0)}{\infty}}{(2)(175 * 10^{-12}f)\ [5.0V + 3(0.7V)]}$$

$$= \frac{222.75}{104.37 * 10^{-6}} = 2.13MHz$$

These values are adequate for the specified application.

The next item to determine is the VCO gain factor, K_{VCO}, using Equation (9):

$$K_{VCO} = \frac{f\,max\ -\ f\,min}{VCO_{in}\,max\ -\ VCO_{in}\,min}$$

$$K_{VCO} = \frac{2.13 * 10^6\ -\ 0.194 * 10^6}{2.75V\ -\ 0.25V} = 774.4KHz/V$$

or in radians

$$= (2\pi)\ (774.4 * 10^3) = 4.86 * 10^6 Rad/sec/V$$

The final values used for the desired frequency range are R_1 = 42kΩ, C_{ext} = 175pF, $R_2 = \infty$, VCO_{in} max = 2.75V, and VCO_{in} min = 0.25V.

The next step is to determine the loop filter. Choosing a filter like the one in Figure 3, calculate the component as follows:

$$K_\phi = \frac{V_{dd}}{4\pi} = \frac{5.0}{4\pi} = 0.4V/rad$$

$$w_n = \frac{100KHz}{10} = 10KHz * 2\pi = 62.83 * 10^3 rad/sec$$

d = 0.707 (for starters), and

N = 2 to 20

where

$K_\varnothing$ = phase detector gain

V_{dd} = output swing

Choose C_1 to be 0.01μF, N = 10 for approximate mid–range F_o, and calculate R_1 and R_2 using Equations (13) and (14):

$$R_1 + R_2 = \frac{K_\phi K_{VCO}}{NC_1 w_n^2} = \frac{(0.4)(4.86 * 10^6)}{(10)(0.01 * 10^{-6})(62.83 * 10^3)^2}$$

$$= \frac{1.944 * 10^6}{394.76} = 4924.5\Omega$$

$$R_2 = \frac{2d}{C_1 w_n} - \frac{N}{C_1(K_\phi K_{VCO})}$$

$$= \frac{(2)(0.707)}{(0.01 * 10^{-6})\ (62830)} - \frac{10}{(0.01 * 10^{-6})(0.4)(4.86 * 10^6)}$$

$$= 2250.52–514.4 = 1736\Omega$$

Then, R_1 = 4924.5 – 1736 = 3188.5Ω.

Since N is changeable, it is a good idea to check min and max on w_n and d. For more information on why, see Application Note AN535/D or the MC4044 Data Sheet in the MECL Data Book DL122/D. The following examples show sample calculations for N = 2 and 20.

For N = 20, use Equation (10) to calculate w_n and d:

$$w_n\,min = \sqrt{\frac{K_\phi K_{VCO}}{NC_1(R_1 + R_2)}}$$

$$= \sqrt{\frac{(0.4)(4.86 * 10^6)}{(20)(0.01 * 10^{-6})(3188.5 + 1736)}}$$

$$= 44.43 * 10^3 rad/sec,\ or$$

$$= \frac{44.43 * 10^3 rad/sec}{2\pi} \approx 7KHz$$

and

$$d_{min} = (0.5)(w_n)\left[R_2C_1 + \frac{N}{K_\phi K_{VCO}}\right]$$

$$= (0.5)(44.43 * 10^3) * \left[(1736)(0.01 * 10^{-6}) + \frac{20}{(0.4)(4.86 * 10^6)}\right]$$

$$= 0.6144$$

For N = 2:

$$w_{n\,max} = \sqrt{\frac{(0.4)(4.86 * 10^6)}{(2)(0.01 * 10^{-6})(3188.5 + 1736)}}$$

$$= 140.49 * 10^3 \text{rad/sec, or}$$

$$= \frac{140.49 * 10^3 \text{rad/sec}}{2\pi} = 22.36\text{KHz}$$

and

$$d_{max} = (0.5)(140.49 * 10^3) * \left[(1736)(0.01 * 10^{-6}) + \frac{2}{(0.4)(4.86 * 10^6)}\right]$$

$$= 1.292$$

This shows the effect of changing n on loop performance and for this application is adequate.

If the components are not what is desired, choosing a different w_n and/or d allows them to be modified.

Alternatively, picking different C, R_1 or R_2 and recalculating the other parameters can be done. If the filter does not provide adequate performance, making w_n smaller or d larger may improve stability.

Characterization of Retrigger Time in the HC4538A Dual Precision Monostable Multivibrator

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APPLICATION NOTE

Introduction

The MC74HC4538A is a monostable multivibrator commonly used as a one–shot, or in applications that require a pulse width of reliable dimensions. The pulse width and the minimum retrigger time are usually well behaved over the suggested pulse–width range of 1μs to 1 second. However, some customers have found that in using shorter than recommended pulse widths the retrigger time did not behave as it had at longer pulse widths. ON Semiconductor has done an overall characterization of the minimum retrigger time in an investigation of this phenomenon.

The retrigger time is applicable when the device is triggered a second time within the period of the output pulse. When this happens, the output pulse remains high for a period of $\tau + T_{rr}$. The earliest the part can be retriggered, or the minimum retrigger time, is the focus of this characterization. A trigger pulse on A or B inputs before this minimum retrigger time would be ignored.

Analysis and Data

When used in the retriggerable mode (Figure 1), the MC74HC4538A uses an external R_X & C_X to regulate the output pulse width, and the minimum retrigger time (T_{rr}). The minimum retrigger time depends on:

1) Time to discharge R_XC_X from V_{CC} to (V_{ref} lower=1/3 V_{CC}) $T_{discharge}$. This discharge occurs quickly because external resistance, R_X, does not have any effect on the R_C time constant. The resistance in the discharge path, as seen in Figure 2, is the on–resistance of M3, and the interconnect resistance. The interconnection resistance is dependent on the polysilicon sheet resistance, the metal sheet resistance, and the contact resistance. The interconnection resistance is heavily process dependent, but fortunately it is small overall and doesn't vary significantly from lot to lot.
The discharge time can be computed from:

$$T_{discharge} = \left(Ln\frac{3}{2}\right) \cdot R_i \cdot C_X$$

(Equation 1)

Typically the value of R_i would be near 300Ω.

2) Loop delay (T_{delay} = constant) ranges from 20–60ns, and is strongly correlated to V_{CC}. This is the time for the signal coming from the lower reference circuit to reset the flip–flop, and turn off M3. The amount of the undershoot voltage is a function of the loop delay, and for small values of capacitance the undershoot voltage is well below the lower reference voltage.

3) The time to charge R_XC_X from the undershoot voltage back to the lower reference voltage (V_{ref} lower). This time is given by the R_XC_X transient equation:

$$T_{charge} = R_X \cdot C_X \cdot Ln\left(1 + \frac{3 \cdot V_{undershoot}}{2 \cdot V_{CC}}\right)$$

(Equation 2)

where $V_{undershoot}$ = (V_{ref} lower) – Gnd. Hence the retrigger time is given by:

$$T_{rr} = T_{discharge} + T_{delay} + T_{charge}$$

(Equation 3)

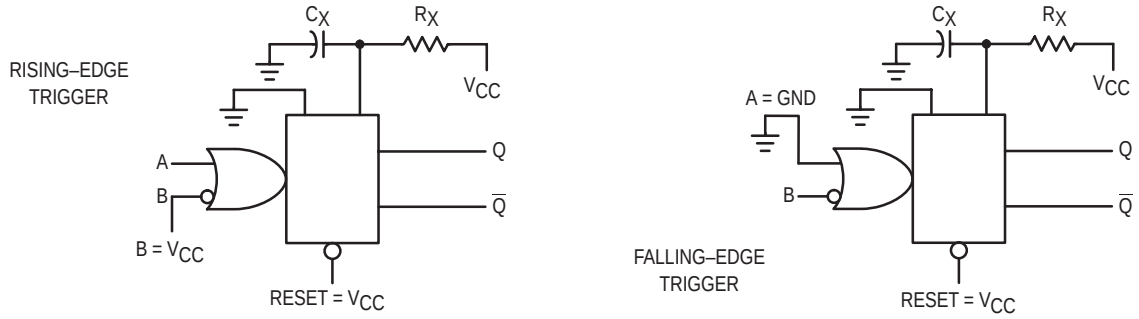


Figure 1. Retriggerable Monostable Circuitry

LOGIC DETAIL
(1/2 THE DEVICE)

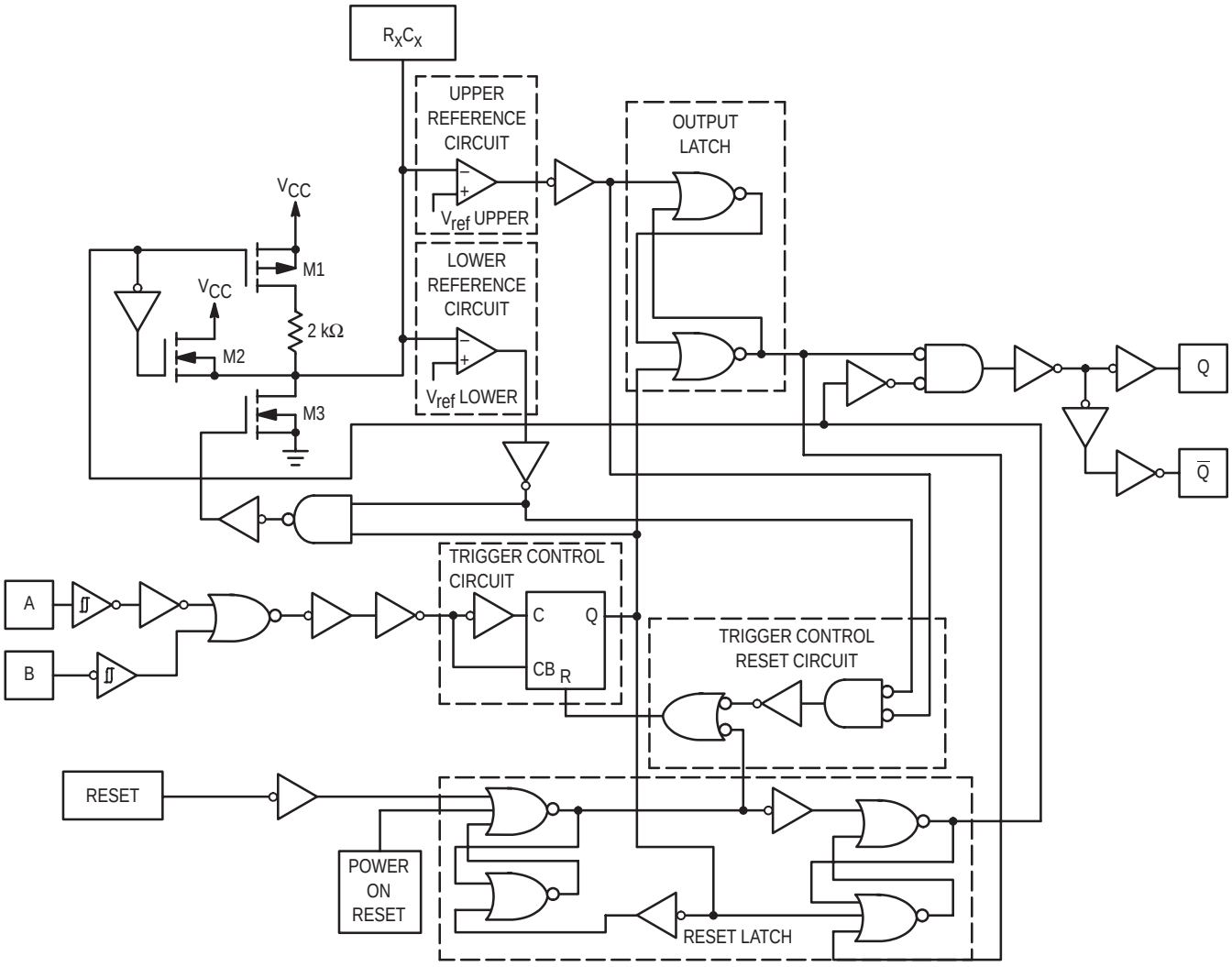


Figure 2. MC74HC4538A Logic Circuit Detail

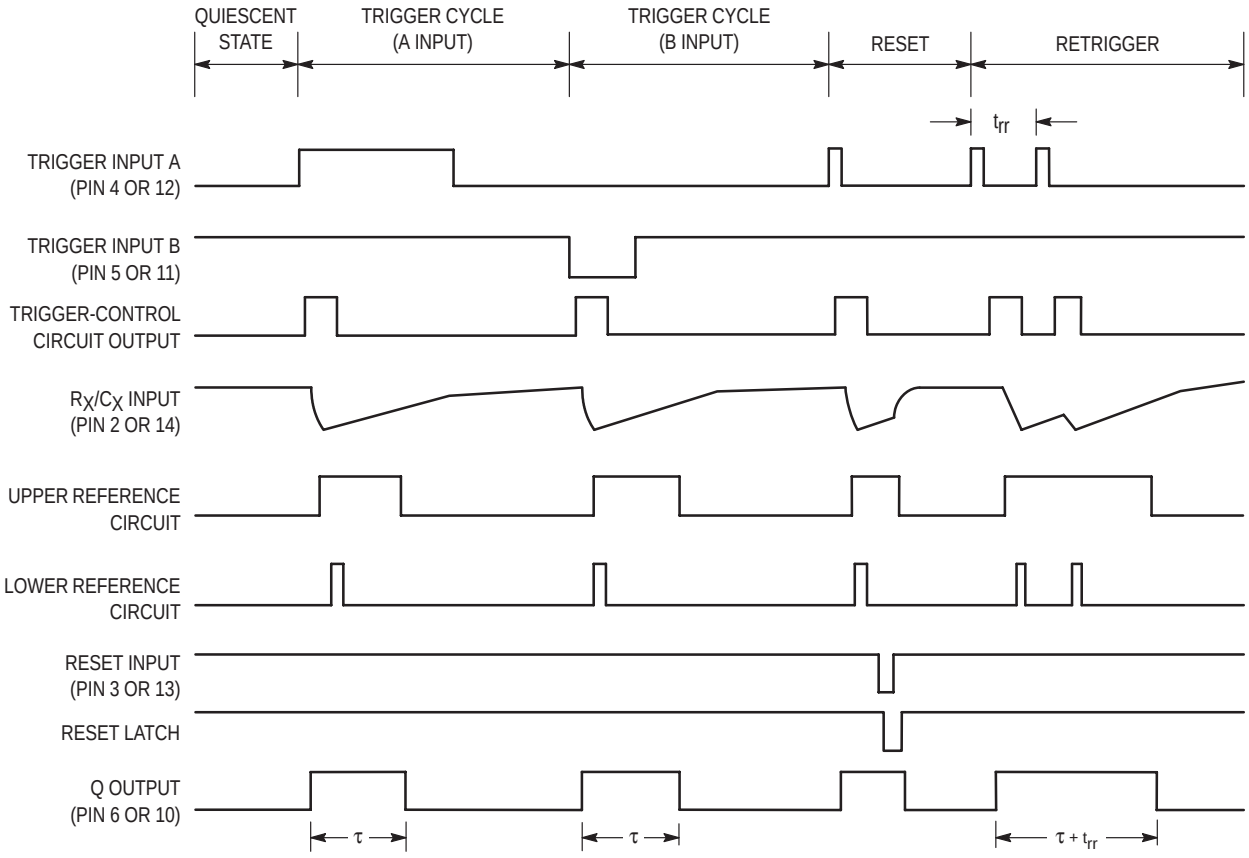


Figure 3. Timing Diagram

Design and Applications

The output pulse width of the HC4538A is determined by the external timing components, R_X and C_X, and can be represented linearly as shown in Figure 10.

The array in Table 1 was generated to make a concise study of the behavior for the retrigger time for short pulse widths. A sample of 10 pieces from each of 7 non–consec–utive wafer lots were tested at each condition.

The retrigger time for external capacitance that ranges from 3000pF < C_X < 4.7μF, Region 3 on the graphs, can be computed by making use of the following linear equation (Equation 4).

Table 1. Test Matrix

C_X/R_X	10pF	100pF	220pF	1000pF
2KΩ	4.5V	4.5V	4.5V	4.5V
10KΩ	3.0V 4.5V	3.0V 4.5V	3.0V 4.5V	3.0V 4.5V
100KΩ	3.0V 4.5V	3.0V 4.5V	3.0V 4.5V	3.0V 4.5V
1MΩ	3.0V 4.5V	3.0V 4.5V	3.0V 4.5V	3.0V 4.5V

$$T_{rr} = 10^{z},$$

$$\text{where } z = \Big[-1062.41 - (0.1236764 \cdot V_{CC}) + (1.13509292 \cdot (\text{Log } C_X)^3) - (2.875 \times 10^{-17} \cdot R_X^3) + (3.5256 \times 10^{-16} \cdot (\text{Log } C_X)^2 \cdot R_X) + (5.9621 \times 10^{-12} \cdot (\text{Log } C_X) \cdot R_X^2) + (4.03306325 \cdot (\text{Log } C_X)^2) + (7.9452 \times 10^{-11} \cdot R_X^2) + (5.1513 \times 10^{-5} \cdot (\text{Log } C_X) \cdot R_X) + (0.02312176 \cdot \text{Log } R_X) + (1.8339 \times 10^{-4} \cdot R_X) - (171.91718 \cdot \text{Log } C_X) + (4.64784302 \times 10^{8} \cdot C_X) \Big]$$

Equation 4. Retrigger Time for 4.7μF > C_X > 3000pF

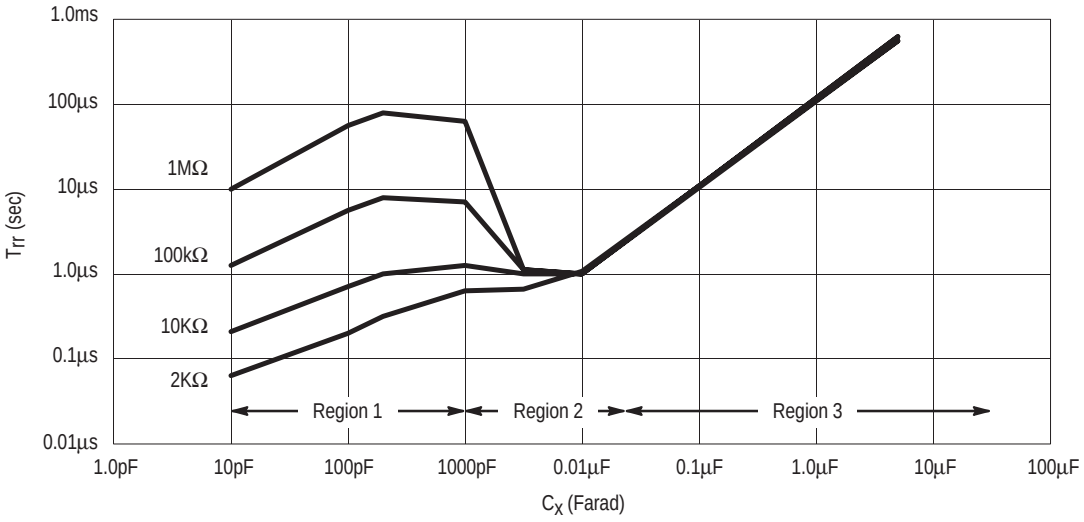


Figure 4. Retrigger Time versus Timing Capacitance at V_{CC} = 4.5V

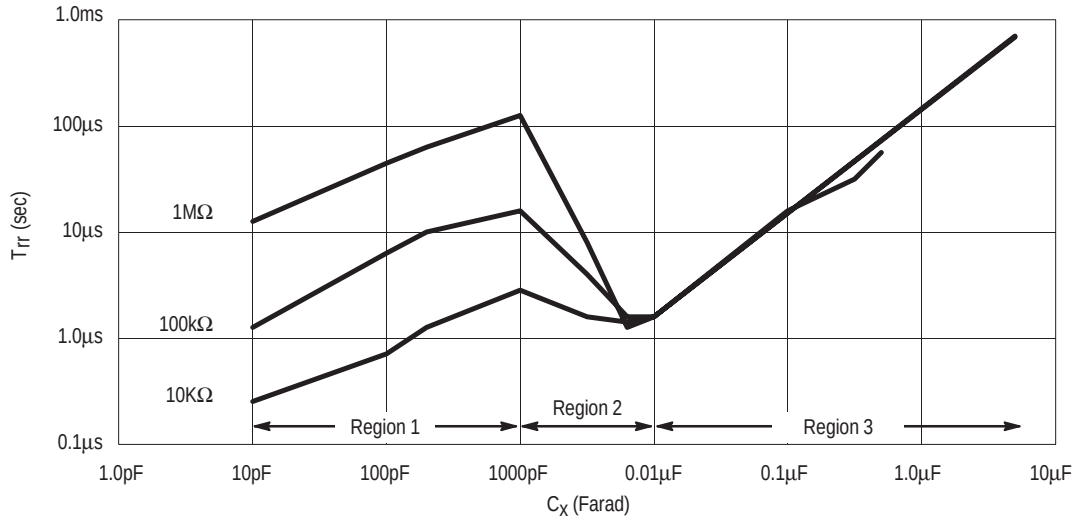


Figure 5. Retrigger Time versus Timing Capacitance at V_{CC} = 3.0V

For values of 1000pF < C_X < 3000pF, the non–linear portion of the curves are converging. In this region, Region 2, the equation was represented by too few measurements to generate a reasonably accurate equation. Therefore, the equation in Region 2 will remain underived. A value may be approximated from the graphs in Figure 4 and Figure 5.

It was determined from experiment and statistical analysis of the data that the retrigger time for small values of external capacitance within the range of 10pF < C_X < 1000pF, Region 1, can be characterized with the following linear equation (Equation 5).

$$T_{rr} = 10^{z},$$

$$\text{where } z = \left[-315.29624 - (0.082881 \bullet V_{CC}) - (0.3146338 \bullet (\text{Log } C_X)^3) + 4.3277 \times 10^{-16} \bullet R_X^3 \right) -$$
$$(3.984 \times 10^{-7} \bullet (\text{Log } C_X)^2 \bullet R_X) + (3.0657 \times 10^{-12} \bullet (\text{Log } C_X) \bullet R_X^2) - (9.467093 \bullet (\text{Log } C_X)^2) -$$
$$(4.575 \times 10^{-10} \bullet R_X^2) - (1.124 \times 10^{-5} \bullet (\text{Log } C_X) \bullet R_X) - (94.092747 \bullet \text{Log } C_X) +$$
$$(1.36599588 \times 10^{8} \bullet C_X) - (1.423 \times 10^{-5} \bullet R_X) \left]$$

Equation 5. Retrigger Time for $10pF < C_X < 1000pF$

Here, the same components of:

$$T_{rr} = T_{discharge} + T_{delay} + T_{charge}$$

(Equation 3)

are still represented, but have become combined by the linear regression. The constant and V_{CC} dependent term still derive from the loop delay, and serve to shift the components along the vertical axis. The major difference between this and the larger values of C_X is twofold.

First, over all of Region 3 the undershoot is effectively 0 volts. This results in T_{charge} not contributing to T_{rr} and the predictable minimum T_{rr} occurring in Region 2.

Second, as we progress to smaller values of capacitance in Region 1, C_X is too small to support V_{ref}lower as the charge is drained through M3. This is why the resistance of R_X now plays a role in T_{rr}. This condition creates the undershoot of V_{ref}lower and the time of T_{charge} is then controlled by the current through R_X. This is also why as the value of C_X increases for the same resistance, T_{rr} increases as it takes longer to charge the larger capacitor. For values of $R_X > 10k\Omega$, this increasing undershoot of V_{ref}lower and the resultant increase in T_{charge} negates any improvement in T_{rr}.

At small values of C_X, the circuit capacitance will also come into play. The size of the undershoot of V_{ref}lower can vary as a function of normal process variance. This will also introduce an uncertainty into T_{rr} for these smaller values. The curves and regression equations here were derived statistically and only represent the mean of the variance in 7 non–consecutive production lots.

This difference in the non–zero value of T_{charge} in Region 1 can also be seen in Figure 6 and Figure 7 as the slope of T_{rr} becomes zero as the undershoot becomes zero.

Also, note that in Figure 8 through Figure 11, this effect has no influence on the Output Pulse Width as the Pulse Width is controlled by R_XC_X and V_{ref}upper.

$$\tau = 10^{z},$$

$$\text{where } z = \left[-1.0059363 - (7.6336 \times 10^{-3} \bullet V_{CC}) + (0.87653815 \bullet \text{Log } R_X) + \right.$$
$$\left. (0.8635535 \bullet \text{Log } C_X) - (9.3203 \times 10^{-3} \bullet \text{Log } R_X \bullet \text{Log } C_X) \right]$$

Equation 6. Pulse Width

Equation 6 is a linear regression equation for calculating the pulse width and is also made from the data means. From the logarithmic plots in Figure 8 through Figure 11, it can be seen that there is no cubic dependency similar to T_{rr}, even at the small values of capacitance. The pulse width is completely controlled by the relationship between R_XC_X and V_{ref}upper. This predictability of the pulse width has tempted some customers into trying to use the part for very short pulse widths. Unfortunately it has also resulted in inconsistent performance for T_{rr}.

Summary

While smaller pulse widths and T_{rr} values can be achieved, selection of the external components must take into account the introduction of undershoot of V_{ref}lower. Also, as we have stated above, as the value of C_X decreases in the non–linear region, the total capacitance becomes more dependent upon internal circuit capacitance. Since the internal circuit capacitance is process dependent, it can vary from lot to lot, and from manufacturing site to manufacturing site. It is for this reason that the device is not recommended to be used in this range, as doing so would potentially result in inconsistent performance over large production runs. The curves represented in this applications note were made using linear regression on a number of lots widely separated in time, but all from the same manufacturing site. As a result, the curves can only be regarded as statistical means, and may not represent the performance of any particular device the customer may encounter.

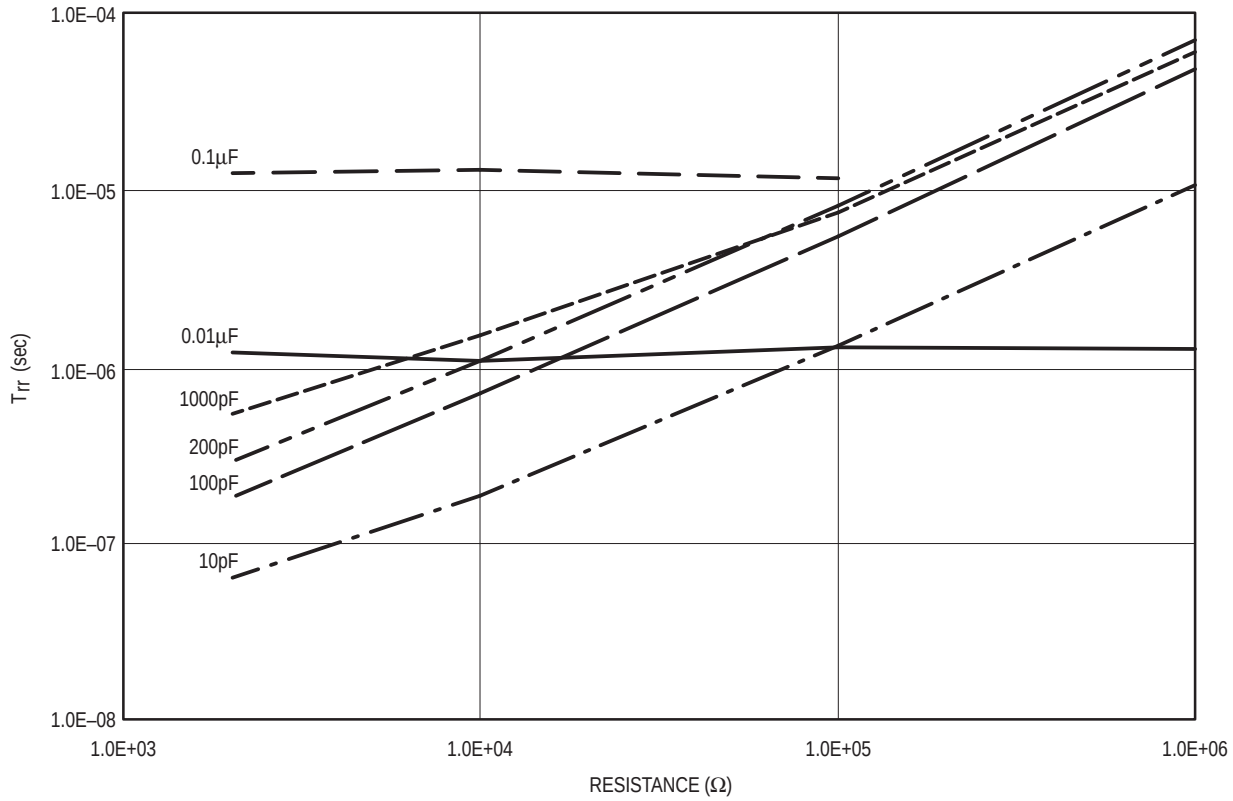


Figure 6. Retrigger Time vs Resistance at V_{CC} = 4.5V

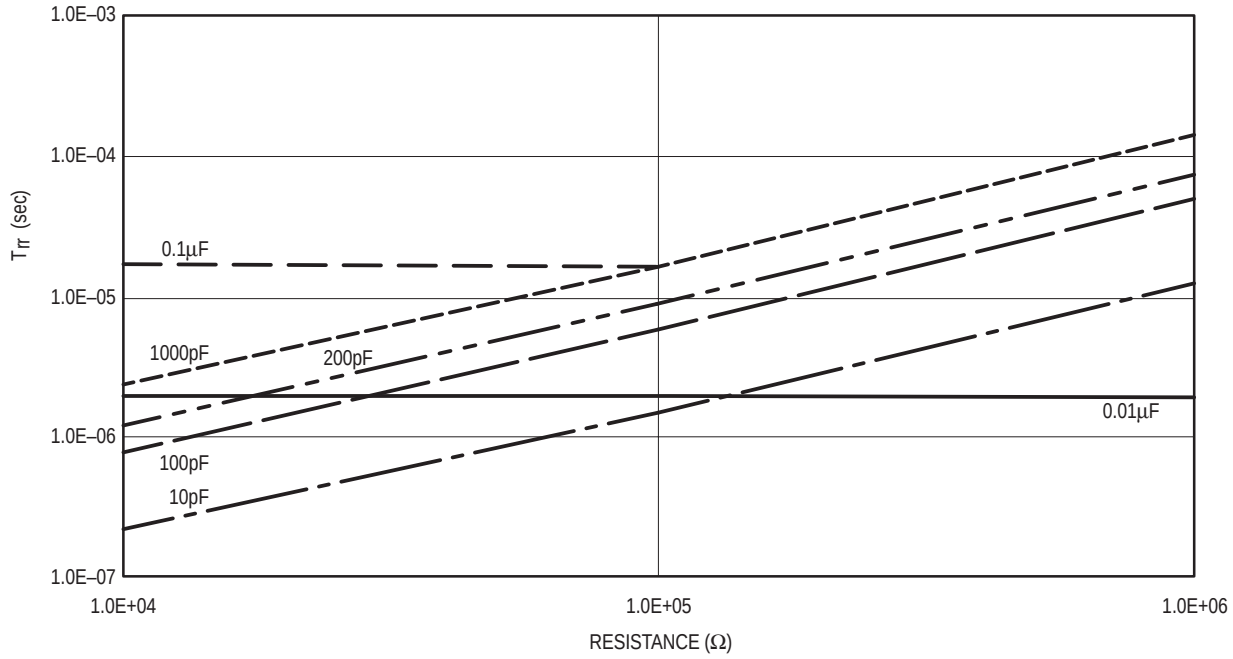


Figure 7. Retrigger Time vs Resistance at V_{CC} = 3.0V

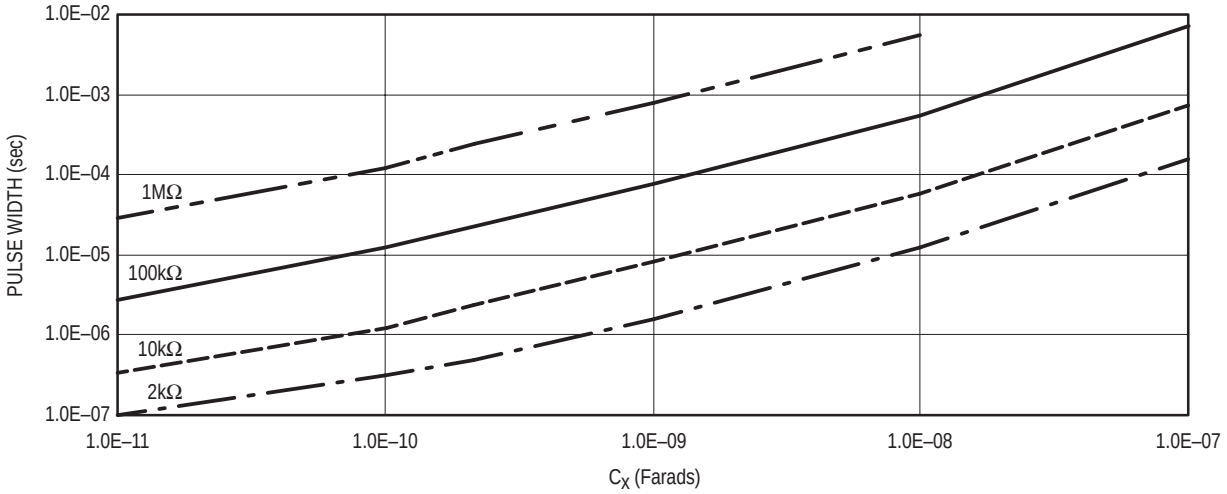


Figure 8. Pulse Width vs Timing Capacitance at V_{CC} = 4.5V

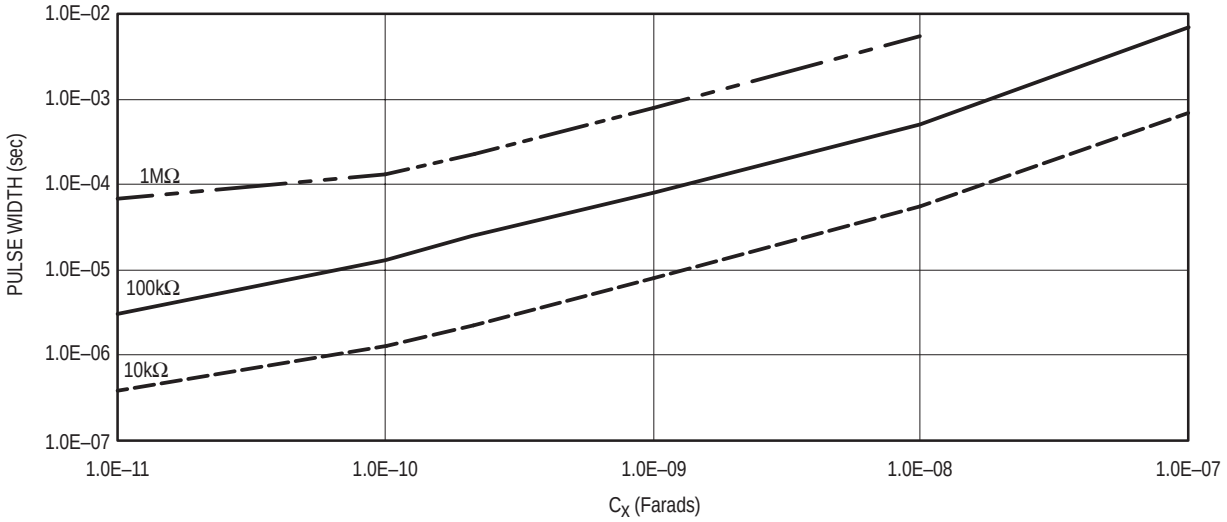


Figure 9. Pulse Width vs Timing Capacitance at V_{CC} = 3.0V

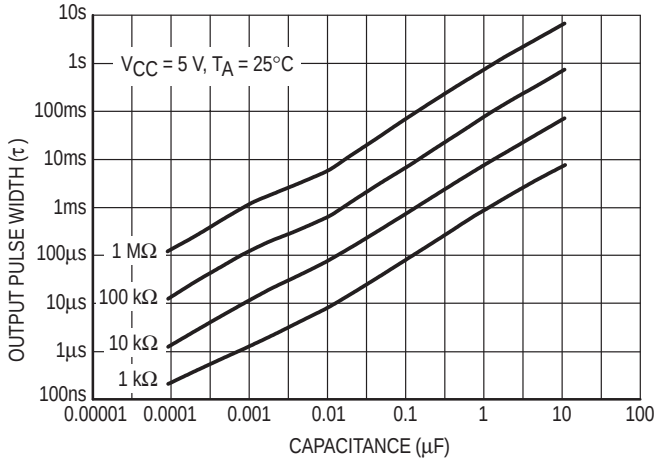


Figure 10. Output Pulse Width vs Timing Capacitance

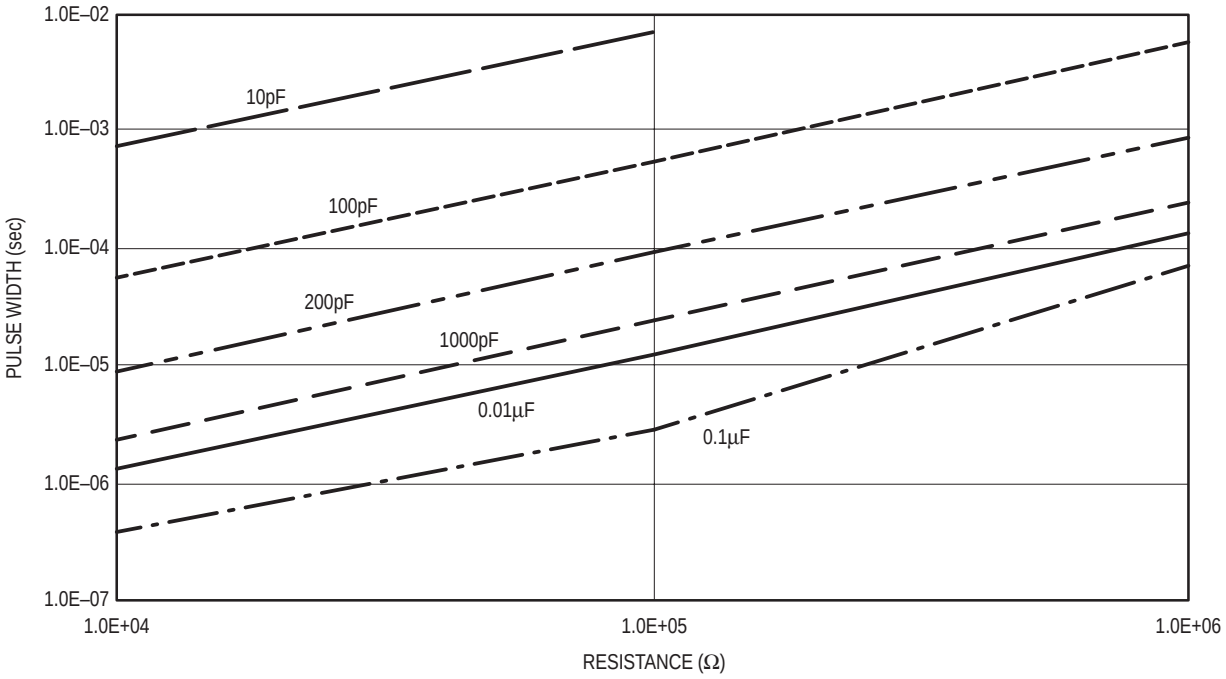


Figure 11. Pulse Width versus Resistance at V_{CC} = 3.0V

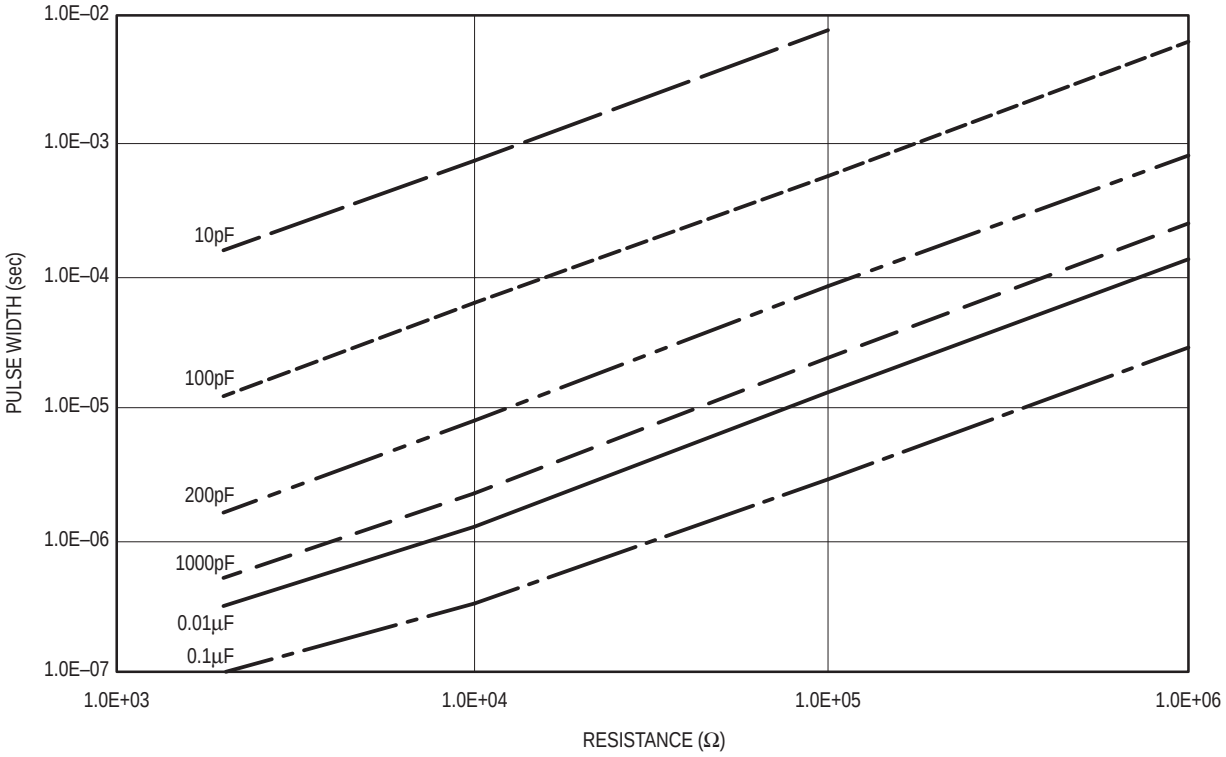


Figure 12. Pulse Width versus Resistance at V_{CC} = 4.5V

CHAPTER 5
Case Outlines and Ordering Information

High–Speed CMOS Family
Device Nomenclature

MC VV WWW XXXX Y

ON Semiconductor Circuit Identifier

Temperature Range
- 74 Series (–55 to +125°C)

High–Speed CMOS Specification Identifier
- HC = Buffered High–Speed CMOS
- HCU = Unbuffered High–Speed CMOS*
- HCT = High–Speed CMOS TTL Compatible

Function Type
- XX(X) Same Function and Pin Configuration as LSTTL
- 4XXX Same Function and Pin Configuration as CMOS 14000
- 7XX(X) Variation of LSTTL or CMOS 14000 Device

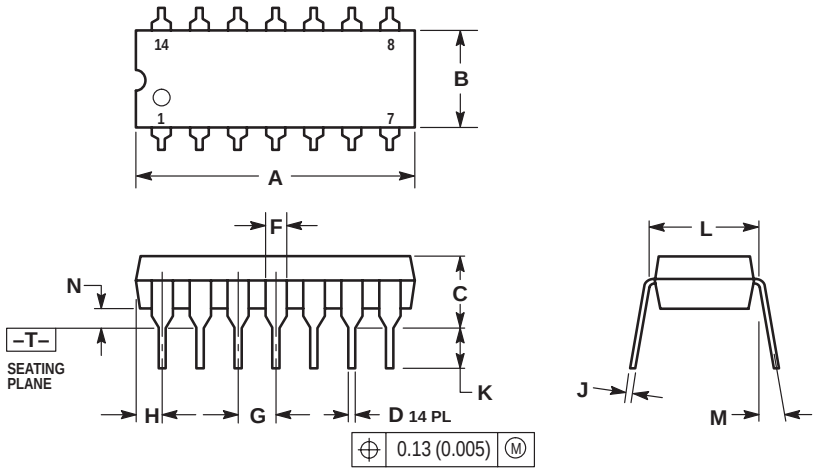
Package Type
- D for 150 mil Plastic SOIC
- DT for TSSOP
- DW for 300 mil Plastic SOIC
- F for 200 mil EIAJ SOIC
- N for Plastic PDIP

***Not Available On All Devices**

Case Outlines

14-Pin Packages

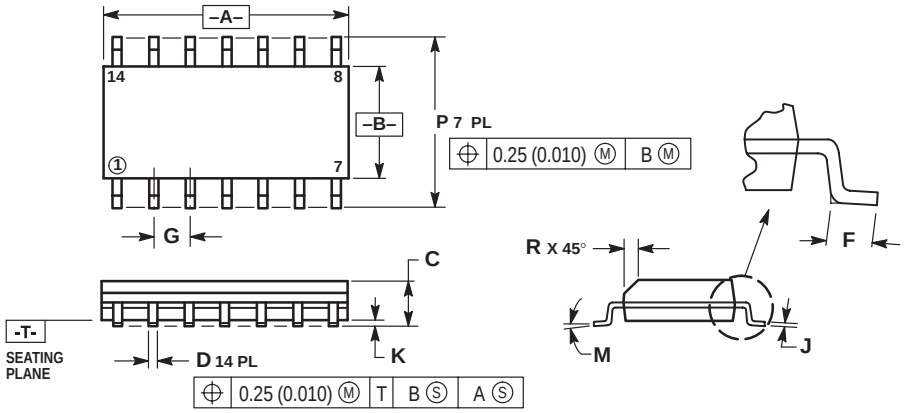
PDIP–14
N SUFFIX
PLASTIC DIP PACKAGE
CASE 646–06
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	—	10°	—	10°
N	0.015	0.039	0.38	1.01

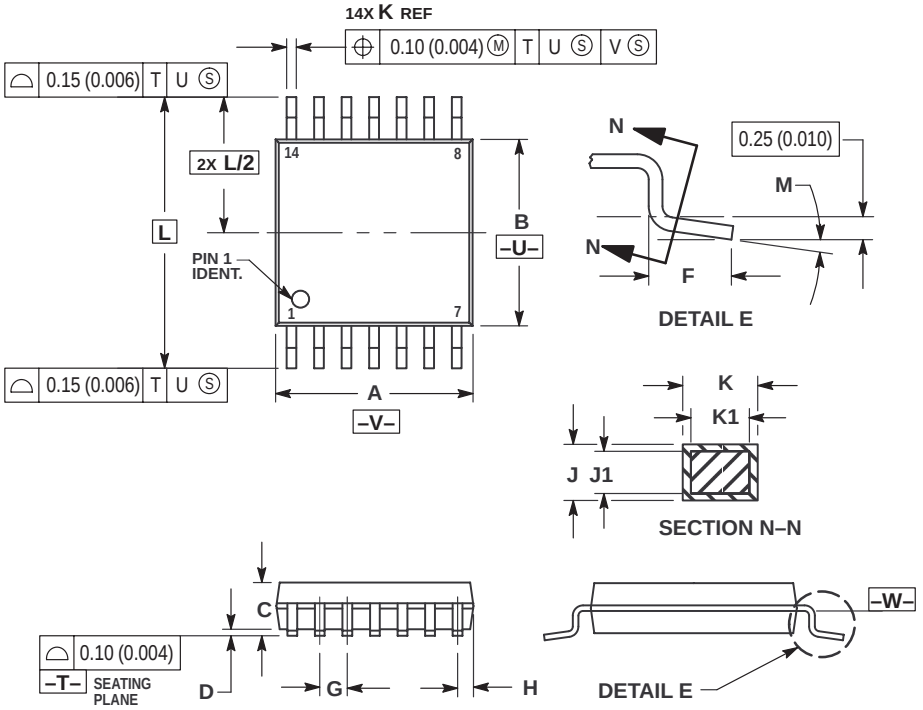
SO–14
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

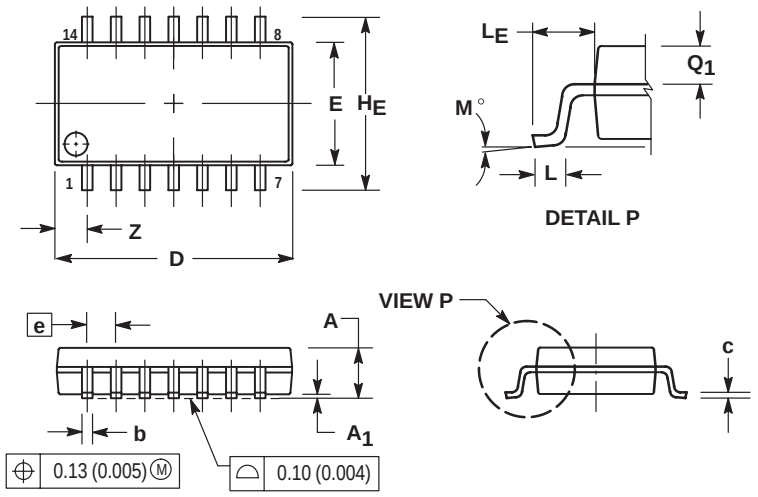
TSSOP–14
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948G–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SO–14 EIAJ
F SUFFIX
PLASTIC EIAJ SOIC PACKAGE
CASE 965–01
ISSUE O

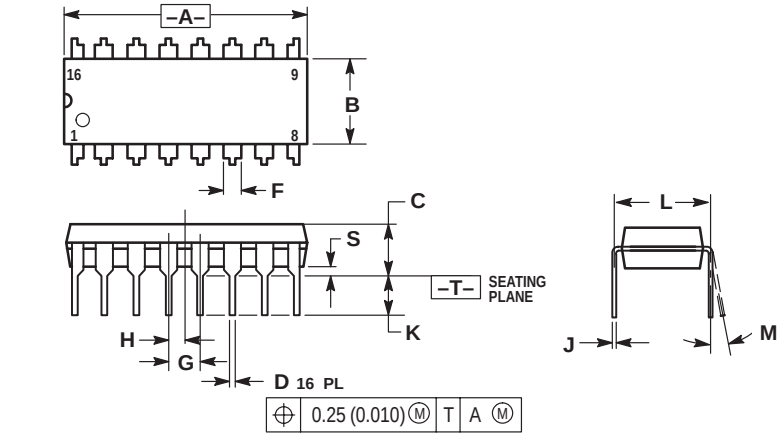


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	—	1.42	—	0.056

16-Pin Packages

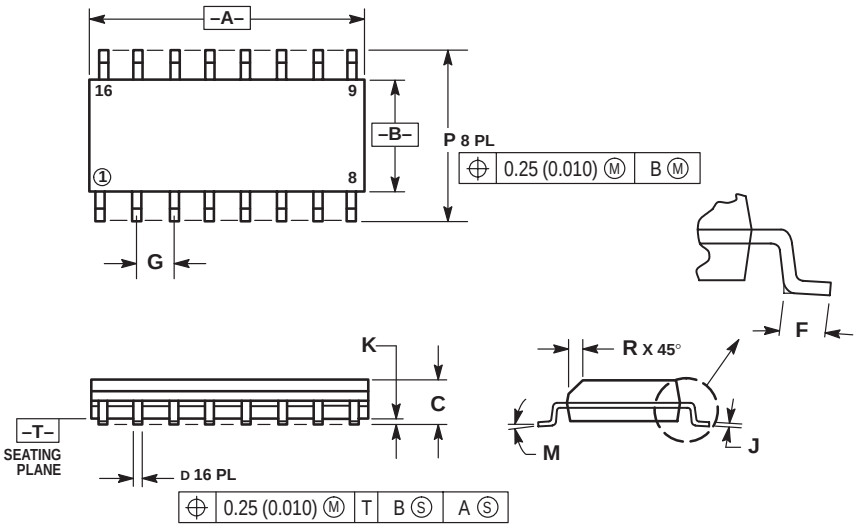
PDIP–16
N SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

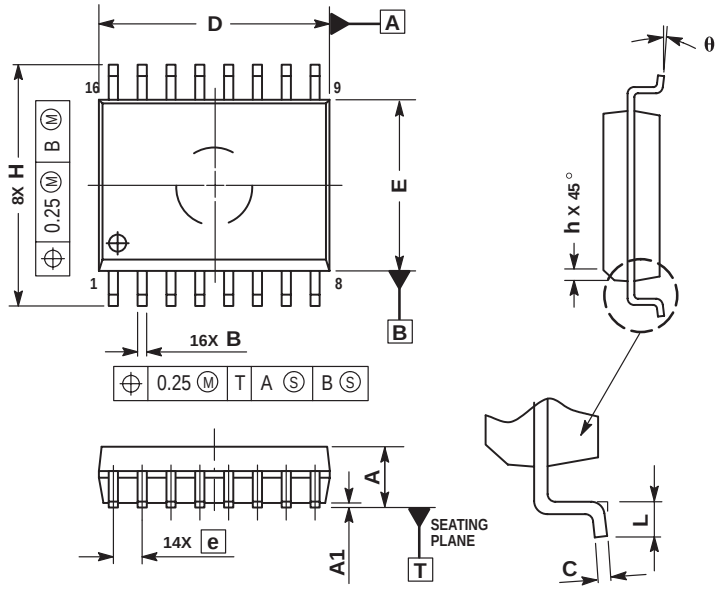
SO–16
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

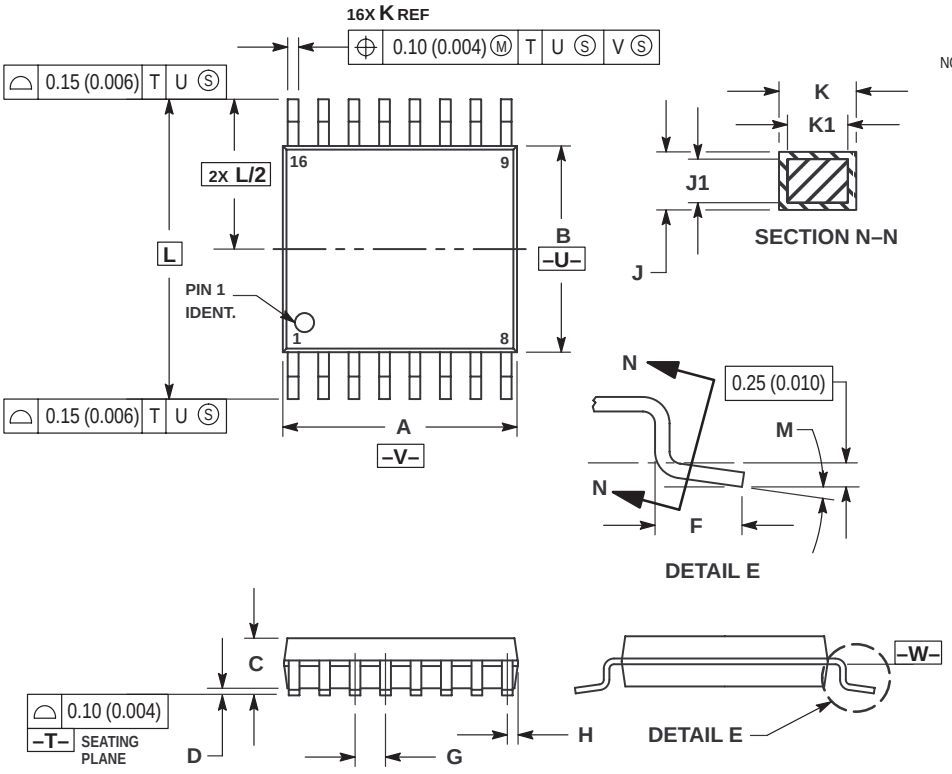
SO–16 WIDE
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751G–03
ISSUE B



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

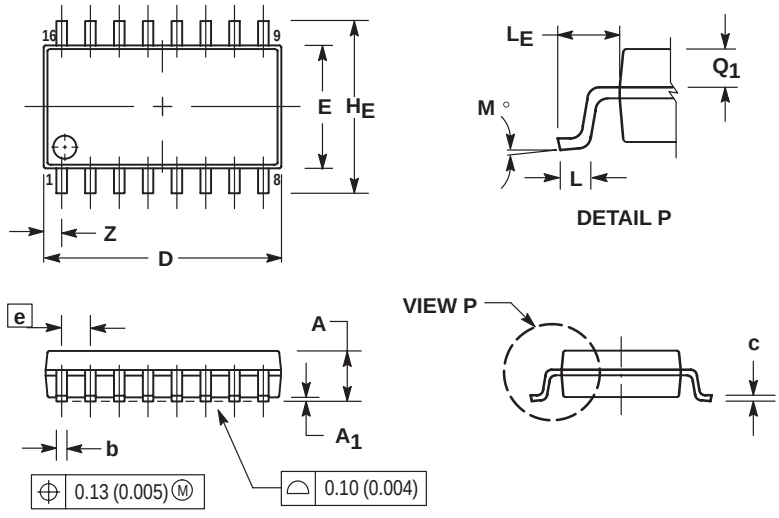
TSSOP–16
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948F–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SO–16 EIAJ
F SUFFIX
PLASTIC EIAJ SOIC PACKAGE
CASE 966–01
ISSUE O

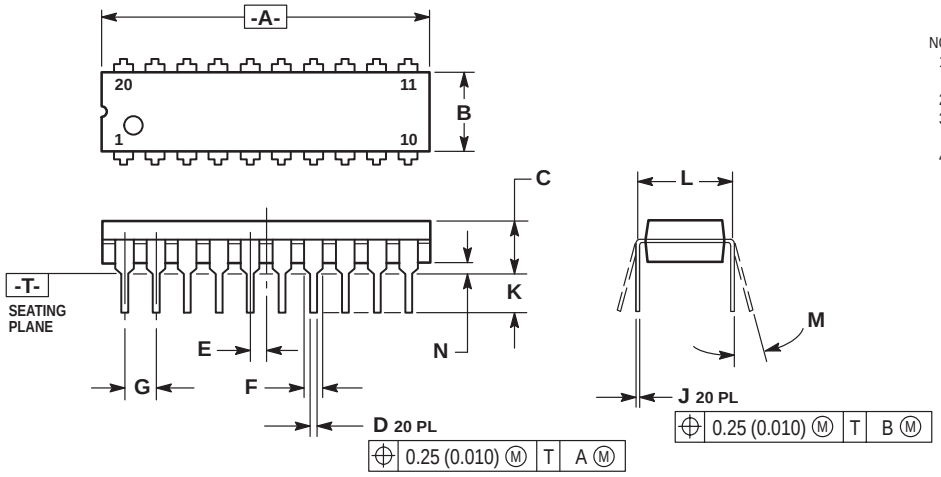


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	—	0.78	—	0.031

20-Pin Packages

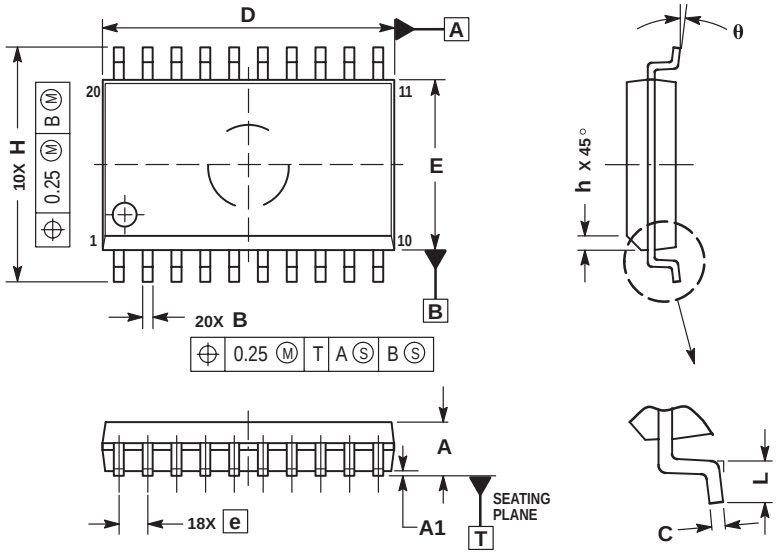
PDIP–20
N SUFFIX
PLASTIC DIP PACKAGE
CASE 738–03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

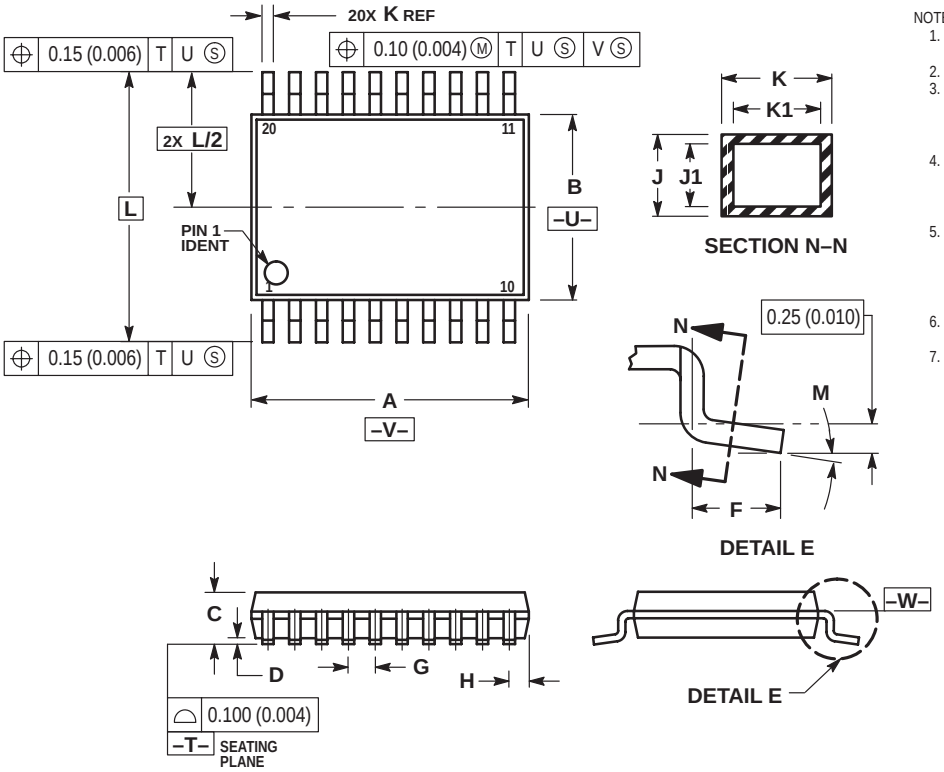
SO–20 WIDE
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–05
ISSUE F



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

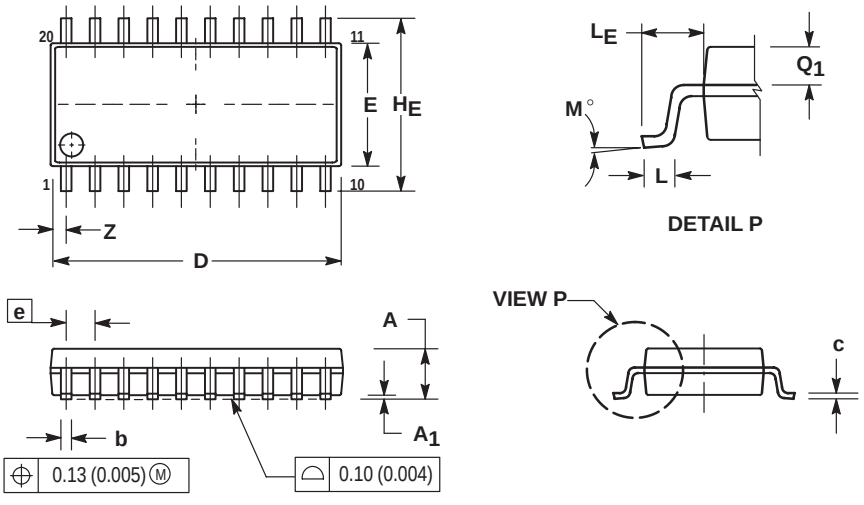
TSSOP–20
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948E–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SO–20 EIAJ
F SUFFIX
PLASTIC EIAJ SOIC PACKAGE
CASE 967–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q_1	0.70	0.90	0.028	0.035
Z	—	0.81	—	0.032

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A User's Guide contains procedural, task–oriented instructions for using or running a device or product. A User's Guide differs from a Reference Manual in the following respects:

* Majority of information (> 60%) is procedural, not functional, in nature
* Volume of information is typically less than for Reference Manuals
* Usually written more in active voice, using second–person singular (you) than is found in Reference Manuals
* May contain photographs and detailed line drawings rather than simple illustrations that are often found in Reference Manuals

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A Product Preview is a summary document for a product/device under consideration or in the early stages of development. The Product Preview exists only until an "Advance Information" document is published that replaces it. The Product Preview is often used as the first section or chapter in a corresponding reference manual. The Product Preview displays the following disclaimer at the bottom of the first page: "ON Semiconductor reserves the right to change or discontinue this product without notice."

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TECHNICAL DATA

The Technical Data document is for a product/device that is in full production (i.e., fully released). It replaces the Advance Information document and represents a part that is M, X, XC, or MC qualified. The Technical Data document is virtually the same document as the Product Preview and the Advance Information document with the exception that it provides information that is unavailable for a product in the early phases of development (such as complete parametric characterization data). The Technical Data document is also a more comprehensive document that either of its earlier incarnations. This document displays no disclaimer, and while it may be informally referred to as a "data sheet," it is not labeled as such.

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